

December 2014

FCPF190N65FL1

N-Channel SuperFET[®] II FRFET[®] MOSFET 650 V, 20.6 A, 190 m Ω

Features

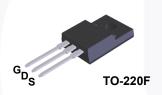
- 700 V @T_J = 150°C
- $R_{DS(on)} = 168 \text{ m}\Omega \text{ (Typ.)}$
- Ultra Low Gate Charge (Typ. Q_q = 60 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 304 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

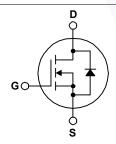
Applications

- LCD / LED / PDP TV Telecom / Server Power Supplies
- Solar Inverter
 AC DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		FCPF190N65FL1	Unit	
V _{DSS}	Drain to Source Voltage		650	V
	Cata ta Causaa Maltaga	- DC	±20	V
V_{GSS}	Gate to Source Voltage	- AC (f > 1 Hz)	±30	V
I _D Drain Current	Drain Current	- Continuous (T _C = 25°C)	20.6	^
	Drain Current	- Continuous (T _C = 100°C)	13.1	A
I _{DM}	Drain Current	- Pulsed (Note 1)	61.8	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		400	mJ
I _{AR}	Avalanche Current (Note 1)		4	Α
E _{AR}	Repetitive Avalanche Energy	0.39	mJ	
dv/dt	MOSFET dv/dt		100	\//no
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	50	V/ns
D	Davies Dissipation	$(T_C = 25^{\circ}C)$	39	W
P_{D}	Power Dissipation - Derate Above 25°C		0.31	W/°C
T _J , T _{STG}	Operating and Storage Temperate	-55 to +150	οС	
TL	Maximum Lead Temperature for S	Soldering, 1/8" from Case for 5 Seconds	300	οС

Thermal Characteristics

Symbol	Parameter FCPF190N65FL1			
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.2	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 62.5		*C/VV	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF190N65FL1	FCPF190N65F	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charae	cteristics					
D\/	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	650	-	-	V
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	700	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
I	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	-	10	μА
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 520 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	60	-	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	μΑ

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 2 \text{ mA}$	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	168	190	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 10 \text{ A}$	-	18	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		2350	3055	pF
Coss	Output Capacitance			77	100	pF
C _{rss}	Reverse Transfer Capacitance			0.68	-	pF
Coss	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	- \	44	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	- \	304	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 10 A,		60	78	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	12	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	25	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.6	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	25	60	ns
t _r		$V_{DD} = 380 \text{ V}, I_D = 10 \text{ A},$	-/	11	32	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_g = 4.7 Ω	-	62	134	ns
t _f	Turn-Off Fall Time	(Note 4)	/ -	4.2	18	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current			-	20.6	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	61.8	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 10 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 10 A,	-	105	- , ,	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	515	-	nC

Notes:

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I_{AS} = 4 A, R_{G} = 25 Ω , Starting T_{J} = 25°C
- 3. I $_{SD} \leq$ 10 A, di/dt \leq 200 A/ μ s, V $_{DD} \leq$ 380 V, Starting T $_{J}$ = 25°C
- 4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

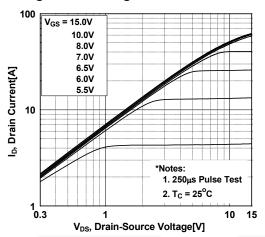


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

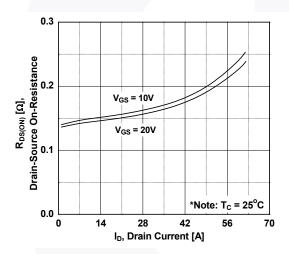


Figure 5. Capacitance Characteristics

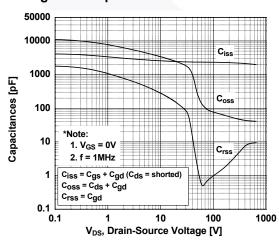


Figure 2. Transfer Characteristics

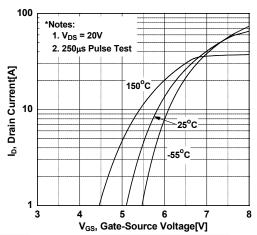


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

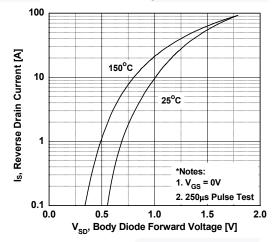
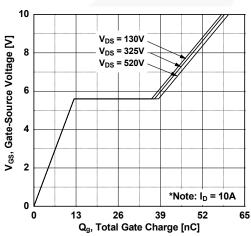


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

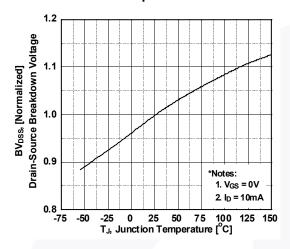


Figure 9. Maximum Safe Operating Area

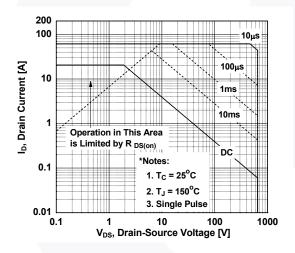


Figure 11. Eoss vs. Drain to Source Voltage

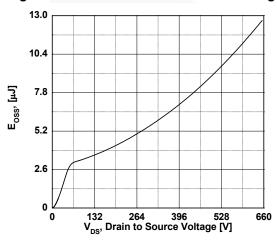


Figure 8. On-Resistance Variation vs. Temperature

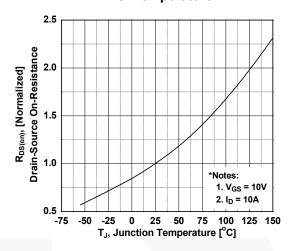
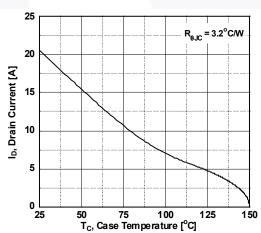
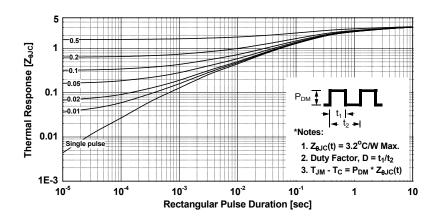


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



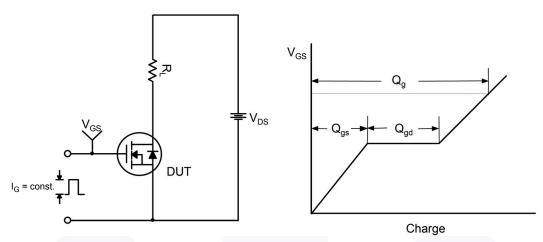


Figure 13. Gate Charge Test Circuit & Waveform

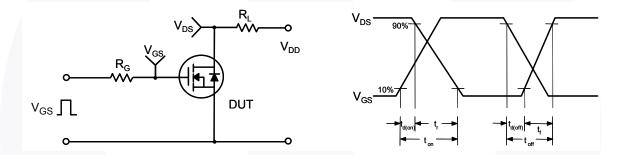


Figure 14. Resistive Switching Test Circuit & Waveforms

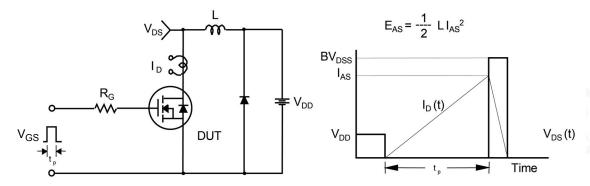


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

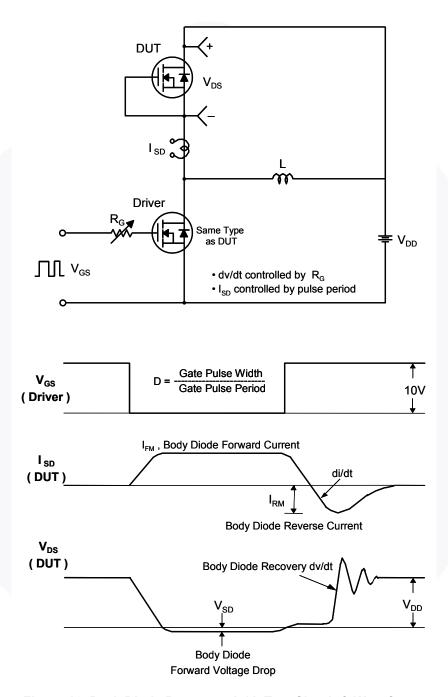


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

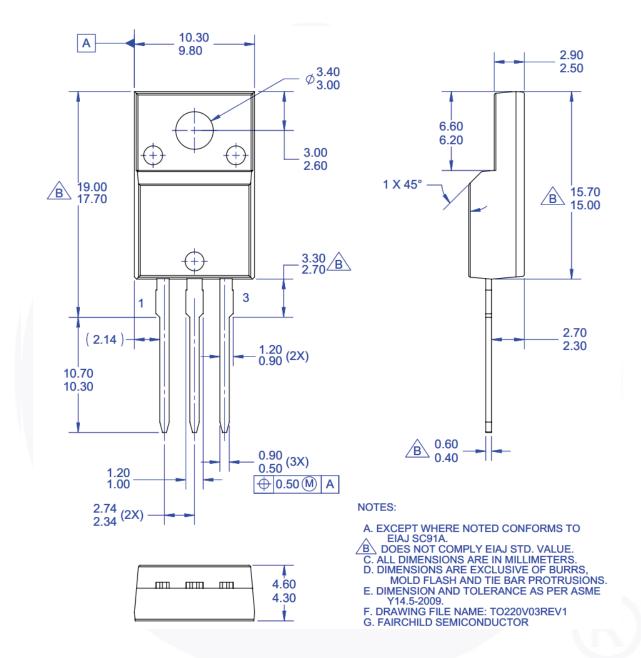


Figure 17. TO220, Molded, 3LD, Full Pack, EIAJ SC91, Takcheong

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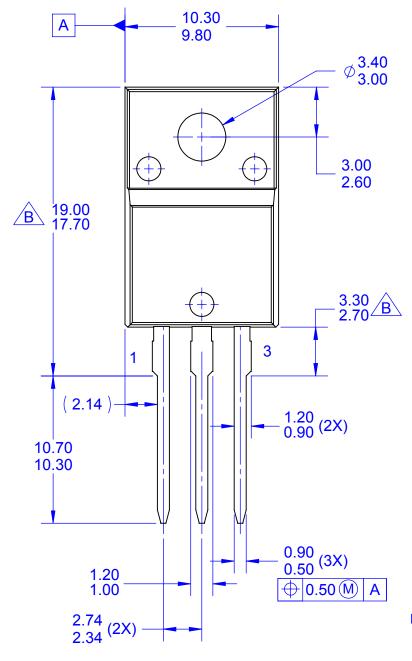
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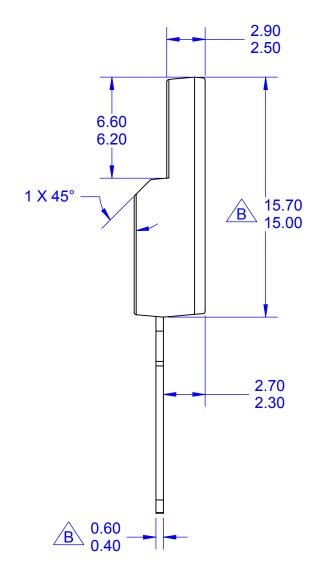
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