FD6288T&Q

3-PHASE BRIDGE DRIVER

Description

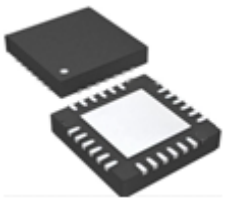
FD6288T&Q is an integrated three-span half-bridge gate driver IC designed for high voltage, high speed drive MOSFETs that operate up to +250V. The special HVIC technology can realize stable monolithic structure. Logic inputs are compatible with CMOS or LSTTL outputs, and the logic voltage can be down to 3.3V. The output driver has a high pulse current buffer stage, which aims to achieve a minimum driver impedance. Propagation delays are matched to simplify use in high frequency applications. Floating channel can be used to drive N-channel power MOSFET with high-end configuration, working voltage up to 250V.

Features

- Fully operational to +250V
- Gate driver supply range from 5V to 20V
- Independent Three half-bridge drivers
- 3.3V/5V logic input compatible
- Undervoltage lockout for all channels
- Cross-conduction prevention logic
- Internal set dead-time
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

Packages

TSSOP-20



QFN-24

Applications

- Motor drives
- DC-AC inverter drives

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air condition.

Definition	Symbol		Min~Max	Units
High side floating supply voltage	$V_{B1,2,3}$		-0.3～275	V
High side floating supply offset voltage	$V_{S1,2,3}$		$V_{B1,2,3}$-25～$V_{B1,2,3}$+0.3	V
High side floating output voltage	$V_{HO1,2,3}$		$V_{S1,2,3}$-0.3～$V_{B1,2,3}$+0.3	V
Low side and logic fixed supply voltage	V_{CC}		-0.3～25	V
Low side output voltage	$V_{LO1,2,3}$		-0.5～V_{CC}+0.3	V
Logic input voltage（HIN,LIN）	V_{IN}		-0.5～V_{CC}+0.3	V
Allowable offset supply voltage transient	dV_S/dt		≤50	V/ns
Package power dissipation @T_A≤25°C	P_D	20 lead TSSOP	≤1.25	W
		24 lead QFN	≤3.0	
Thermal resistance, junction to ambient	R_{thJA}	20 lead TSSOP	≤100	°C/W
		24 lead QFN	≤42	
Junction temperature	T_j		≤150	°C
Storage temperature	T_{stg}		-55～150	°C

Note1: In any case, power dissipation should not exceed P_D.

Note2: Voltages above the absolute maximum ratings may damage the chip.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15V differential.

Definition	Symbol	Min	Max	Units
High side floating supply voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+5	$V_{S1,2,3}$+20	V
High side floating supply offset voltage	$V_{S1,2,3}$	Note1	250	V
High side floating output voltage	$V_{HO1,2,3}$	V_S	$V_{B1,2,3}$	V
Low side and logic fixed supply voltage	V_{CC}	5	20	V
Low side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic input voltage（HIN,LIN）	V_{IN}	0	V_{CC}	V
Ambient temperature	T_A	-40	125	°C

Note1: Logic operational for V_S of (COM – 4V) to (COM + 600V). Logic state held for V_S of (COM – 4V) to (COM –V_{BS}).

Note2: The long-term operation of the chip outside the recommended conditions may affect its reliability. It is not recommended to work in an environment that exceeds the recommended conditions.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) =15V and TA =25°C unless otherwise specified. All the parameters are referenced to COM.

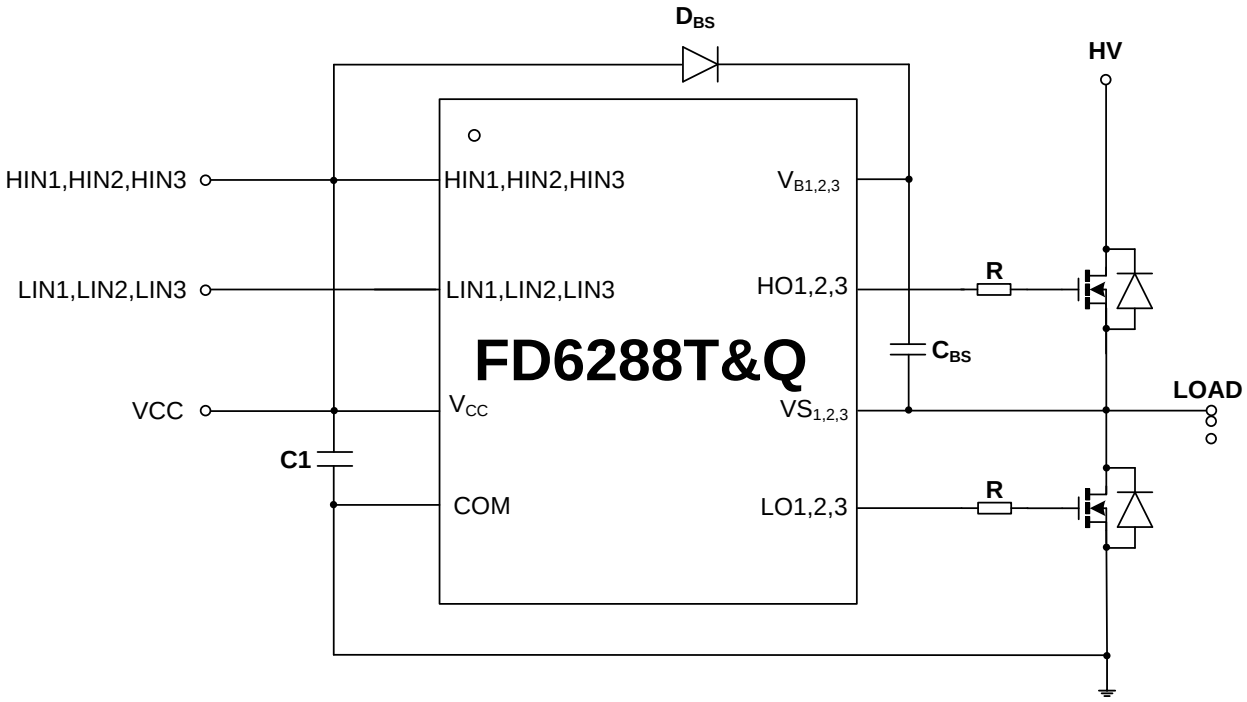
Definition	Symbol	Test conditions	Min.	Typ.	Max.	Units
Logic "1" input voltage	V_{IH}		2.7	-	-	V
Logic "0" input voltage	V_{IL}		-	-	0.8	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O=100mA	-	0.6	0.9	
low level output voltage, V_O	V_{OL}		-	0.3	0.45	
Offset supply leakage current	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=250V	-	0.1	5.0	uA
Quiescent V_{BS} supply current	I_{QBS}	V_{IN} =0V or 5V	-	180	270	
Quiescent V_{CC} supply current	I_{QCC}		-	330	500	
Logic "1" input bias current	I_{IN+}	V_{IN}=5V	-	25	40	
Logic "0" input bias current	I_{IN-}	V_{IN}=0V	-	-	1	
V_{CC} and V_{BS} supply undervoltage positive going threshold	V_{CCUV+} V_{BSUV+}		4.2	4.6	5.0	V
V_{CC} and V_{BS} supply undervoltage negative going threshold	V_{CCUV-} V_{BSUV-}		3.9	4.3	4.7	
Output high short circuit pulsed current	I_{O+}	V_O=0V,PW≤10us	1.1	1.5	1.9	A
Output low short circuit pulsed current	I_{O-}	V_O=15V,PW≤10us	1.3	1.8	2.3	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) =15V, C_L=1000pF, and TA =25°C, unless otherwise specified.

Definition	Symbol	Test conditions	Min.	Typ.	Max.	Units
Turn on propagation delay	ton	$V_{S1,2,3}$=0V	-	300	450	ns
Turn off propagation delay	toff	$V_{S1,2,3}$=250V	-	100	160	
Delay matching, HS & LS turn on/off	MT		-	-	30	
Turn on rise time	tr		-	12	25	
Turn off fall time	tf		-	12	25	
Deadtime , LS turn-off to HS turn-on & HS turn-off to LS turn-on	DT		100	200	300	

Typical Connection



C1： Power filter capacitor, according to the circuit can choose 1μF ~ 10μF, as close to the chip pin as possible.

R： Gate drive resistor, and the resistance depends on the device being driven.

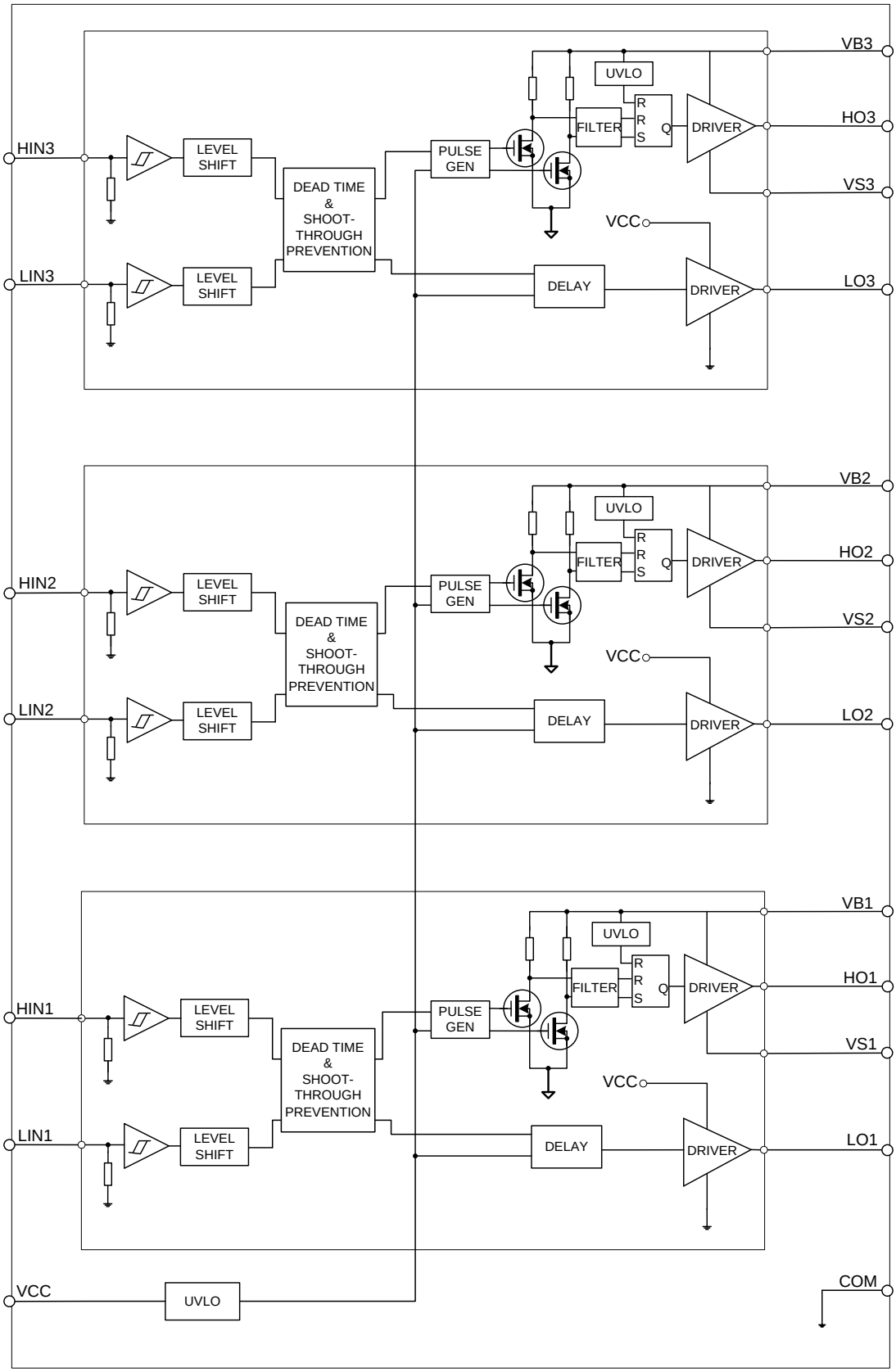
D_{BS}：Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

C_{BS}：Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose0. 22μF ~ 10μF. The capacitor should be as close as possible to the chip pin.

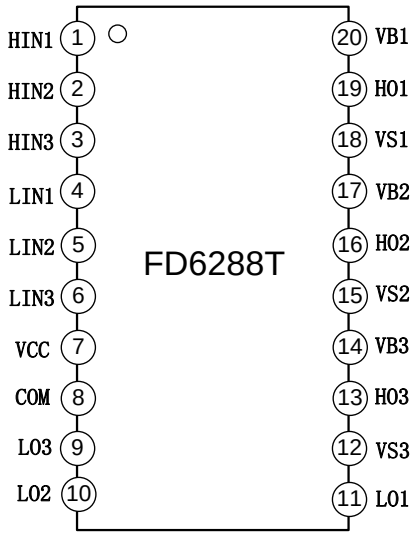
Note:

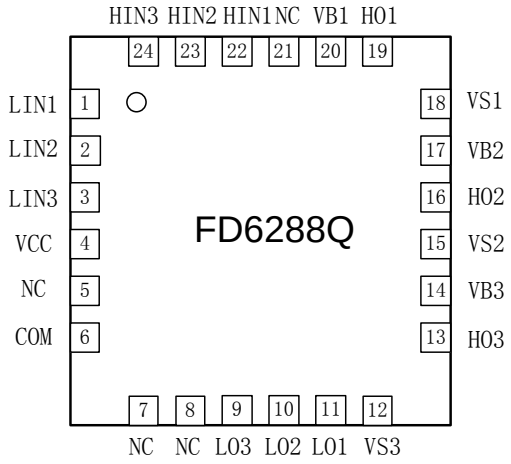
The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

Functional Block Diagram



Lead Assignments

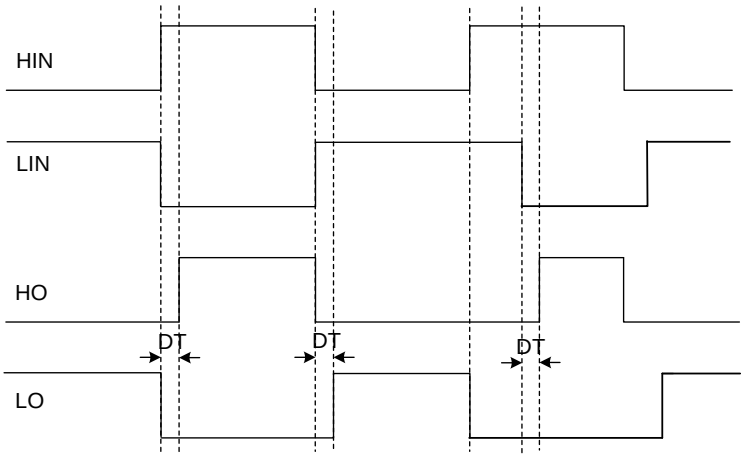




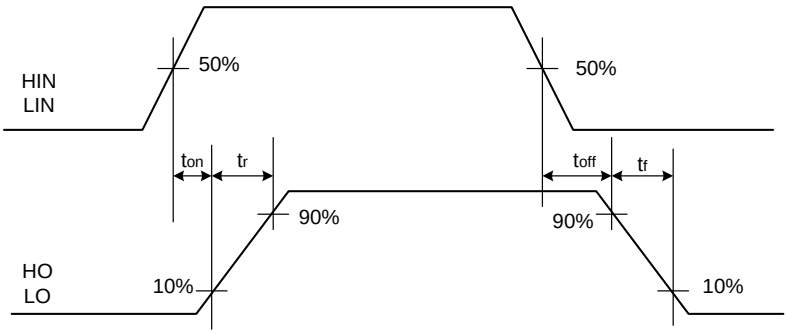
Lead definitions

Symbol	Description
V_{CC}	Low side and logic fixed supply
HIN1,2,3	Logic input for high side gate driver output(HO),in phase
LIN1,2,3	Logic input for low side gate driver output(LO),in phase
COM	Low side return
LO1,2,3	Low side gate drive output
$V_{S1,2,3}$	High side floating supply return
HO1,2,3	High side gate drive output
$V_{B1,2,3}$	High side floating supply

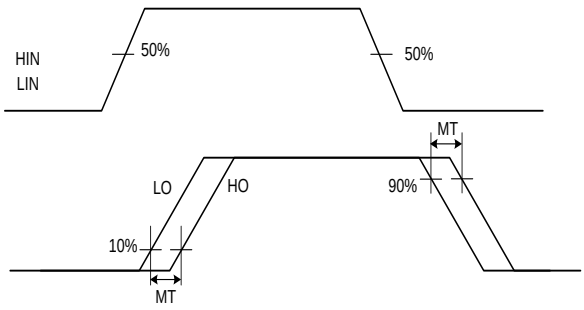
Input/Output Timing Diagram

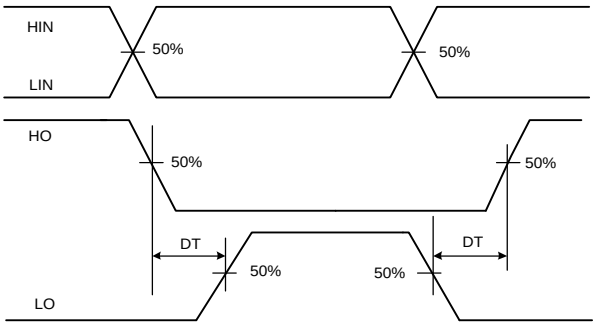


Switching Time Waveform Definitions



Delay Matching Waveform Definitions and Deadtime Waveform Definitions





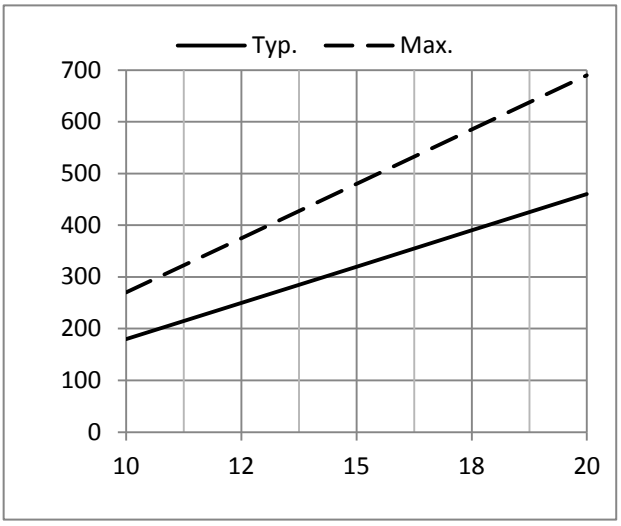


Figure 1A V_{CC} Supply Current vs Supply Voltage

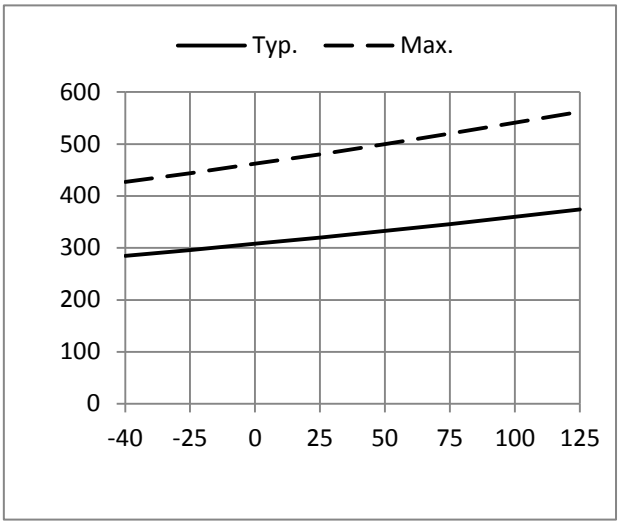


Figure 1B V_{CC} Supply Current vs Temperature

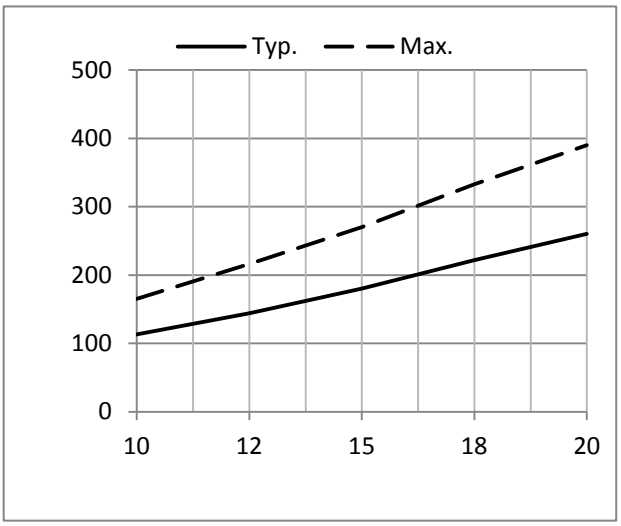


Figure 2A V_{BS} Supply Current vs Supply Voltage

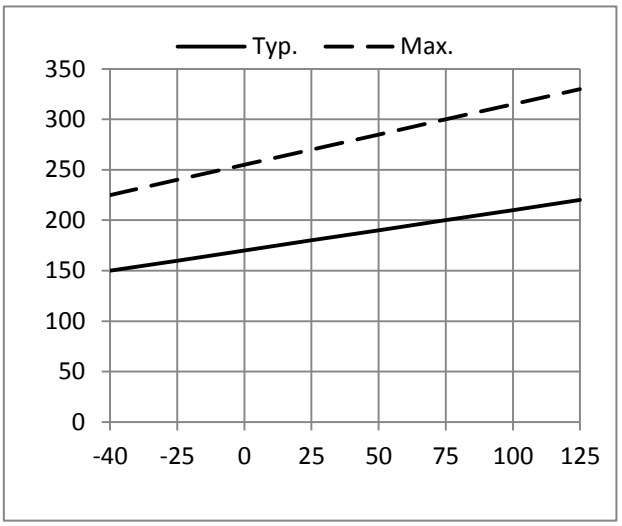


Figure 2B V_{BS} Supply Current vs Temperature

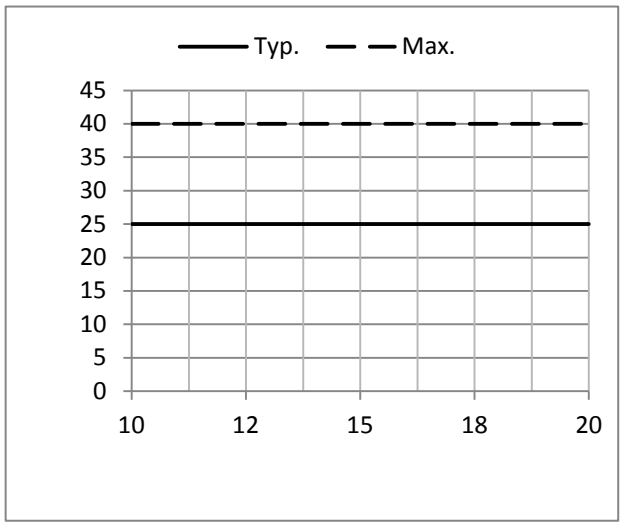


Figure 3A Logic “1” Input Current vs Supply Voltage

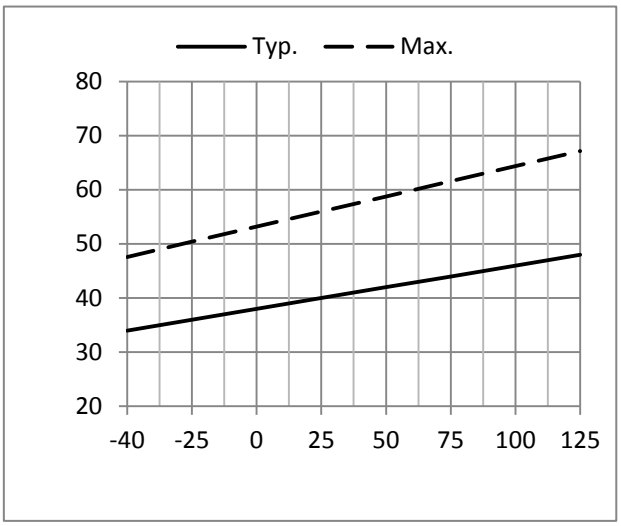


Figure 3B Logic “1” Input Current vs Temperature

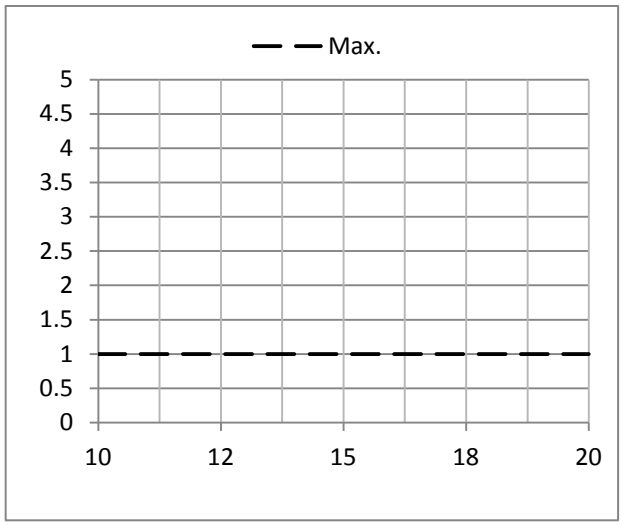


Figure 4A Logic “0” Input Current vs Supply Voltage

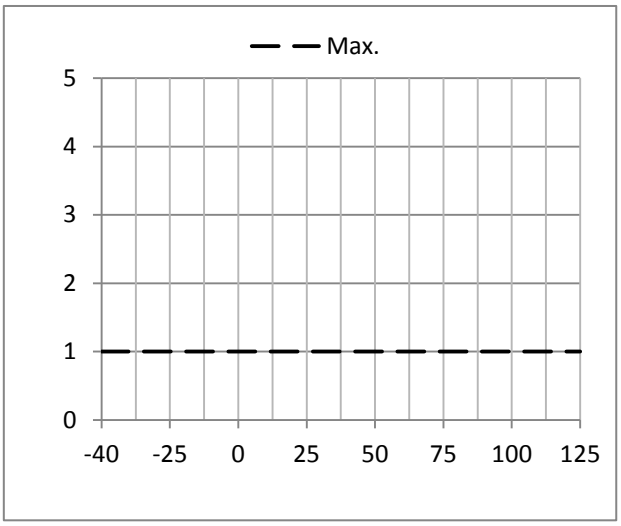


Figure 4B Logic “0” Input Current vs Temperature

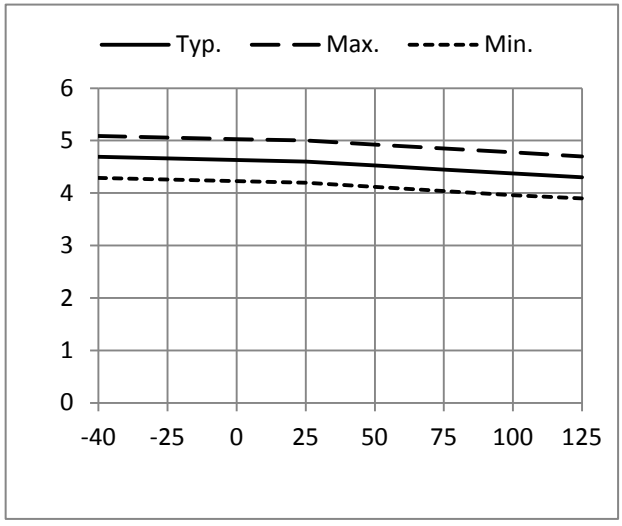


Figure 5A V_{CC} Undervoltage Threshold(+) vs Temperature

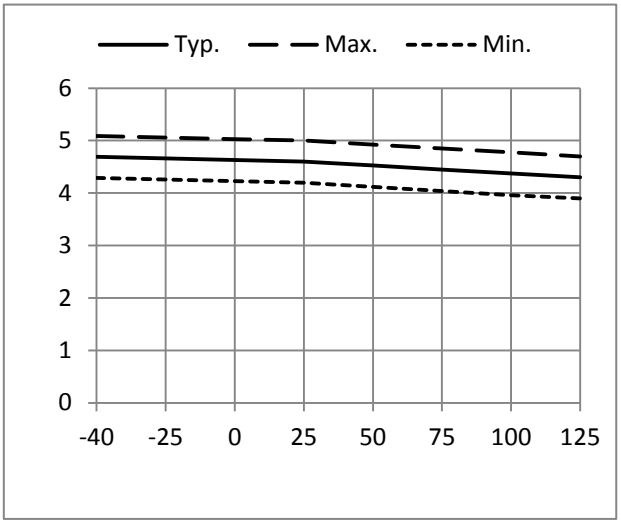


Figure 5B V_{CC} Undervoltage Threshold(-) vs Temperature

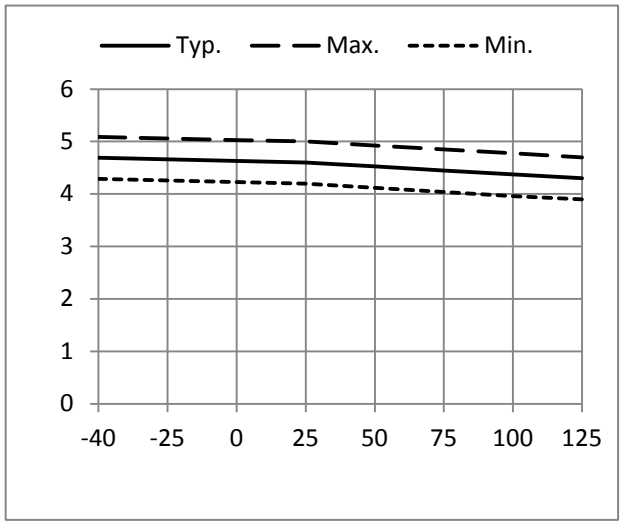


Figure 6A V_{BS} Undervoltage Threshold(+) vs Temperature

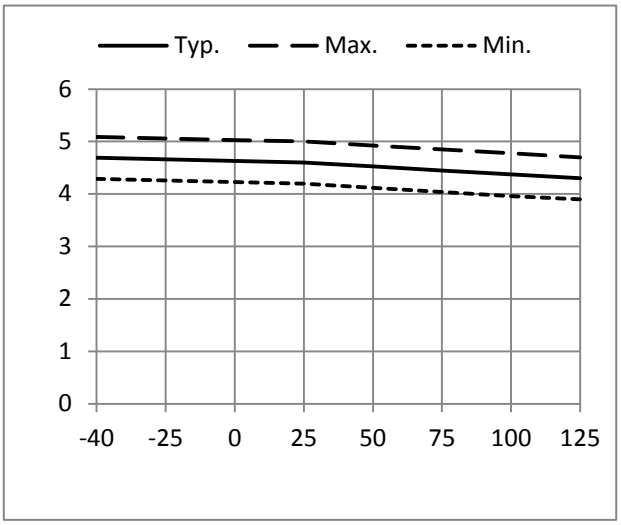


Figure 6B V_{BS} Undervoltage Threshold(-) vs Temperature

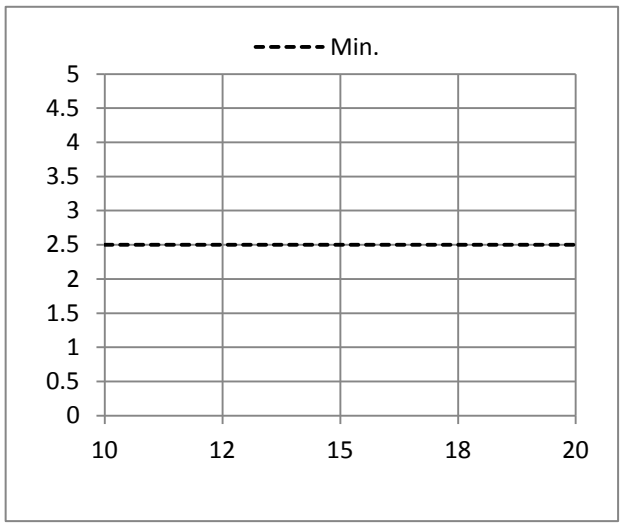


Figure 7A Logic “1” Input Voltage vs Supply Voltage

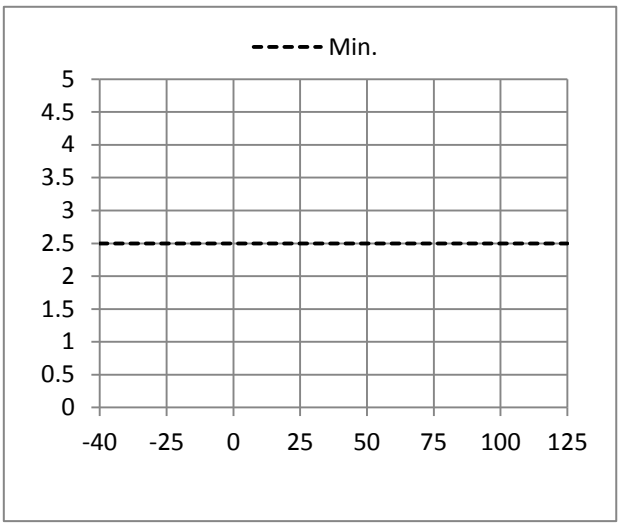


Figure 7B Logic “1” Input Voltage vs Temperature

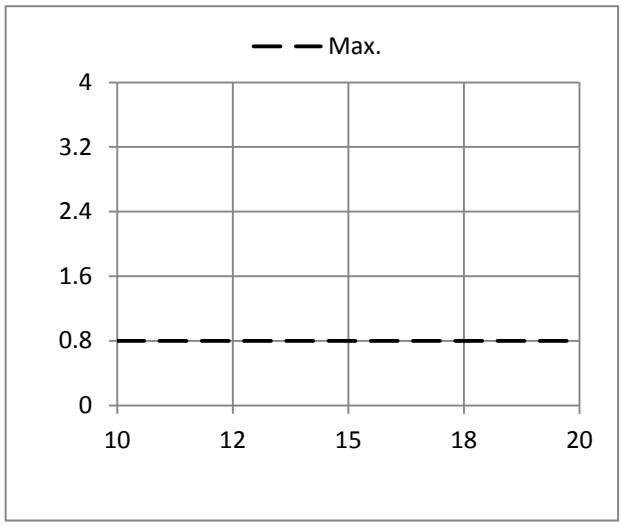


Figure 8A Logic “0” Input Voltage vs Supply Voltage

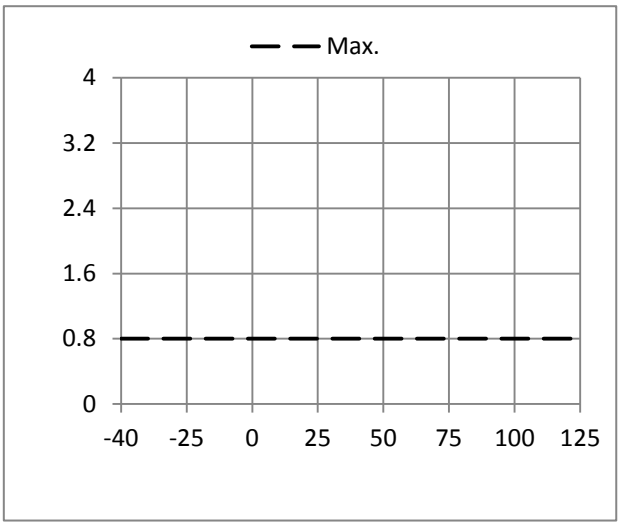


Figure 8B Logic “0” Input Voltage vs Temperature

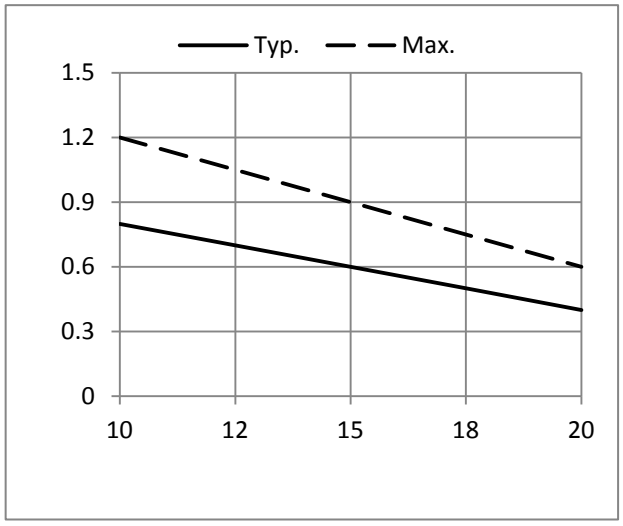


Figure 9A High Level Output Voltage vs Supply Voltage

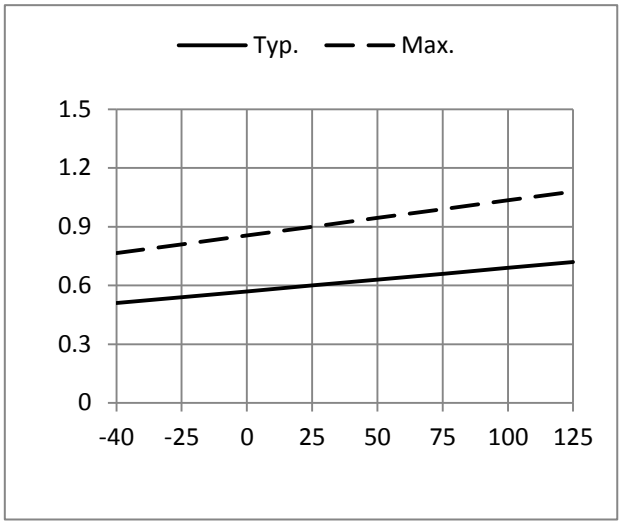


Figure 9B High Level Output Voltage vs Temperature

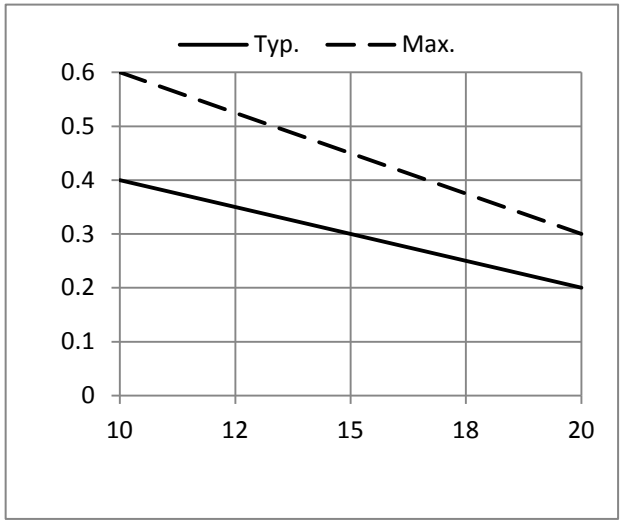


Figure 10A Low Level Output Voltage vs Supply Voltage

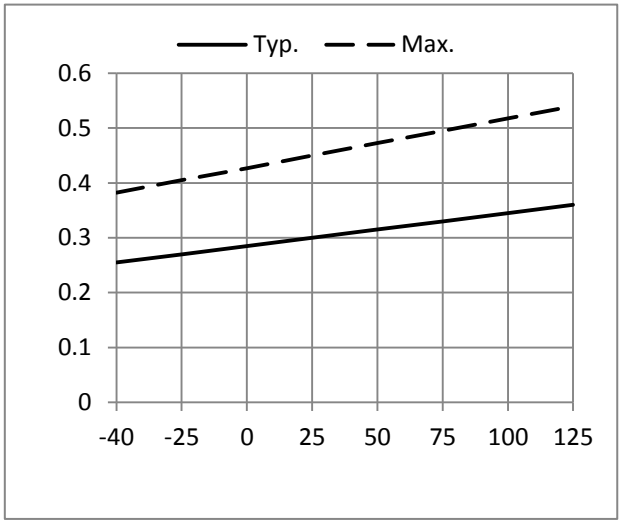


Figure 10B Low Level Output Voltage vs Temperature

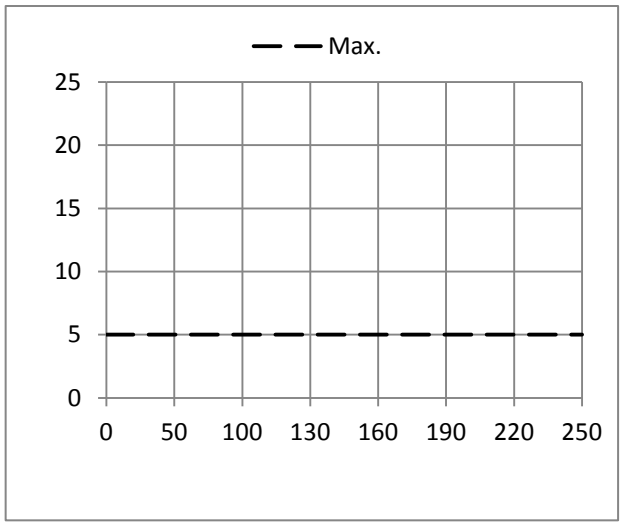


Figure 11A Offset Supply Current vs Voltage

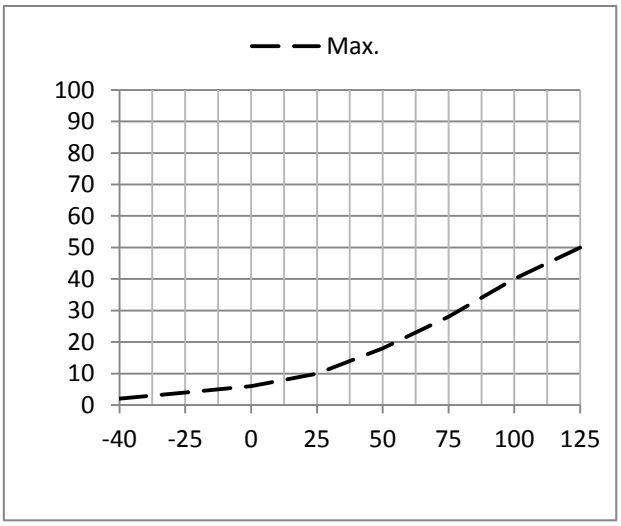


Figure 11B Offset Supply Current vs Temperature

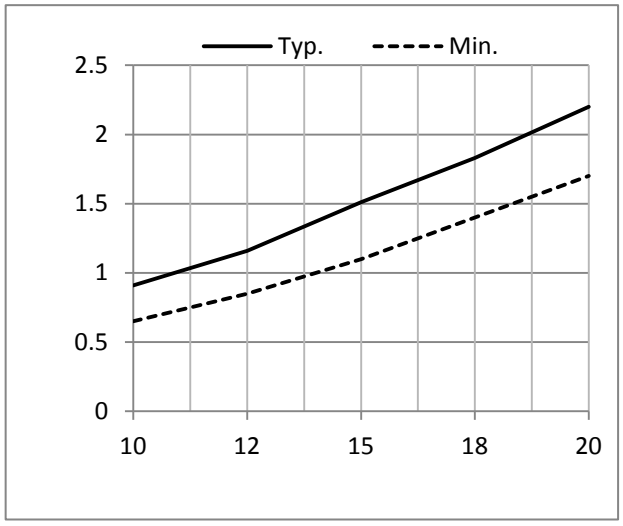


Figure 12A Output Source Current vs Supply Voltage

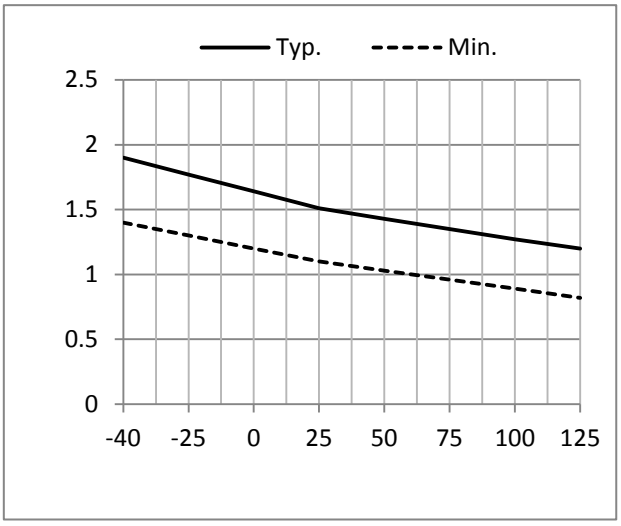


Figure 12B Output Source Current vs Temperature

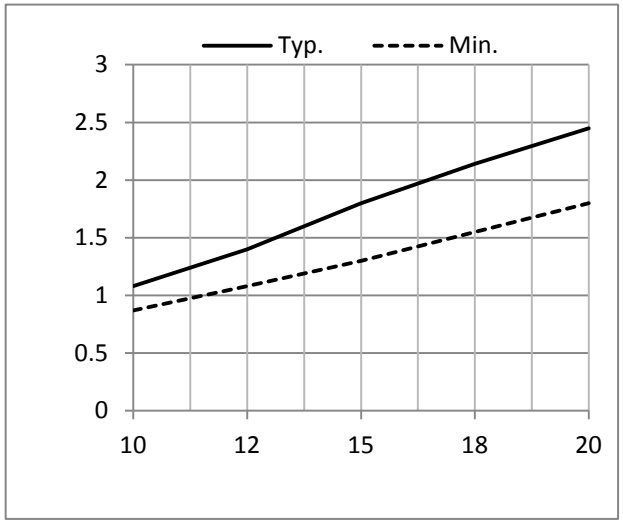


Figure 13A Output Sink Current vs Supply Voltage

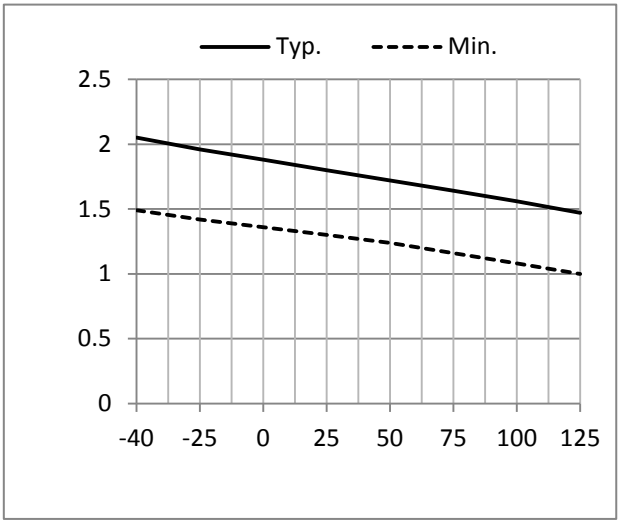


Figure 13B Output Sink Current vs Temperature

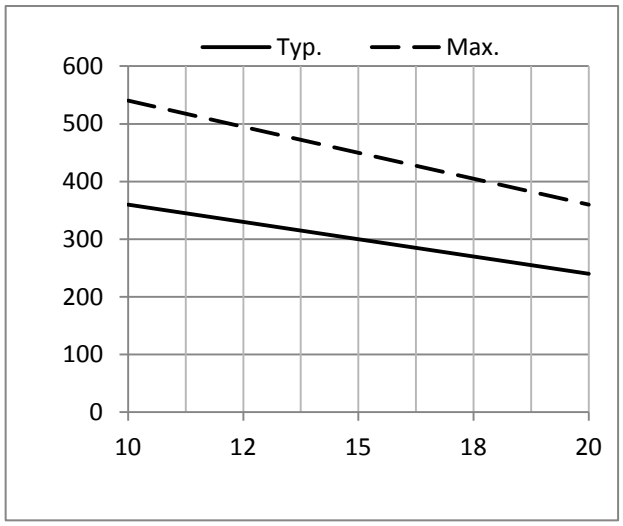


Figure 14A Turn On Time vs Supply Voltage

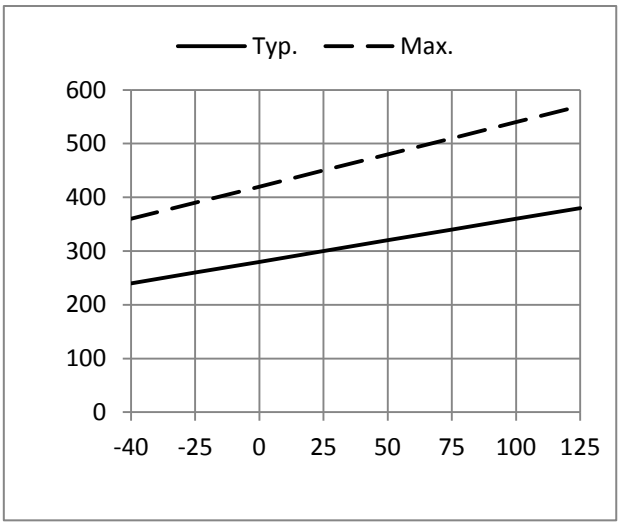


Figure 14B Turn On Time vs Temperature

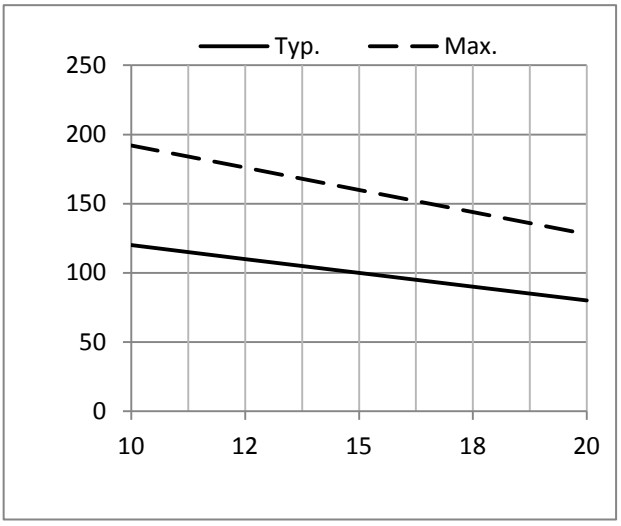


Figure 15A Turn Off Time vs Supply Voltage

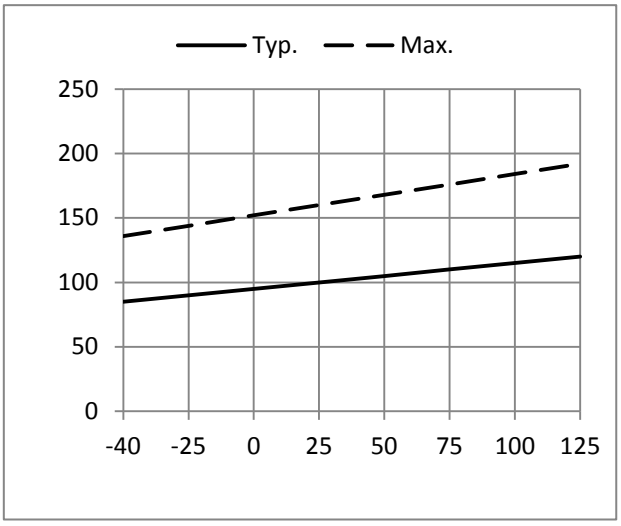


Figure 15B Turn Off Time vs Temperature

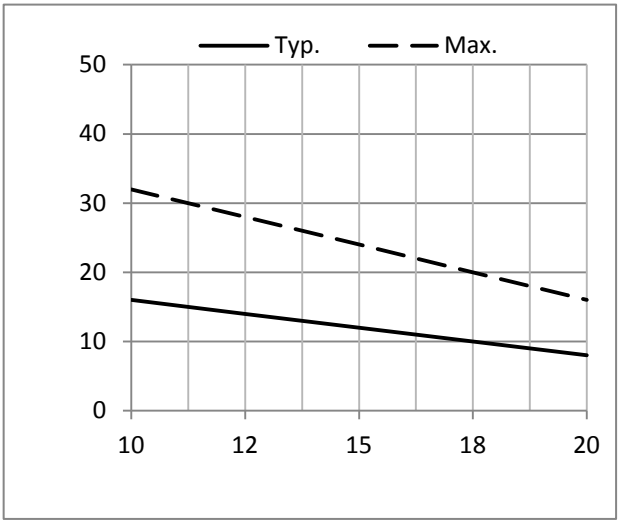


Figure16A Turn On Rise Time vs Supply Voltage

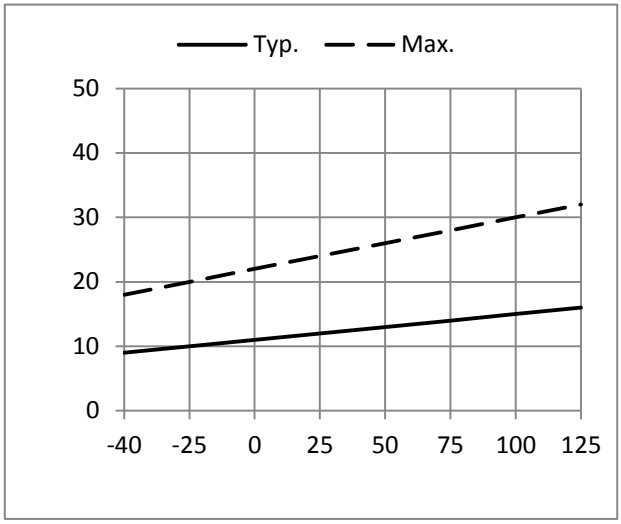


Figure 16B Turn On Rise Time vs Temperature

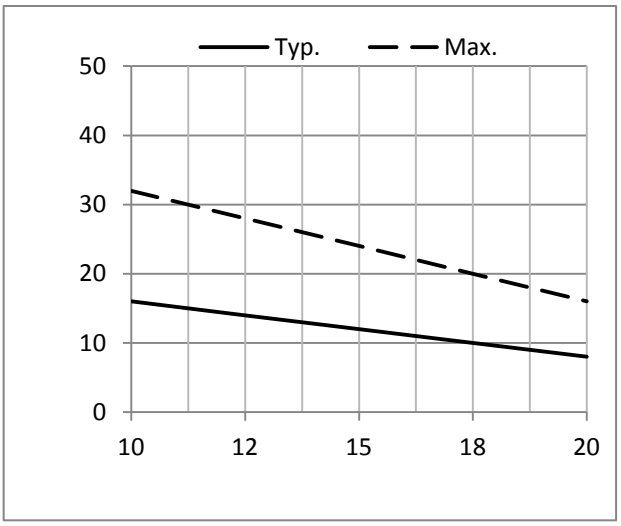


Figure 17A Turn Off Fall Time vs Supply Voltage

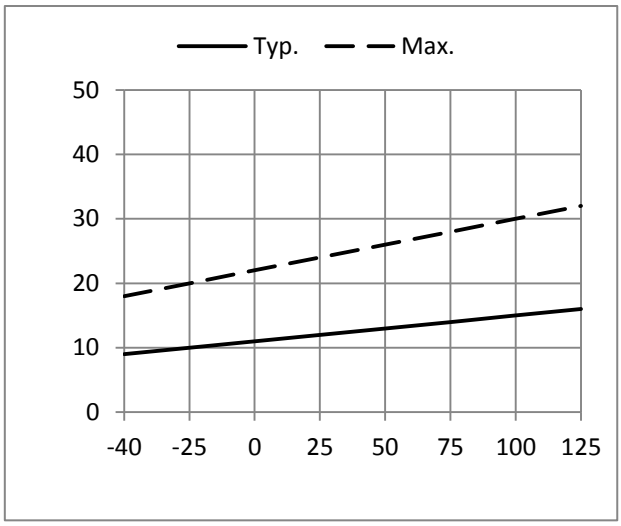


Figure 17B Turn Off Fall Time vs Temperature

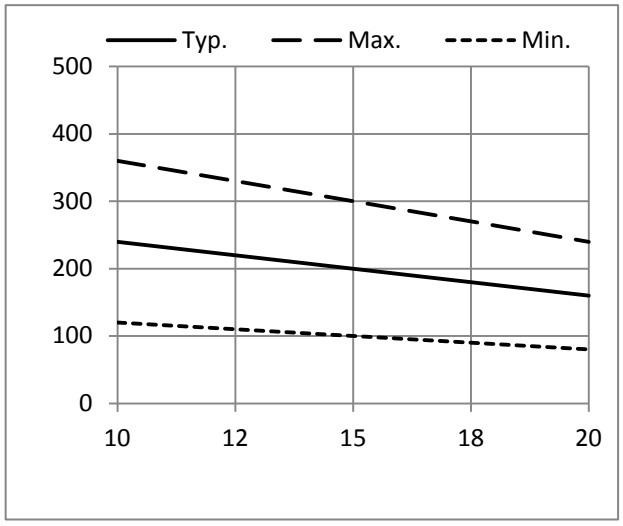


Figure 18A Dead Time vs Supply Voltage

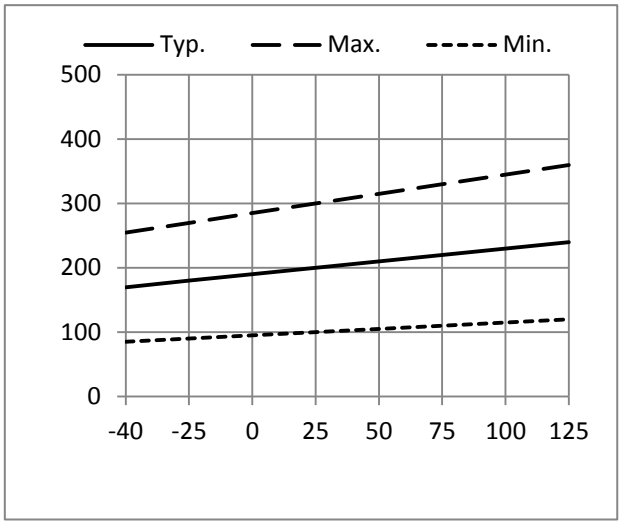


Figure 18B Deadtime Time vs Temperature

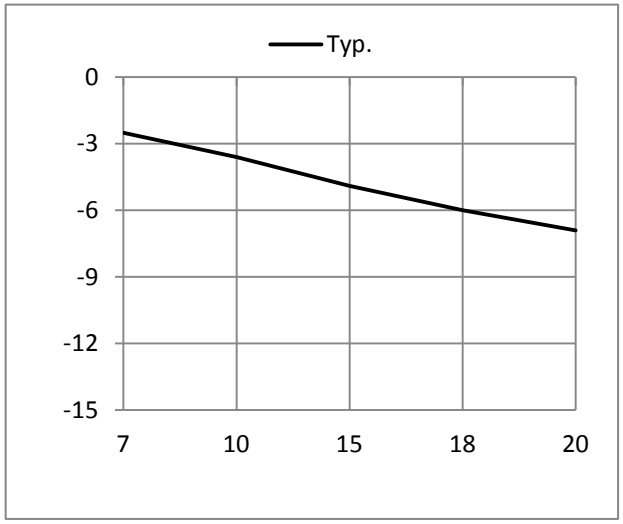


Figure 19A V_S Negative offset vs Supply Voltage

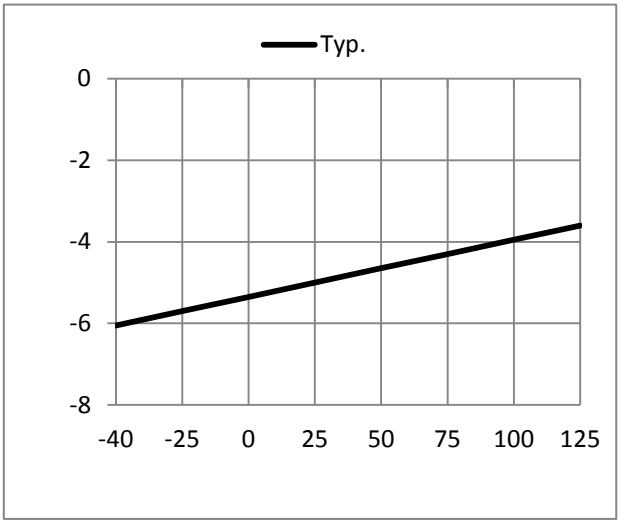
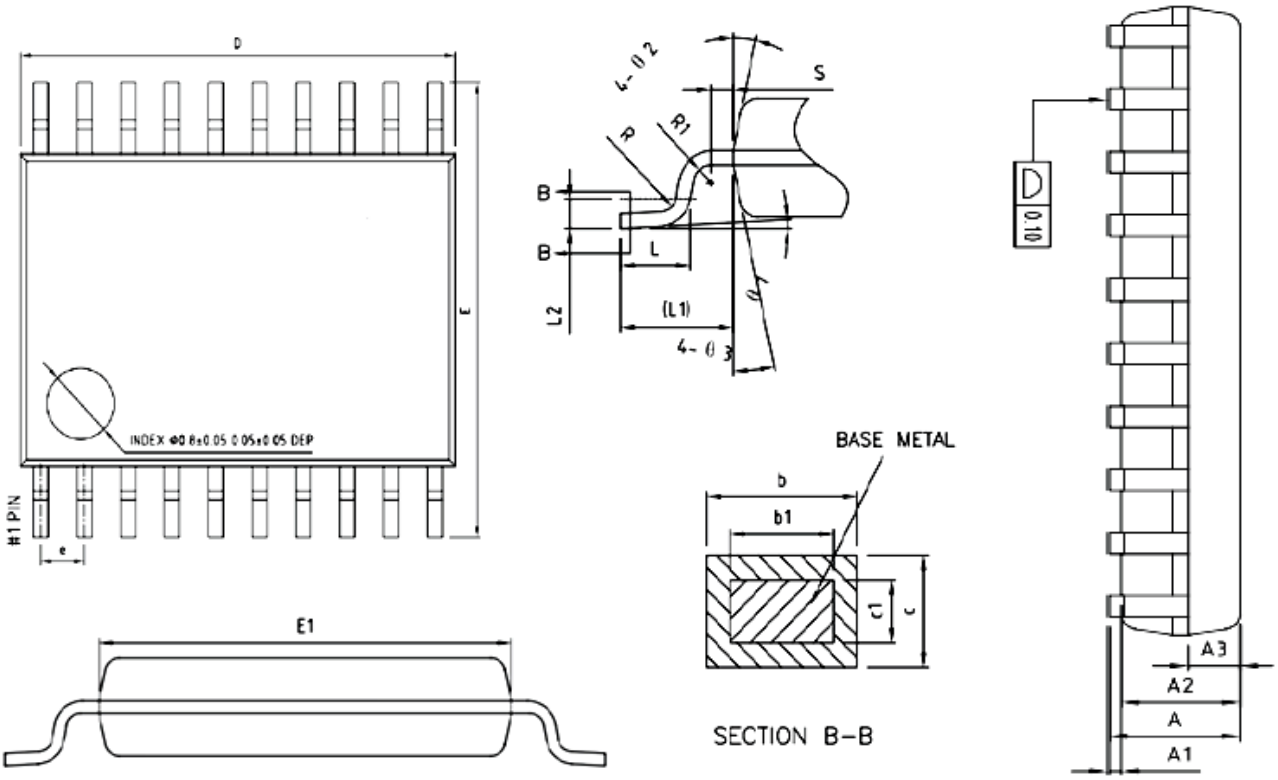


Figure 19B V_S Negative offset vs Temperature

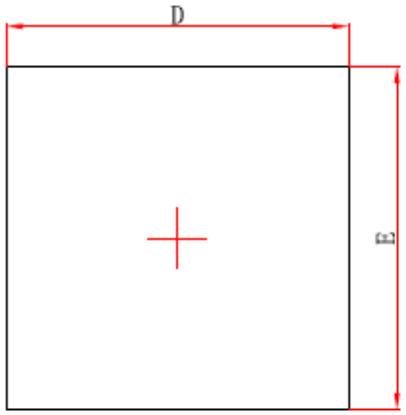
Case outlines



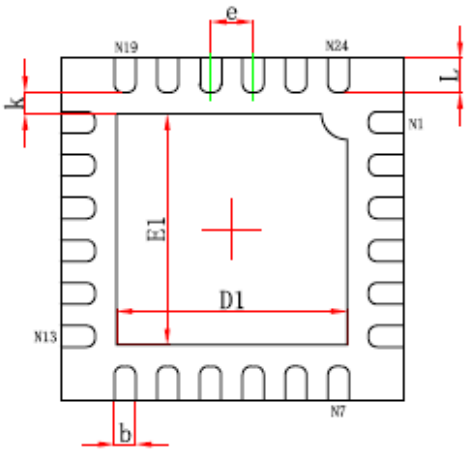
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

20 Lead TSSOP

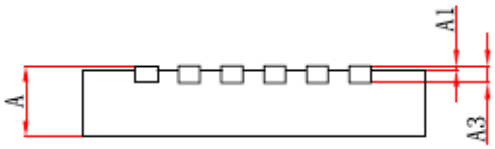
Part Number	Package Type	Marking ID	Package Method	Quantity
FD6288T	TSSOP20	FD6288T	Tape&Reel	3000



Top View



Bottom View



Side View

Symbol	Dimensions with mm		Dimensions with inch	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.0031/0.0035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
K	0.200MN		0.008MN	
B	0.200	0.300	0.008	0.012
E	0.500TYP		0.020TYP	
L	0.324	0.476	0.013	0.019

24 Lead QFN

Part Number	Package Type	Marking ID	Package Method	Quantity
FD6288Q	QFN24	FD6288Q	Tape&Reel	3000

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Fortior Technology (Shenzhen) Co.,Ltd.

Room203, 2/F, Building No.11,Keji Central Road2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com

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