



16 Bit Constant Current LED Driver

Product Description

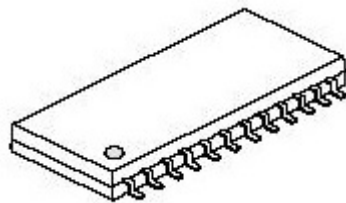
FD9802 is a 16-bit constant current driver for LED displays. This product is designed by Shanghai Fengxin Microelectronics Co., Ltd. The constant current can be set between 5mA to 90mA by an external resistor.

FD9802C has the same function with MBI5026GF and FD9802D has the same function with MBI5026GP. FD9802 can be directly used on the existing PCB, no need to design new PCB. FD9802's performance price ratio is higher; the manufacturers of LED display can save cost by using FD9802.

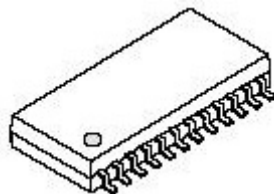
Model

FD9802C (Package SSOP24-1.0)

FD9802D (Package SSOP24-0.635)



FD9802C:SSOP24-300-1.0



FD9802D:SSOP24-150-0.635

Features

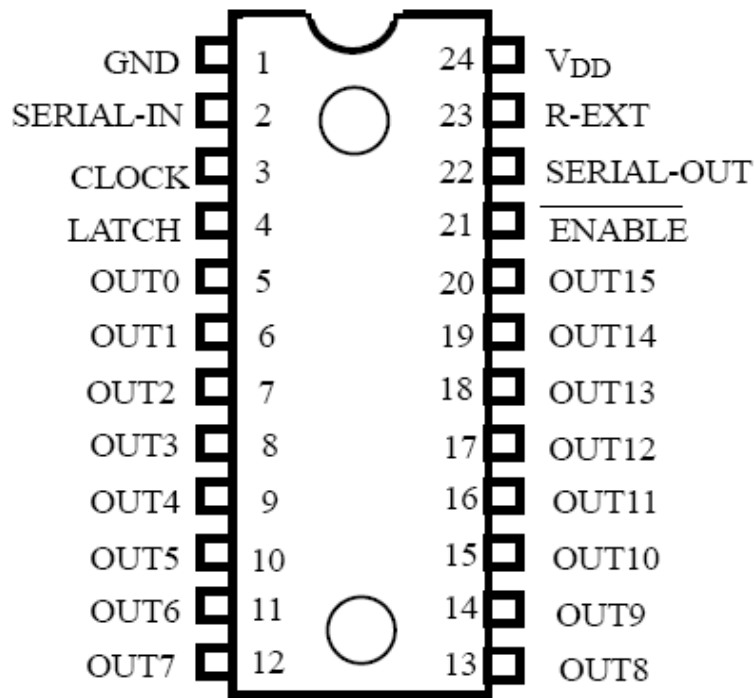
- 16 constant-current output channels
- Constant output current invariant to load voltage change
- Output current adjusted through an external resistor
- Constant output current range: 5-90mA
- Excellent output current accuracy:
 - Between channels: $<\pm 3\%$
 - Between ICs: $<\pm 4\%$
- 25MHZ clock frequency
- Input compatible 5V CMOS
- 5V supply voltage



“Bb-free & Green” Package

Compatible with TI's TLC5926/7, TOSHIBA's TB62726 and Macroblock's MBI5026/4/0.

Pin Assignment



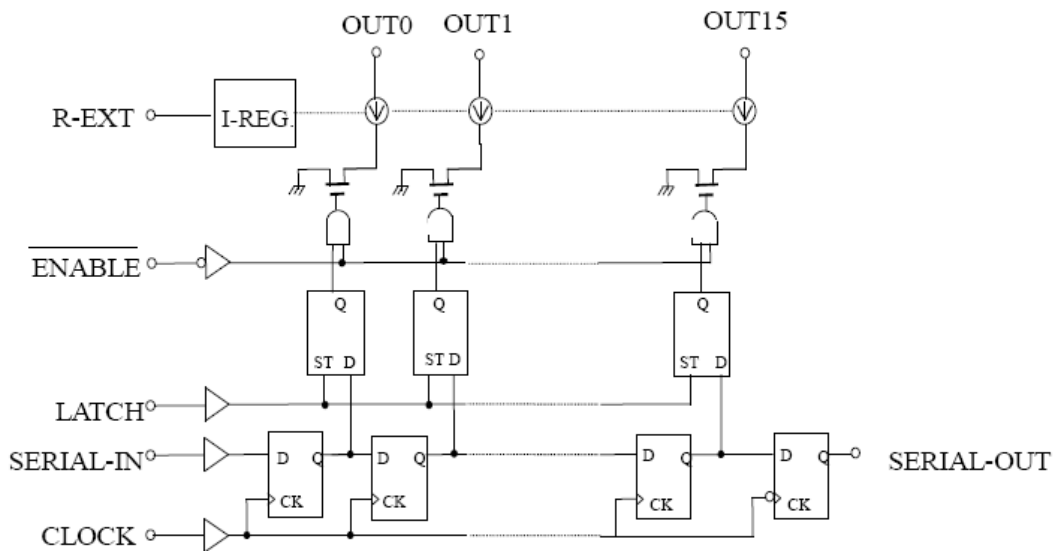
Pin Description

Pin Number	Pin Name	Function
1	GND	Ground terminal.
2	SERIAL-IN	Terminal of serial-data input to the shift register.
3	CLOCK	Clock input terminal for data shift on rising edge.
4	LATCH	Data strobe input terminal. Serial data is transferred to the output latch when LATCH is high. The data is latched when LATCH goes low.
5~20	OUT 0~15	Constant current output terminals.
21	ENABLE	Output enable terminal. All the output terminals are turned off when ENABLE is high; all the output terminals are turned on when ENABLE is low.



22	SERIAL-OUT	Serial-data output terminal, to the next SERIAL-IN.
23	R-EXT	Current setting terminal. Connected with an external resistor to adjust output current.
24	V _{DD}	Supply voltage terminal.

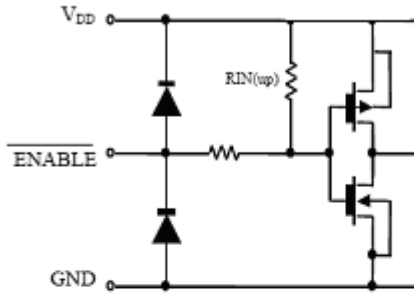
Block Diagram



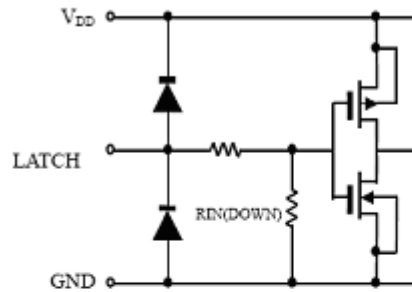
Equivalent Circuit of Inputs and Outputs



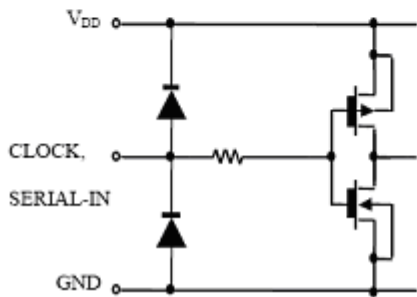
1. ENABLE



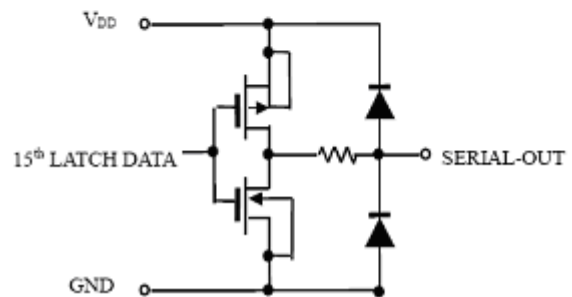
2. LATCH



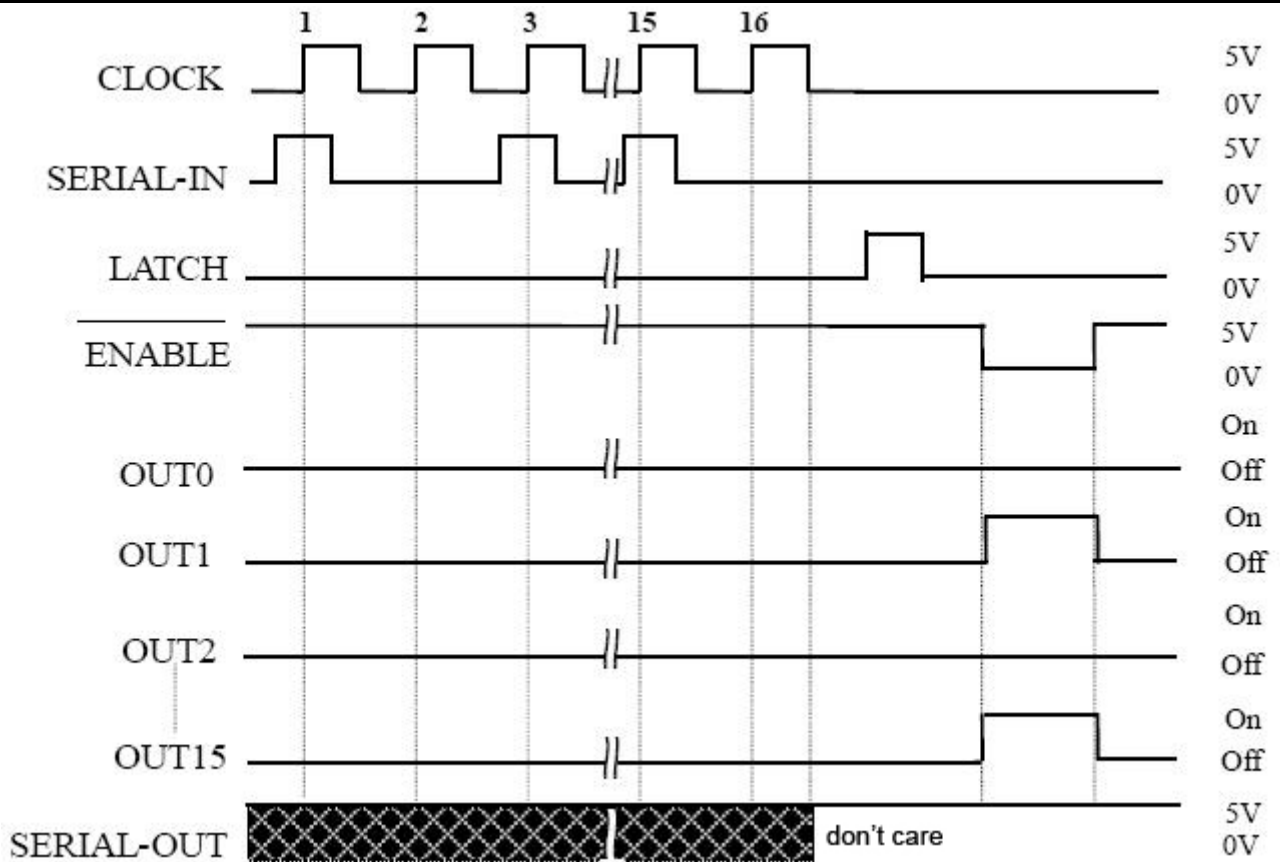
3. CLOCK, SERIAL-IN



4. SERIAL-OUT



Timing Diagram



Note: The latches circuit holds data when the LATCH terminal is Low. When the LATCH terminal is at High level, latch circuit doesn't hold the data, it passes from the input to the output. When the ENABLE terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF. When the ENABLE terminal is at High level, it switches off all the data on the output terminal.

Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ... OUT7 ... OUT15	SERIAL-OUT
↑	H	L	D_n	$\overline{D_n} \dots \overline{D_{n-7}} \dots \overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Note: OUT0 to OUT15 = ON when $D_n = H$; OUT0 to OUT15 = OFF when $D_n = L$.



Maximum Rating

Parameter	Symbol	Value	Unit
Supply voltage	V _{DD}	0~7.0	V
Input voltage	V _{IN}	-0.4~V _{DD} +0.4	V
Output voltage on OUTn	V _{OUT}	-0.5~+17.0	V
Output current on OUTn	I _{OUT}	+90	mA
Clock frequency	f _{CLK}	25	MHz
GND terminal current	I _{GND}	1440	mA
Power Dissipation	P _D	1.00(ON PCB, Ta=25°C)	W
Thermal Resistance	R _{th(j-a)}	120(ON PCB)	°C/W
Storage temperature range	T _{stg}	-55~+150	°C
Operating temperature range	T _{opr}	-40~+85	°C

Recommended Operating Conditions

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	-	4.5	5.0	5.5	V
Input voltage	V _{IH}	-	0.7V _{DD}	-	V _{DD} +0.3	V
	V _{IL}	-	-0.3	-	0.3V _{DD}	
Output voltage on OUTn	V _{OUT}	-	-	-	15.0	V
Output current	I _{OUT}	OUTn	5	-	45	mA
	I _{OH}	SERLAL-OUT	-	-3.7	-	
	I _{OL}	SERLAL-OUT	-	-4.0	-	
LATCH pulse width	T _w LAT	V _{DD} =4.5~5V	100	-	-	ns
CLOCK pulse width	T _w CLK		50	-	-	ns
Setup time for DATA	T _{setup(D)}		60	-	-	ns
Holdtime for DATA	T _{hold(D)}		20	-	-	ns
Hold time for LATCH	T _{setup(L)}		100	-	-	ns
Clock frequency	f _{CLK}	Cascade Operation	-	15	20	MHz
Power Dissipation	P _D	Ta=85 °C	-	-	0.5	W



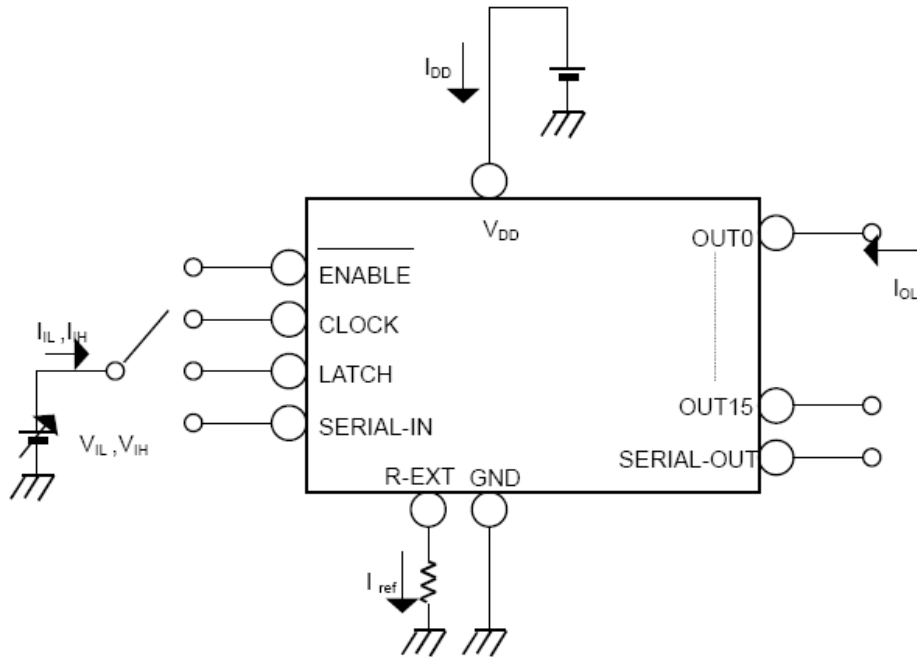
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	-	0.7VDD	-	VDD	V
Low level input voltage	V_{IL}	-	GND	-	0.3VDD	
Output leakage current	I_{OH}	$V_{OH}=9.5V$	-	-	1.0	μA
Output Voltage (S-OUT)	V_{OL}	$I_{OL}=1.0mA$	-	-	0.4	V
	V_{OH}	$I_{OH}=-1.0mA$	4.6	-	-	
Output Current (Between channels)	I_{OL1}	$V_{OUT}=0.7\pm 0.25V$ $R_{EXT}=910\Omega$	-	-	± 3	%
	I_{OL2}	$V_{OUT}=0.7\pm 0.25V$ $R_{EXT}=360\Omega$	-	-	± 3	
Output Current (Between Ics)	I_{OL3}	$V_{OUT}=0.7V$ $R_{EXT}=910\Omega$	-	-	± 4	
	I_{OL4}	$V_{OUT}=0.7V$ $R_{EXT}=360\Omega$	-	-	± 4	
Output Current vs. Output Voltage Regulation	$\%/VDD$	$R_{EXT}=360\Omega$, $T_a=-40\sim 85\text{ }^{\circ}C$	-	1.5	5.0	$\%/V$
Pull-up Resistor□	$R_{IN}(\text{pull up})$	-	150	300	600	$k\Omega$
Pull-down Resistor	$R_{IN}(\text{pull down})$	-	100	200	400	$k\Omega$
Supply Current (OFF)	$I_{DD}(\text{off})1$	$R_{EXT}=\text{OPEN}, \text{OUT}0\sim 7=\text{off}$	-	0.3	0.6	mA
	$I_{DD}(\text{off})2$	$R_{EXT}=470\Omega, \text{OUT}0\sim 7=\text{off}$	3.9	5.5	7.7	
	$I_{DD}(\text{off})3$	$R_{EXT}=250\Omega, \text{OUT}0\sim 7=\text{off}$	7.2	10.1	14.1	
	$I_{DD}(\text{on})1$	$R_{EXT}=470\Omega, \text{OUT}0\sim 7=\text{on}$	3.9	5.5	7.7	



Supply Current (ON)	$I_{DD(on)2}$	REXT=250Ω, OUT0~7=on	7.2	10.1	14.1	
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Test Circuit for Electrical Characteristics



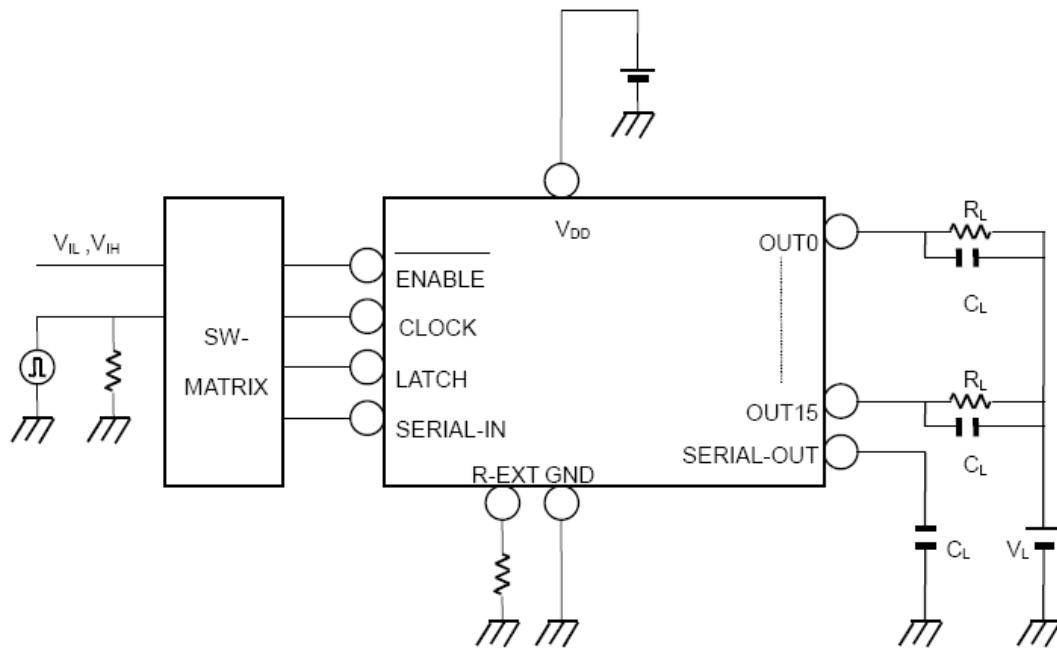
Switching Characteristics

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
propagation delay time ("L" to "H")	CLK-OUTn	tpLH	VDD=5.0V VCE=0.4V VIH= VDD VIL=GND REXT=470Ω	-	120	150	ns
	LATCH - OUTn			-	120	150	
	ENABLE - OUTn			-	120	150	
	CLK-S-OUT			-	30	70	
propagation delay time ("H" to "L")	CLK-OUTn	tpHL	VL=3.0V RL=1.0K CL=10.5pF	-	70	100	ns
	LATCH - OUTn			-	70	100	
	ENABLE - OUTn			-	70	100	
	CLK-S-OUT			-	30	70	



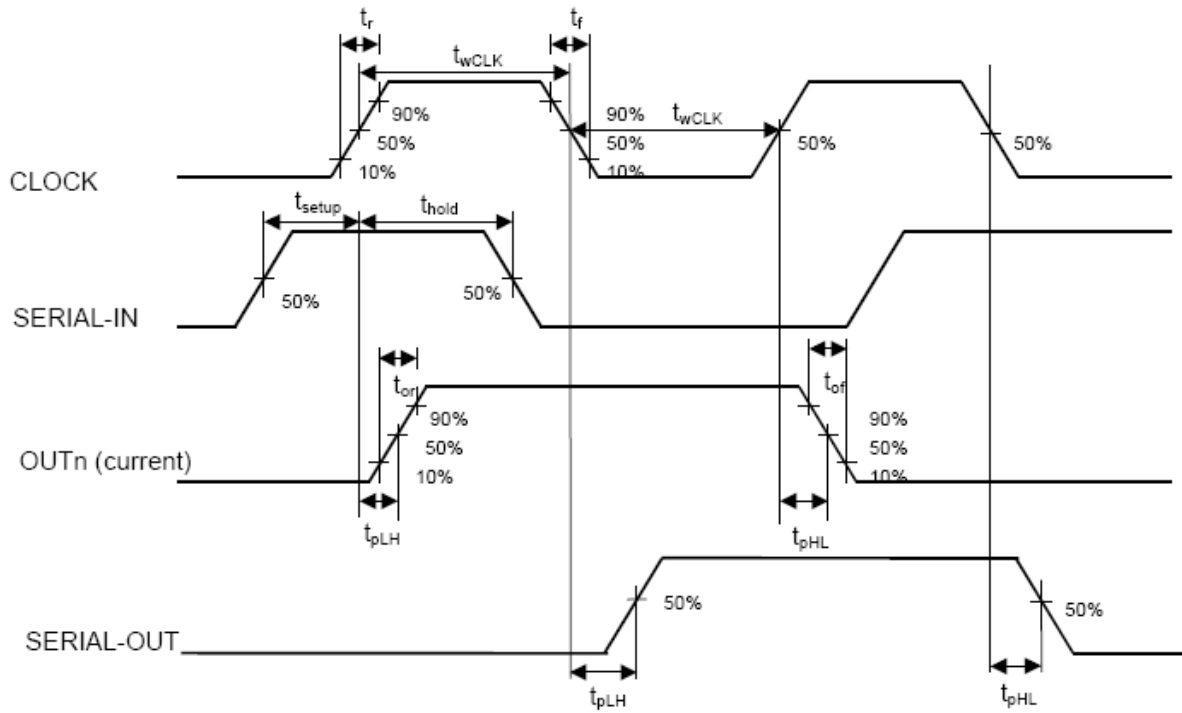
Output current rise time	t_{or}	-	100	200	ns
Output current fall time	t_{of}	-	60	120	ns

Test Circuit for Switching Characteristics

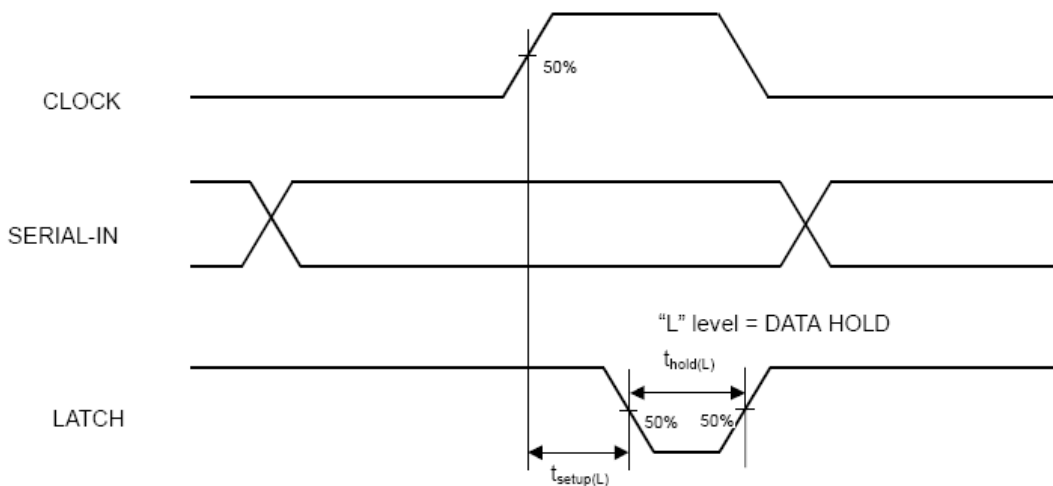


Timing Waveform

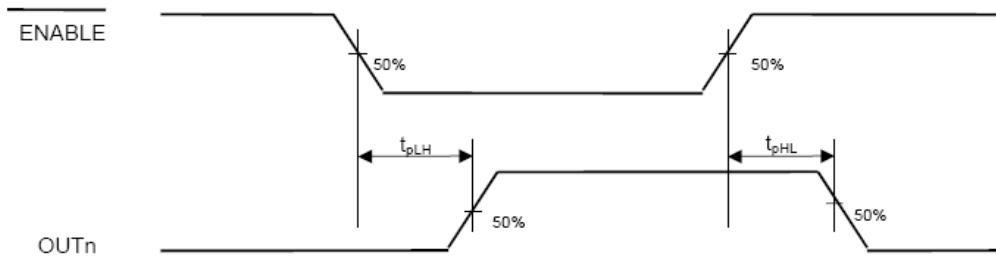
1. CLOCK; OUTn ; SERIAL-IN; SERIAL-OUT



2. CLOCK; SERIAL-IN; LATCH



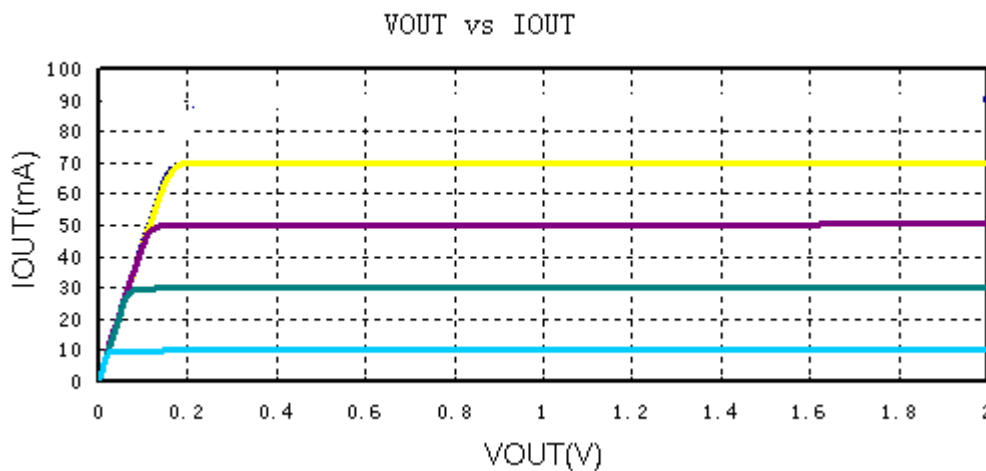
3. ENABLE; OUTn



Constant Current

In LED display application, FD9802 Provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

- 1) The maximum current variation between channels is less than $\pm 3\%$, and that between ICs is less than $\pm 4\%$.
- 2) The output current can be kept constant regardless of the variations of LED forward voltages (V_f). This performs as a perfection of load regulation.

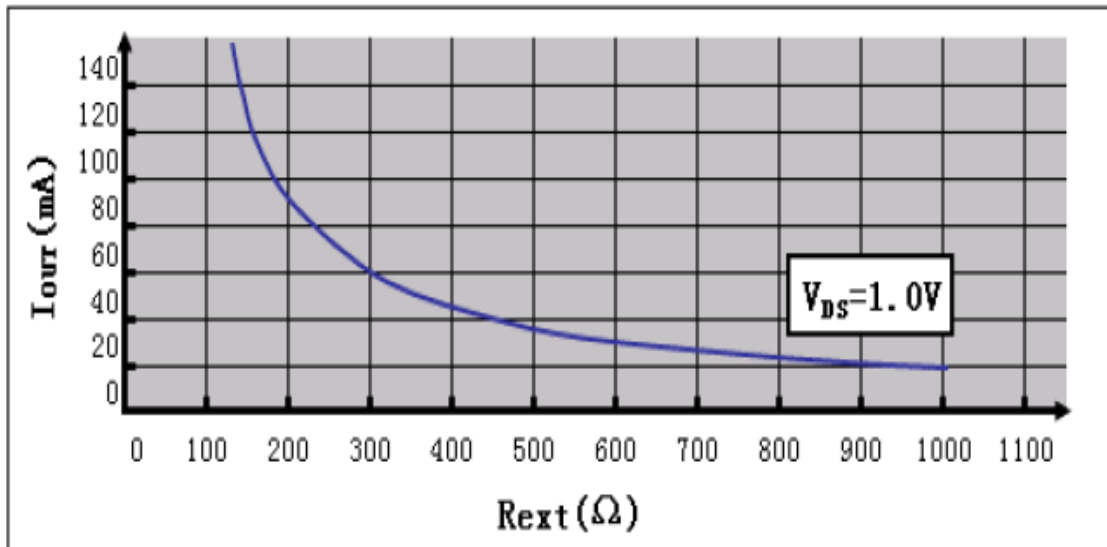




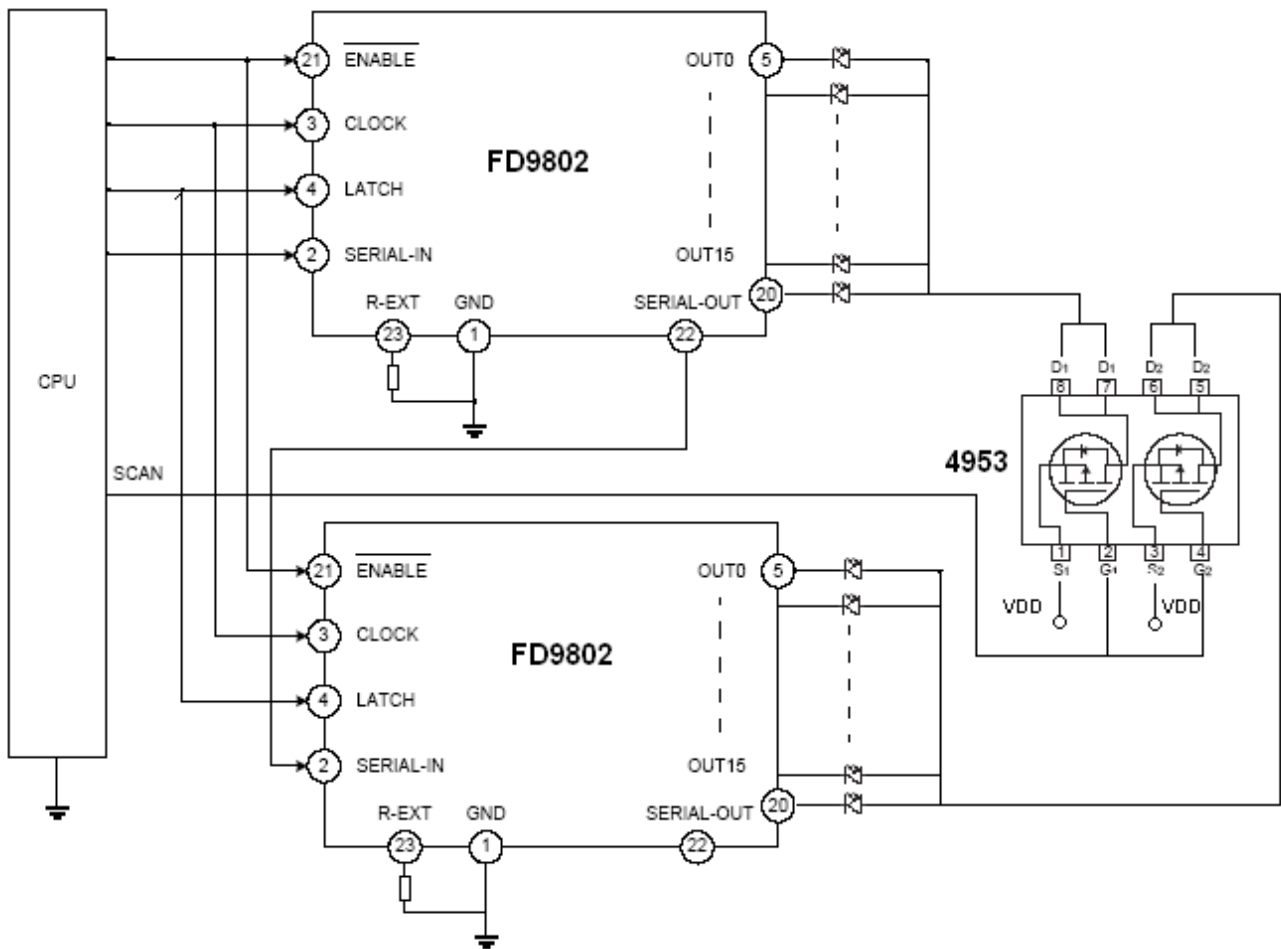
Output Current Setting (I_{OUT}-R-EXT)

The output current is set by the external resistor R_{SET}. The output current is:

$$I_{out} = (1.23/R_{ext}) \times 15.3$$



Application circuitry



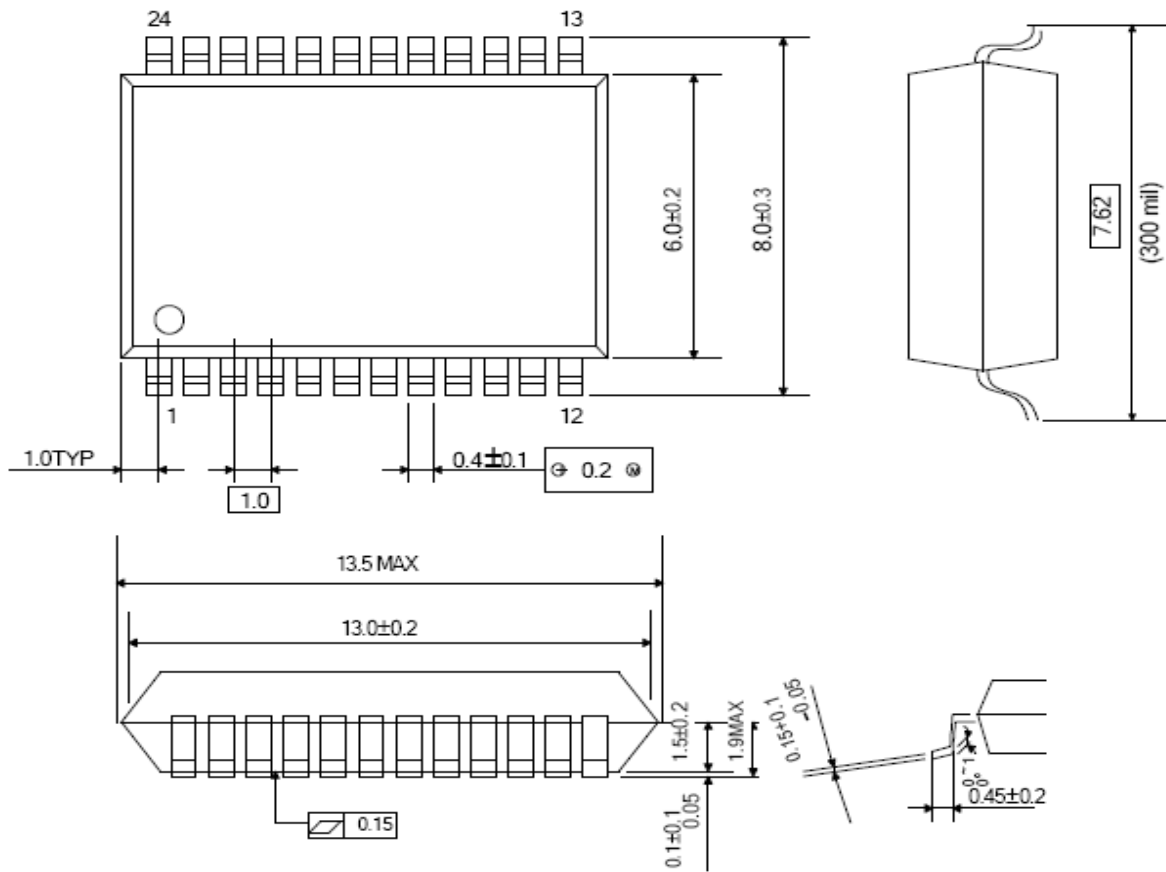
Package Information



Part Number	Package Type
FD9802C	SSOP24-300-1.00
FD9802D	SSOP24-150-0.635

FD9802C (SSOP24-300-1.00)

Unit: mm



Weight: 0.32g (Typ.)



FD9802D (SSOP24-150-0.635)

Unit: mm

