FAIRCHILD™

June 2014

FDB024N08BL7

N-Channel PowerTrench® MOSFET

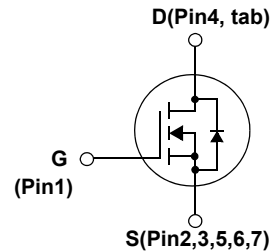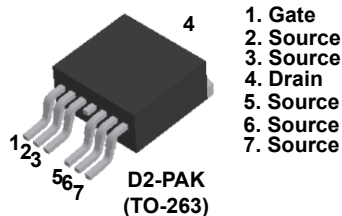### 80 V, 229 A, 2.4 mΩ

Features

- $R_{DS(on)}$ = 1.7 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 100 A
- Low FOM $R_{DS(on)} * Q_G$
- Low Reverse Recovery Charge, Q_{rr} = 112 nC
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- RoHS Compliant
- Qualified according to JEDEC Standards JESD22-A113F and IPC/JEDEC J-STD-020D.1

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies

1. Gate
2. Source
3. Source
4. Drain
5. Source
6. Source
7. Source

D2-PAK (TO-263)

D(Pin4, tab)

G (Pin1)

S(Pin2,3,5,6,7)

MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FDB024N08BL7	Unit
V_{DSS}	Drain to Source Voltage		80	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25°C, Silicon Limited)	229*	A
		- Continuous (T_C = 100°C, Silicon Limited)	162*	
		- Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	- Pulsed (Note 1)	916	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		917	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	246	W
		- Derate Above 25°C	1.64	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

Thermal Characteristics

Symbol	Parameter	FDB024N08BL7	Unit
$R_{θJC}$	Thermal Resistance, Junction to Case, Max.	0.61	°C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB024N08BL7	FDB024N08B	D2PAK-7L	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted

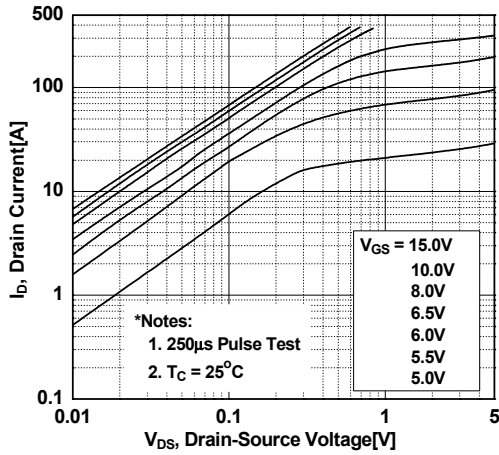| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.05	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 64 V, T_C = 150°C	-	-	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 100 A	-	1.7	2.4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 100 A	-	227	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	-	10170	13530	pF
C_{oss}	Output Capacitance		-	1670	2220	pF
C_{rss}	Reverse Transfer Capacitance		-	35	-	pF
$C_{oss}(er)$	Engry Related Output Capacitance	V_{DS} = 40 V, V_{GS} = 0 V	-	3025	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 100 A	-	137	178	nC
Q_{gs}	Gate to Source Gate Charge		-	56	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	25	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	28	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	2.4	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 100 A, V_{GS} = 10 V, R_G = 4.7 Ω	-	47	104	ns
t_r	Turn-On Rise Time		-	66	142	ns
$t_{d(off)}$	Turn-Off Delay Time		-	87	184	ns
t_f	Turn-Off Fall Time	(Note 4)	-	41	92	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	229*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	916	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 100 A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, V_{DD} = 40 V, I_{SD} = 100 A, dI_F/dt = 100 A/μs	-	80	-	ns
Q_{rr}	Reverse Recovery Charge		-	112	-	nC

Notes:
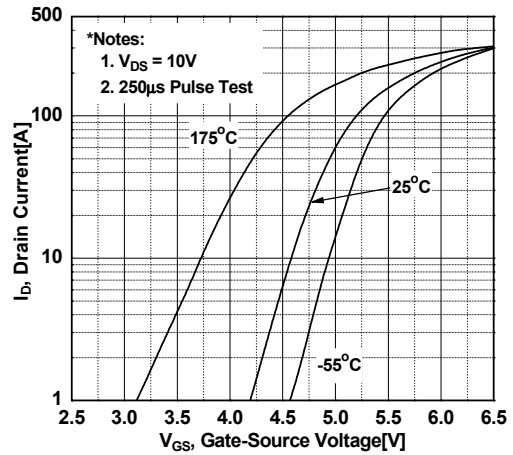
1. Repetitive rating: pulse width limited by maximum junction temperature.
2. L = 3 mH, I_{AS} = 24.72 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 100 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

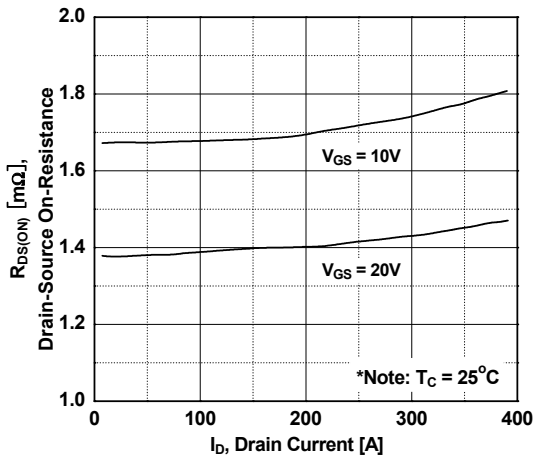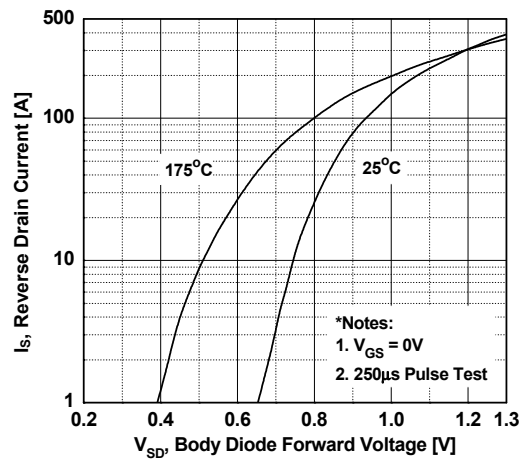### Figure 1. On-Region Characteristics

V_{GS} = 15.0V
10.0V
8.0V
6.5V
6.0V
5.5V
5.0V

*Notes:
1. 250µs Pulse Test
2. T_C = 25°C

I_D, Drain Current[A]

V_{DS}, Drain-Source Voltage[V]

Figure 2. Transfer Characteristics

*Notes:
1. V_{DS} = 10V
2. 250µs Pulse Test

175°C
25°C
-55°C

I_D, Drain Current[A]

V_{GS}, Gate-Source Voltage[V]

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

V_{GS} = 10V
V_{GS} = 20V

*Note: T_C = 25°C

$R_{DS(ON)}$ [mΩ], Drain-Source On-Resistance

I_D, Drain Current [A]

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

175°C
25°C

*Notes:
1. V_{GS} = 0V
2. 250µs Pulse Test

I_S, Reverse Drain Current [A]

V_{SD}, Body Diode Forward Voltage [V]

Figure 5. Capacitance Characteristics

C_{iss}
C_{oss}
C_{rss}

*Note:
1. V_{GS} = 0V
2. f = 1MHz

$C_{iss} = C_{gs} + C_{gd}$ (C_{ds} = shorted)
$C_{oss} = C_{ds} + C_{gd}$
$C_{rss} = C_{gd}$

Capacitances [pF]

V_{DS}, Drain-Source Voltage [V]
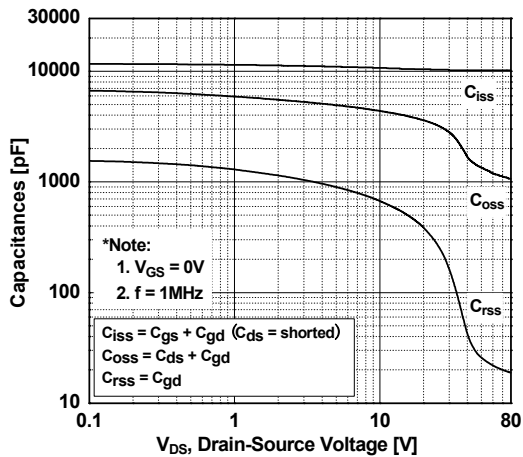
Figure 6. Gate Charge Characteristics

V_{DS} = 16V
V_{DS} = 40V
V_{DS} = 64V

*Note: I_D = 100A

V_{GS}, Gate-Source Voltage [V]

Q_g, Total Gate Charge [nC]
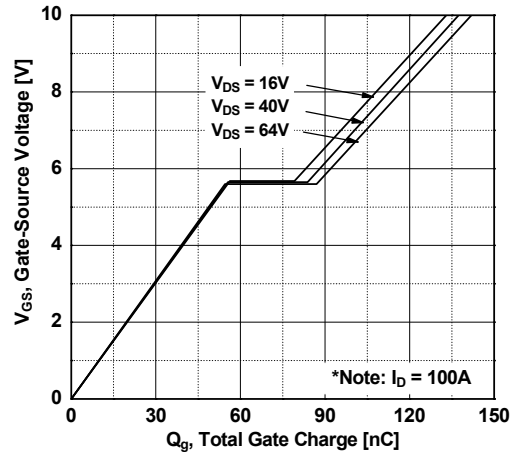
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. V_{GS} = 0V
2. I_D = 250µA
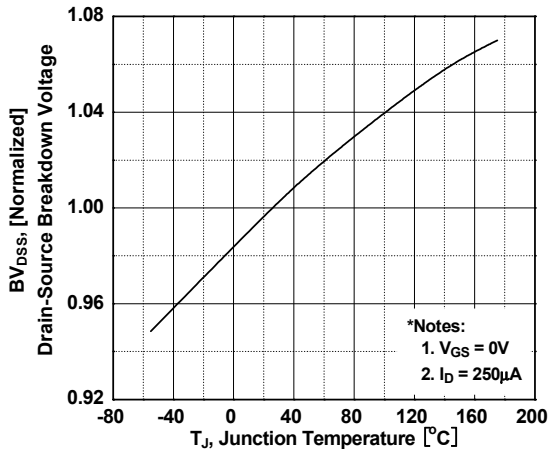
Figure 8. On-Resistance Variation vs. Temperature

*Notes:
1. V_{GS} = 10V
2. I_D = 100A
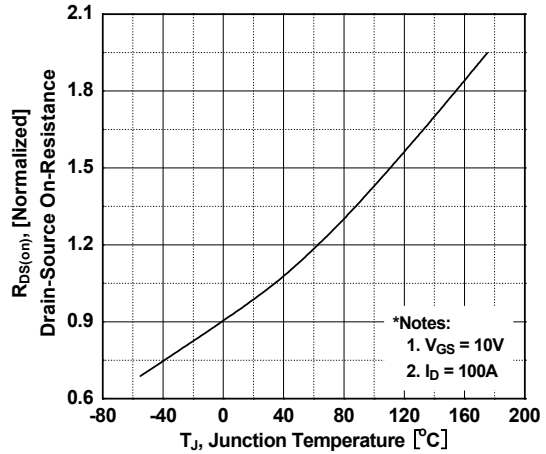
Figure 9. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

*Notes:
1. T_C = 25°C
2. T_J = 175°C
3. Single Pulse
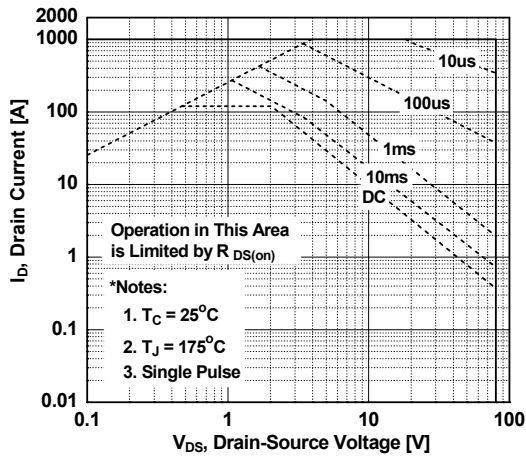
Figure 10. Maximum Drain Current vs. Case Temperature

V_{GS} = 10V

$R_{\theta JC}$ = 0.61°C/W
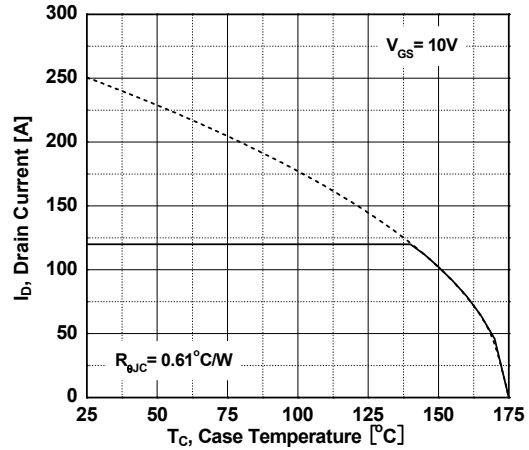
Figure 11. Eoss vs. Drain to Source Voltage
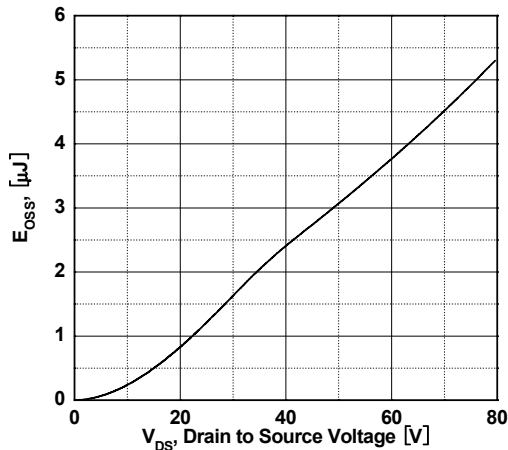
Figure 12. Unclamped Inductive Switching Capability

If R = 0
t_{AV} = (L) (I_{AS})/ (1.3*RATED BV_{DSS}-V_{DD})
If R = 0
t_{AV} = (L/R)ln [(I_{AS}*R)/ (1.3*RATED BV_{DSS}-V_{DD})+1]

STARTING T_J = 25°C

STARTING T_J = 150°C
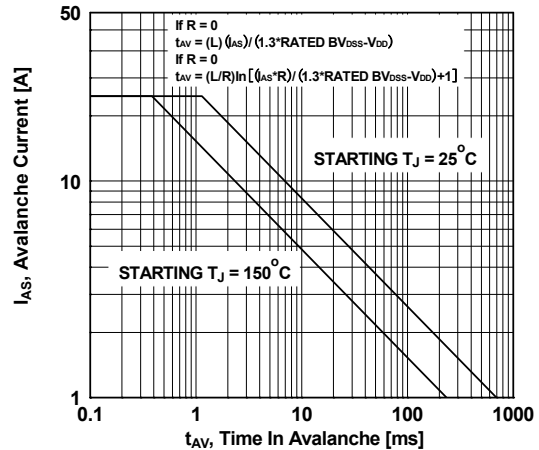
Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

Thermal Response [$Z_{\theta JC}$]

0.5
0.2
0.1
0.05
0.02
0.01
Single pulse

P_{DM}

t_1
t_2

*Notes:
1. $Z_{\theta JC}(t) = 0.61^{\circ}C/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Rectangular Pulse Duration [sec]
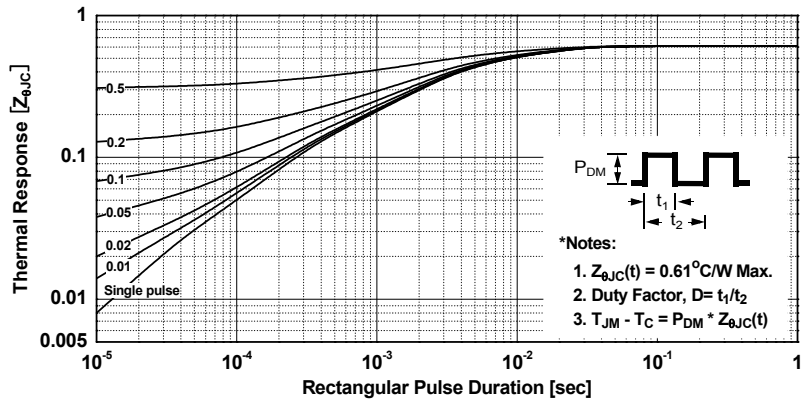
Figure 13. Gate Charge Test Circuit & Waveform
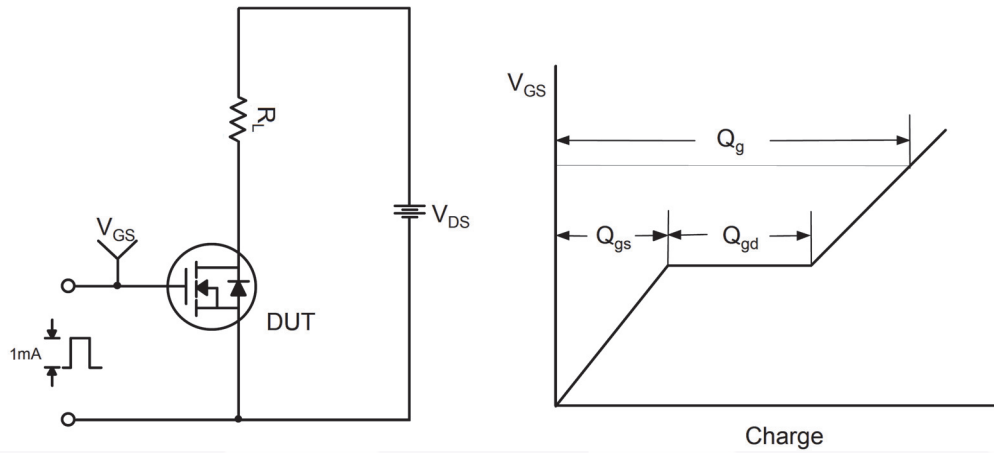
Figure 14. Resistive Switching Test Circuit & Waveforms
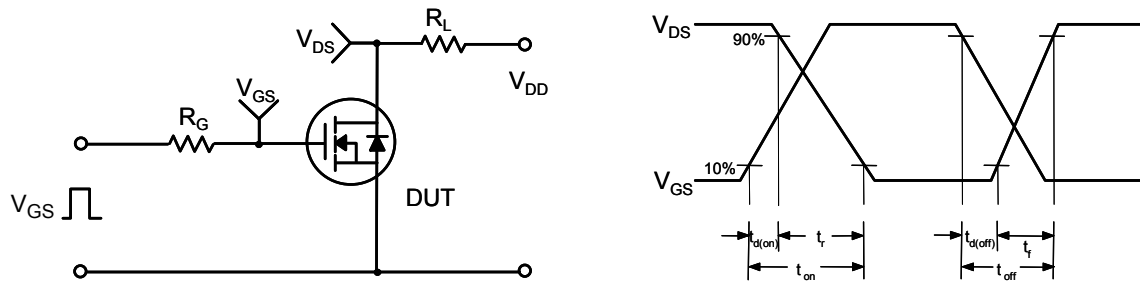
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

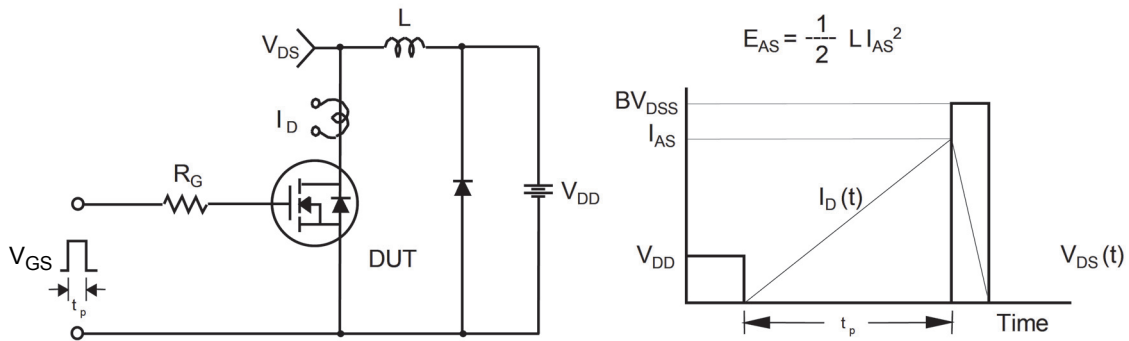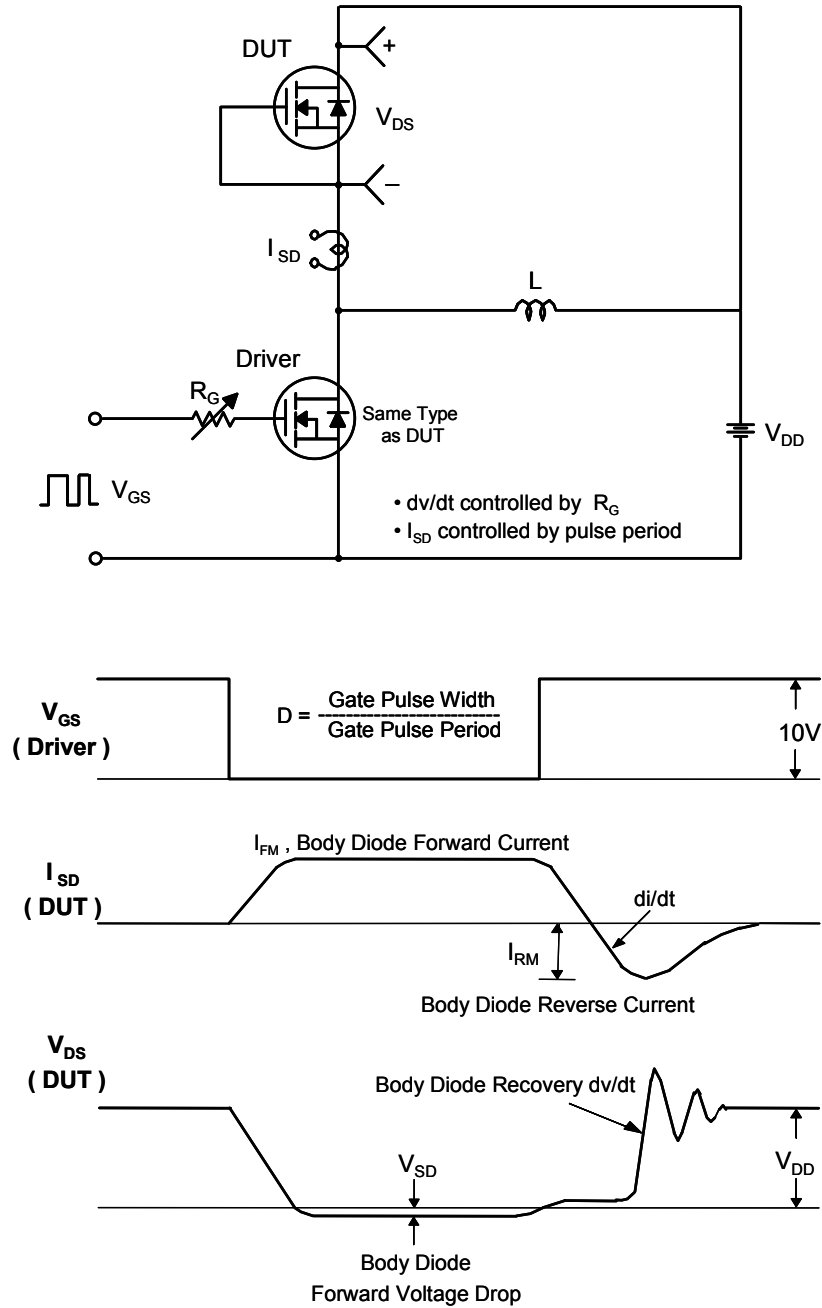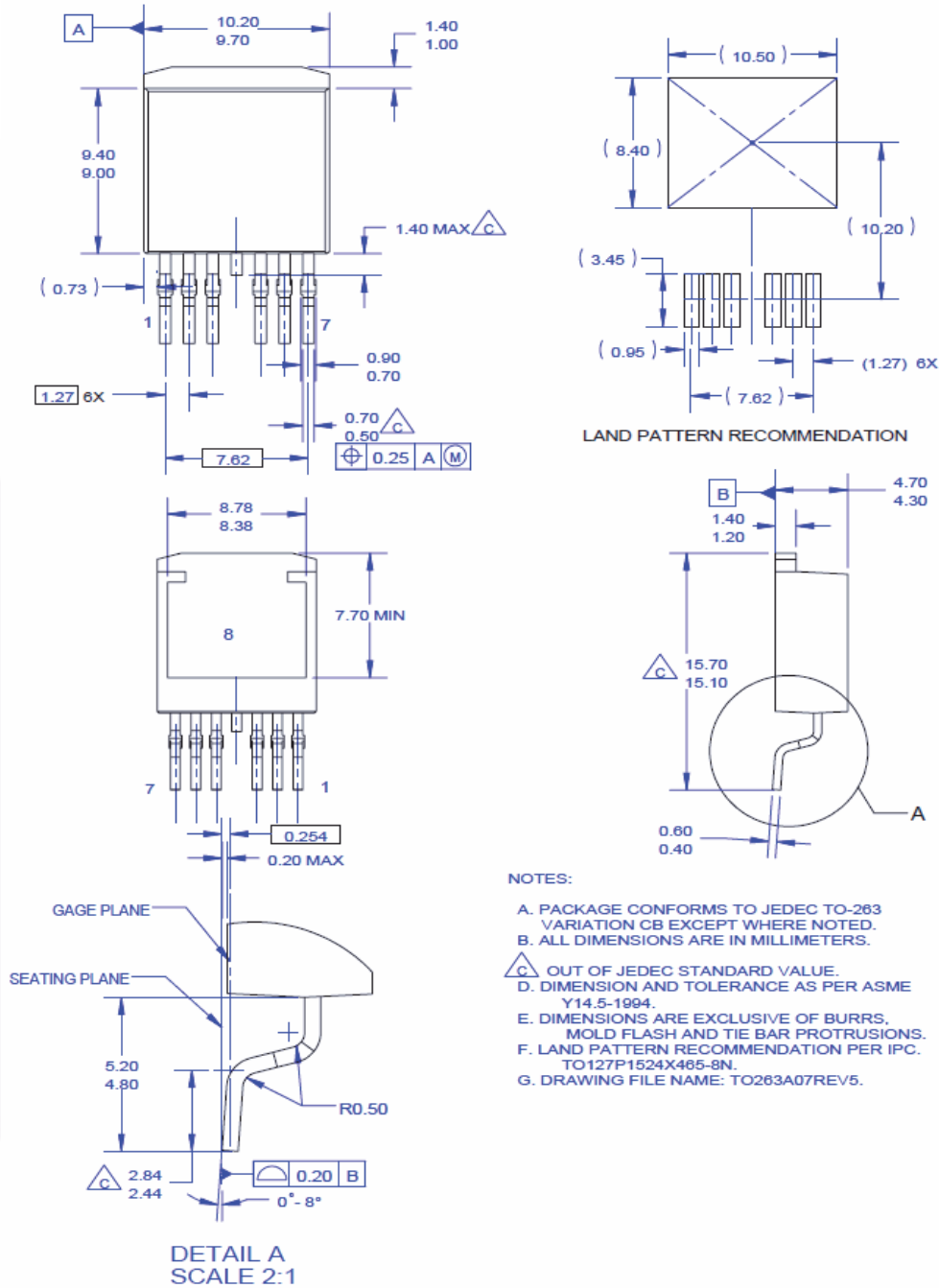## Mechanical Dimensions

LAND PATTERN RECOMMENDATION

GAGE PLANE

SEATING PLANE

DETAIL A
SCALE 2:1

NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263
   VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

C. OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME
   Y14.5-1994.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH AND TIE BAR PROTRUSIONS.
F. LAND PATTERN RECOMMENDATION PER IPC.
   TO127P1524X465-8N.
G. DRAWING FILE NAME: TO263A07REV5.

Figure 17. TO263 (D²PAK), Molded, 7-Lead, Surface Mount

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TO263-0R7

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	F-PFS™	®	SYSTEM ®* GENERAL
AX-CAP®*	FRFET®		
BitSiC™	Global Power Resource℠	PowerTrench®	TinyBoost®
Build it Now™	GreenBridge™	PowerXS™	TinyBuck®
CorePLUS™	Green FPS™	Programmable Active Droop™	TinyCalc™
CorePOWER™	Green FPS™ e-Series™	QFET®	TinyLogic®
CROSSVOLT™	Gmax™	QS™	TINYOPTO™
CTL™	GTO™	Quiet Series™	TinyPower™
Current Transfer Logic™	IntelliMAX™	RapidConfig™	TinyPWM™
DEUXPEED®	ISOPLANAR™	™	TinyWire™
Dual Cool™	Marking Small Speakers Sound Louder and Better™	Saving our world, 1mW/W/kW at a time™	TranSiC™
EcoSPARK®		SignalWise™	TriFault Detect™
EfficentMax™	MegaBuck™	SmartMax™	TRUECURRENT®*
ESBC™	MICROCOUPLER™	SMART START™	μSerDes™
F ®	MicroFET™	Solutions for Your Success™	μ SerDes™
Fairchild®	MicroPak™	SPM®	
Fairchild Semiconductor®	MicroPak2™	STEALTH™	UHC®
FACT Quiet Series™	MillerDrive™	SuperFET®	Ultra FRFET™
FACT®	MotionMax™	SuperSOT™-3	UniFET™
FAST®	mWSaver®	SuperSOT™-6	VCX™
FastvCore™	OptoHiT™	SuperSOT™-8	VisualMax™
FETBench™	OPTOLOGIC®	SupreMOS®	VoltagePlus™
FPS™	OPTOPLANAR®	SyncFET™	XS™
		Sync-Lock™	仙童™

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I68

www.fairchildsemi.com