

MOSFET – N-Channel, POWERTRENCH®

100 V, 214 A, 3.5 mΩ

FDB035N10A

Description

This N-Channel MOSFET is produced using onsemi's advance POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

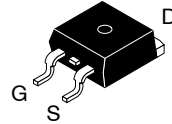
- $R_{DS(on)} = 3.0\text{ m}\Omega$ (Typ.) @ $V_{GS} = 10\text{ V}$, $I_D = 75\text{ A}$
- Fast Switching Speed
- Low Gate Charge, $Q_G = 89\text{ nC}$ (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

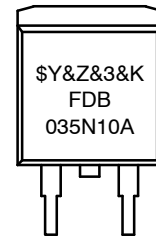
V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
100 V	3.5 mΩ @ 10 V	214 A*

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

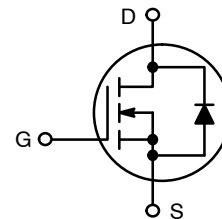


**D²PAK-3 (TO-263, 3-LEAD)
 CASE 418AJ**

MARKING DIAGRAM



\$Y = Logo
 &Z = Assembly Plant Code
 &3 = 3-Digit Date Code Format
 &K = 2-Digits Lot Run Traceability Code
 FDB035N10A = Device Code



N-Channel

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

FDB035N10A

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FDB035N10A	Unit
V _{DSS}	Drain to Source Voltage	100	V
V _{GSS}	Gate to Source Voltage	±20	V
I _D	Drain Current	- Continuous (T _C = 25°C, Silicon Limited)	214*
		- Continuous (T _C = 100°C, Silicon Limited)	151*
		- Continuous (T _C = 25°C, Package Limited)	120
I _{DM}	Drain Current	- Pulsed (Note 1)	856
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	658	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P _D	Power Dissipation	(T _C = 25°C)	333
		- Derate Above 25°C	2.22
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. Starting T_J = 25°C, L = 1 mH, I_{AS} = 36.3 A.
3. I_{SD} ≤ 75 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDB035N10A	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.45	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in ² Pad of 2-oz Copper), Max.	40	

FDB035N10A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V, T _C = 25°C	100	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	0.07	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, T _C = 150°C	-	-	500	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 75 A	-	3.0	3.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 75 A	-	167	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	5485	7295	pF
C _{oss}	Output Capacitance		-	2430	3230	pF
C _{rss}	Reverse Transfer Capacitance		-	210	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 80 V, I _D = 75 A, V _{GS} = 10 V (Note 4)	-	89	116	nC
Q _{gs}	Gate to Source Gate Charge		-	24	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		-	8	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	25	-	nC

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 50 V, I _D = 75 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	-	22	54	ns
t _r	Turn-On Rise Time		-	54	118	ns
t _{d(off)}	Turn-Off Delay Time		-	37	84	ns
t _f	Turn-Off Fall Time		-	11	32	ns
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	1.2	-	Ω

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	214*	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	856	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 75 A	-	-	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 75 A, V _{DD} = 80 V, dI _F /dt = 100 A/μs	-	72	-	ns
Q _{rr}	Reverse Recovery Charge		-	129	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

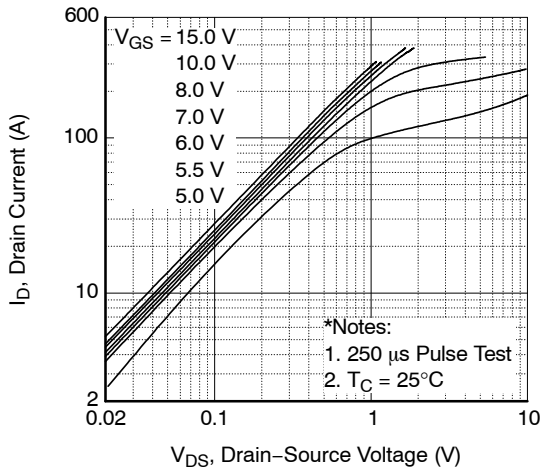


Figure 1. On-Region Characteristics

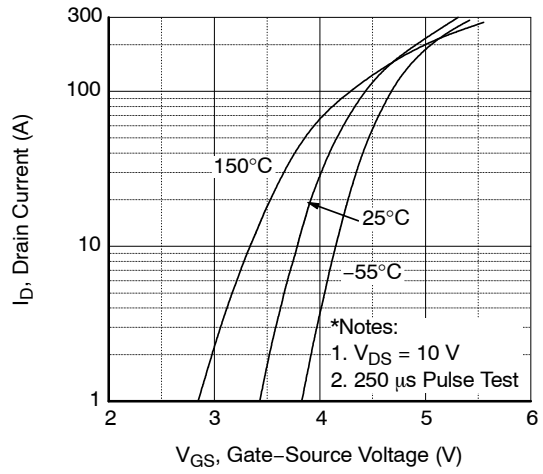


Figure 2. Transfer Characteristics

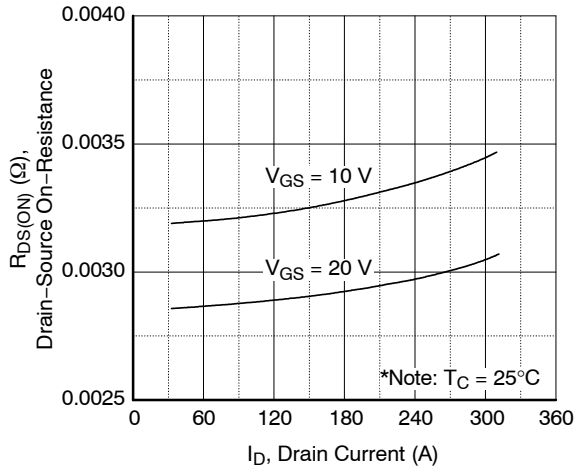


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

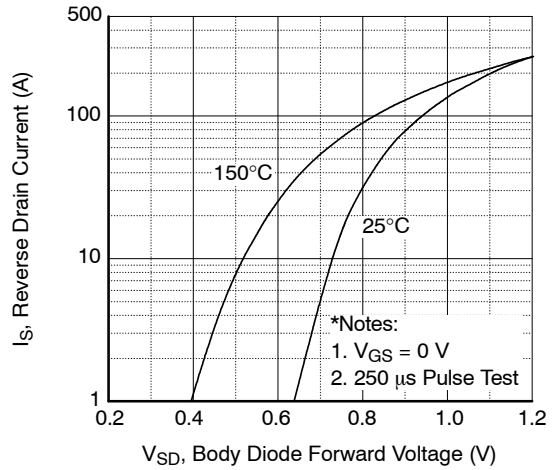


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

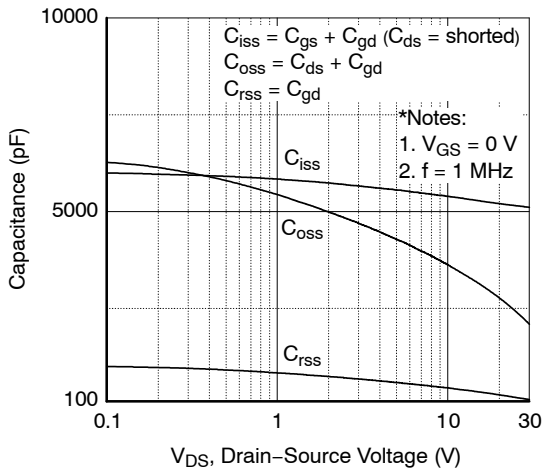


Figure 5. Capacitance Characteristics

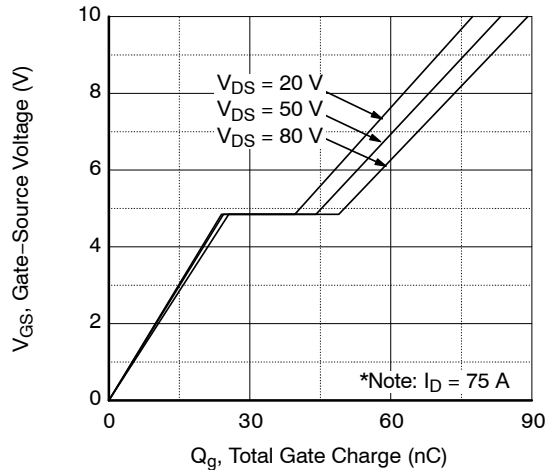


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

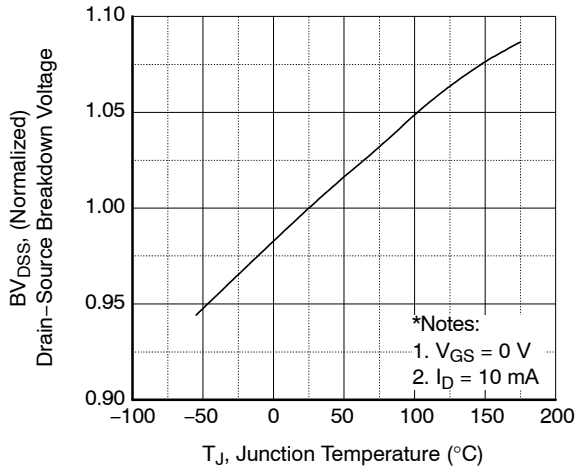


Figure 7. Breakdown Voltage Variation vs. Temperature

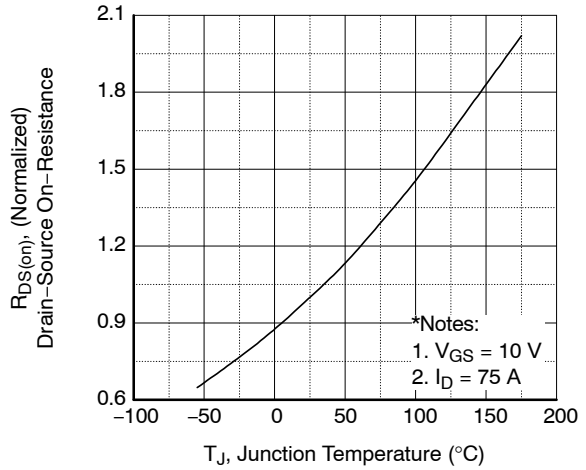


Figure 8. On-Resistance Variation vs. Temperature

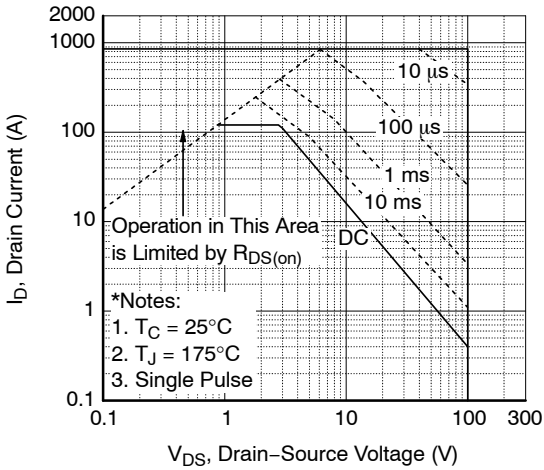


Figure 9. Maximum Safe Operating Area

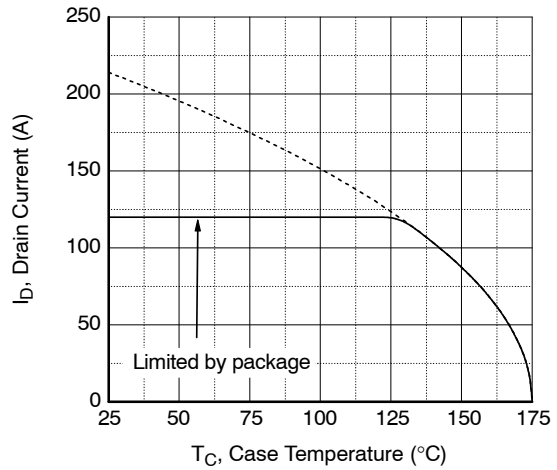


Figure 10. Maximum Drain Current vs. Case Temperature

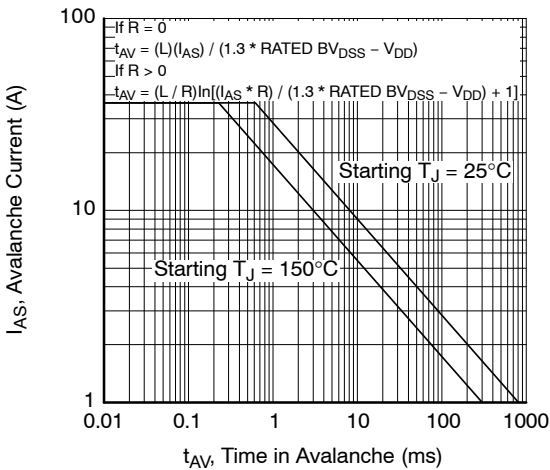


Figure 11. Unclamped Inductive Switching Capability

FDB035N10A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

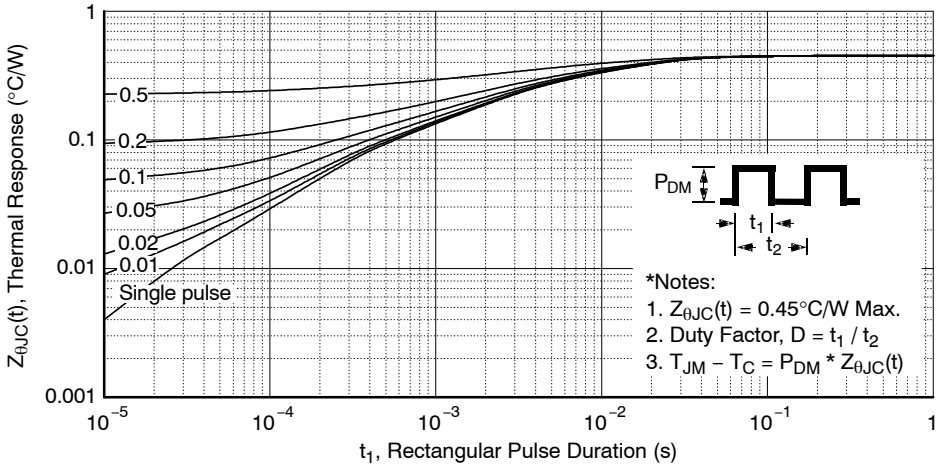


Figure 12. Transient Thermal Response Curve

FDB035N10A

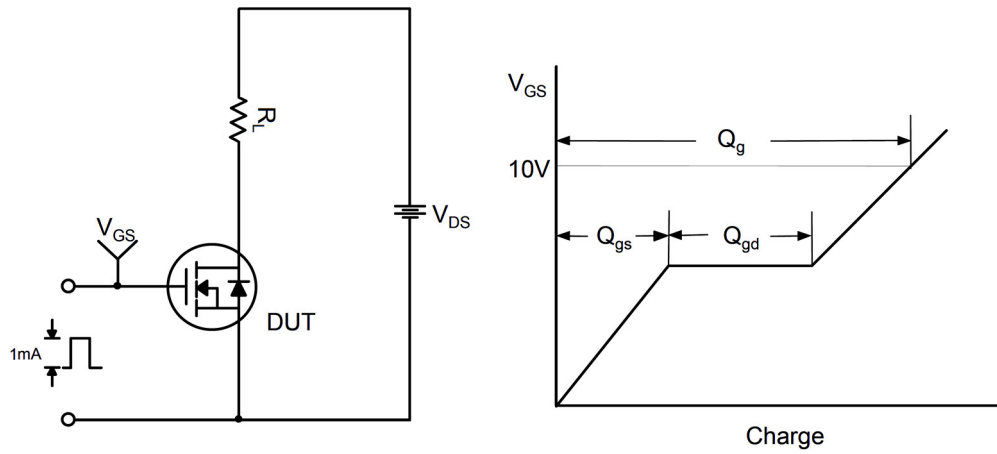


Figure 13. Gate Charge Test Circuit & Waveform

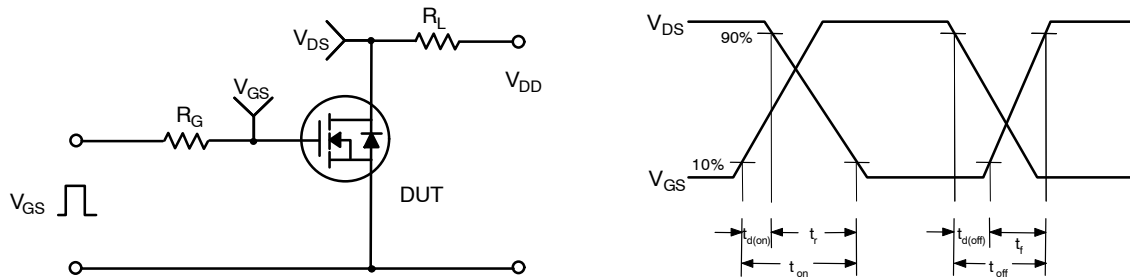


Figure 14. Resistive Switching Test Circuit & Waveforms

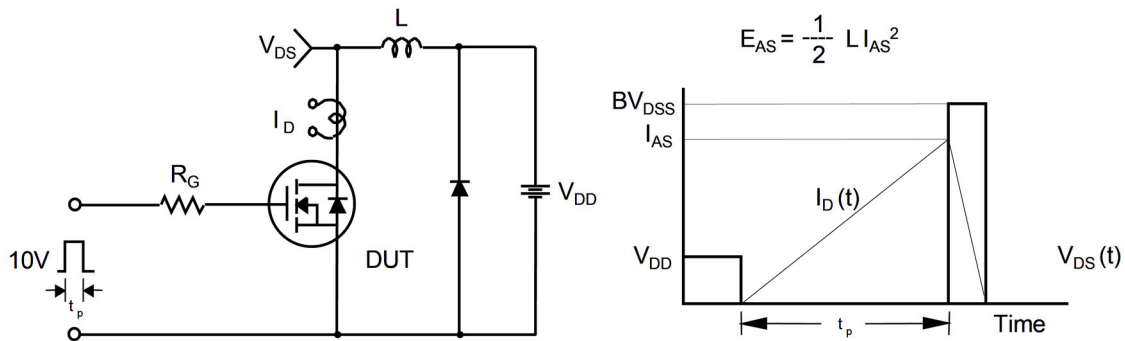


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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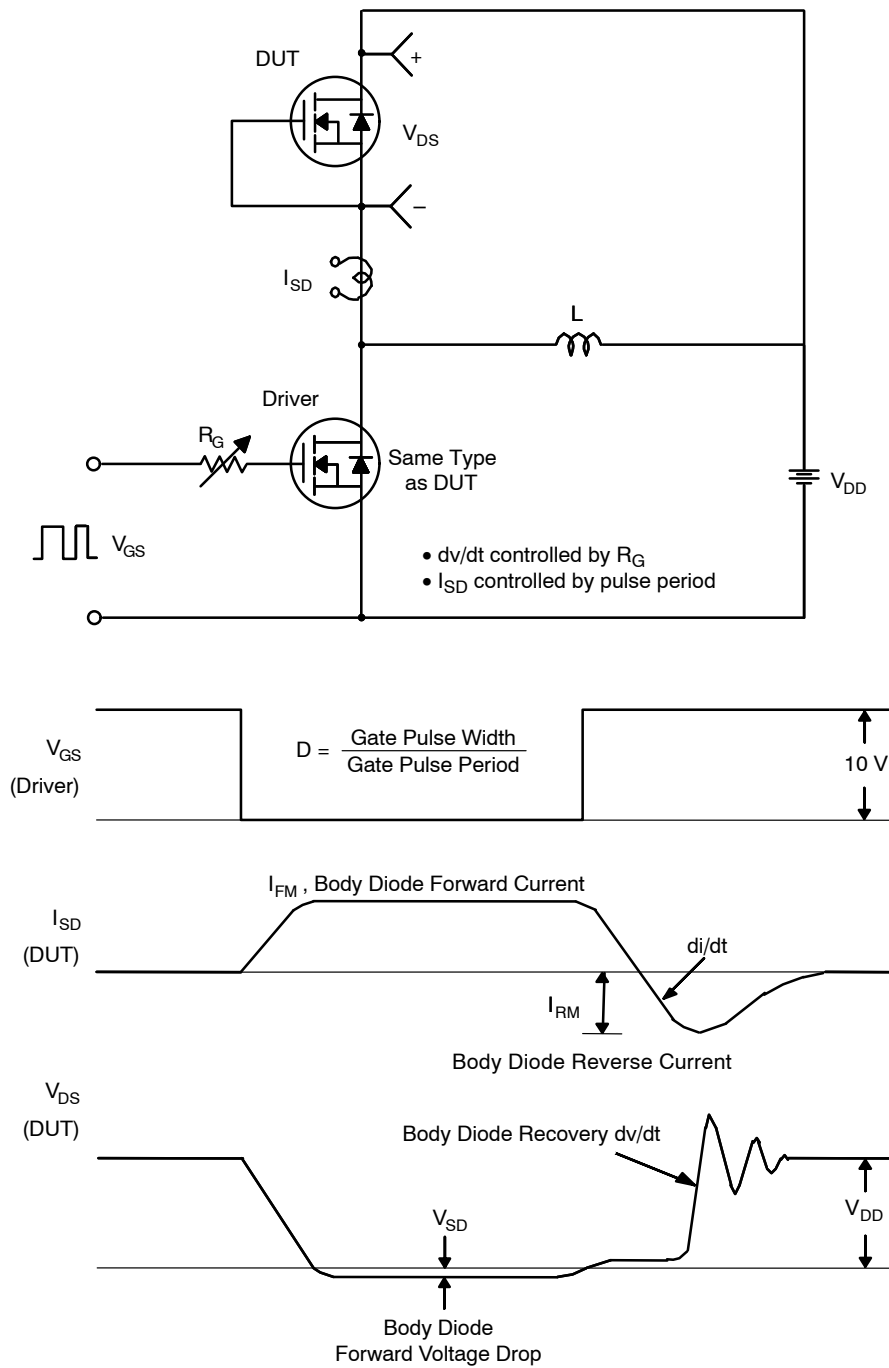


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping [†]
FDB035N10A	FDB035N10A	D ² -PAK	330 mm	24 mm	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

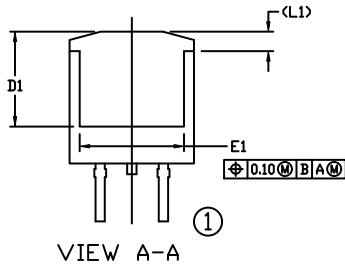
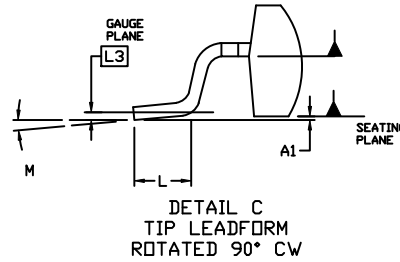
■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



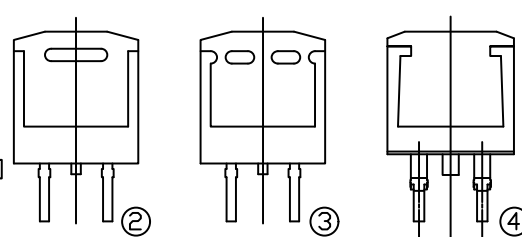
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

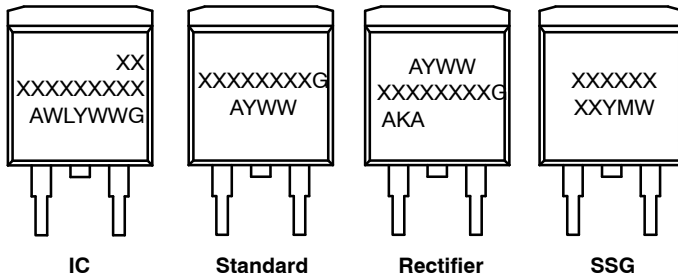


VIEW A-A



VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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