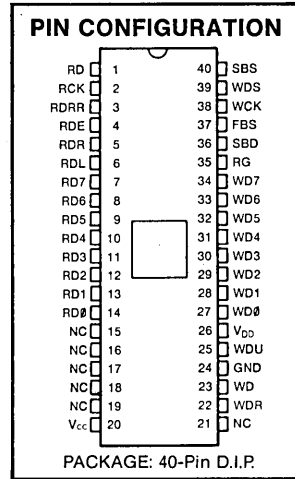


Floppy Disk Hard Sector Data Handler HSDH

FEATURES

- Hard-Sectored Operation — performs all data operations
- Single or Double Density Operation — recording code independent
- Minifloppy or Standard Floppy compatible
- Programmable Sync Byte
- Internal Sync Byte Detection and Byte Framing
- Fully Double Buffered
- Data Overrun/Underrun Detection
- Dual Disk Operation — Write on one disk drive while simultaneously reading from another
- Tri-State Output Bus for processor compatibility
- TTL Compatible Inputs and Outputs

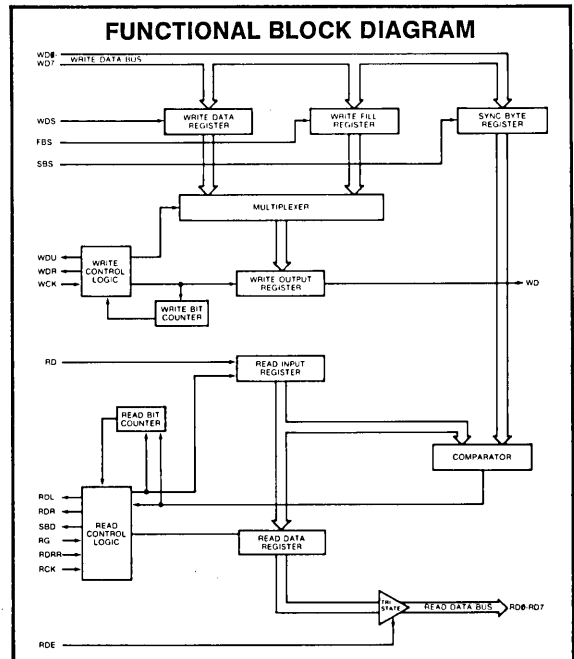


GENERAL DESCRIPTION

The FDC3400 is an MOS integrated circuit which simplifies the data interface between a processor and a floppy disk drive. During a write operation, the HSDH receives data from the processor and shifts it out bit-serially to the floppy disk data encoding logic. Similarly, during a read operation the HSDH receives a bit-serial stream of read data from the floppy disk data separator, establishes byte synchronization by detecting the sync byte, and transfers data on a byte by byte basis to the processor.

The HSDH detects data overrun and underrun conditions and indicates these conditions on its status lines. A data underrun causes write data to be written onto the disk from a special programmable fill register until new data is entered into the write data buffer or until the write operation is ended.

Separate read and write data registers permit simultaneous read and write operations on two different drives for enhanced system throughput. The HSDH is fully double buffered and all inputs and outputs are TTL compatible.



SECTION VI

DESCRIPTION OF OPERATION

Prior to reading or writing on the disk, the read/write head must be positioned and loaded onto the desired track.

Write Operation

The Write Clock is set at the desired bit rate (usually 125, 250, or 500KHz), and the desired fill byte is written into the Write Fill Register. After the external logic makes the write enable to the drive active, the first byte to be written should be loaded into the Write Data Register. This byte is then loaded into the Write Output Register and shifted out bit serially to the external write encoding logic. The first bit shifted out of each byte is the LSB. Whenever a byte is transferred from the Write Data Register to the Write Output Register, Write Data Request becomes active and requests another byte from the processor. If new data is not loaded into the Write Data Register before the Write Output Register becomes empty, then the Write Output Register is loaded with data from the Write Fill Register and the Write Data Underrun status line is set. WDU is reset the next time WDS is pulsed. At the end of the write operation, the processor should return the external write enable line to an inactive state.

Read Operation

The Read Clock is set at the desired bit rate (usually 125, 250, or 500KHz) and the desired sync byte is loaded into the Sync Byte Register. When the processor wishes to read a sector of data it causes a transition on the Read Gate input to set the read logic into a sync byte search mode. In the search mode the serial read data bit stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found, by definition, when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the Sync Byte Detected output is set high. This byte is then loaded into the Read Data Register and the read logic is set into the

byte mode. In this mode each byte read is loaded into the Read Data Register and Read Data Request is made active high for each byte. The processor responds to each Read Data Request by enabling the output bus with Read Data Enable, reading the data byte from the Read Data Register, and resetting Read Data Request by pulsing Read Data Request Reset. If the processor fails to respond to Read Data Request within one byte time, the Read Data Lost status line is set. When the processor has read the required amount of data it may reset Read Gate to an inactive-high level.

System Operation — Additional Features

Automatic Sector Fill

In some applications, such as the end of a logical file, the system buffer may contain less than a full sector of data. In this case the processor need supply only this data to the FDC3400. The FDC3400 will then under-run, setting the Write Data Underrun Status line and thereby causing the remainder of the sector to fill with bytes taken from the Write Fill Register. This operation continues until the processor returns the disk's write enable signal to an inactive level.

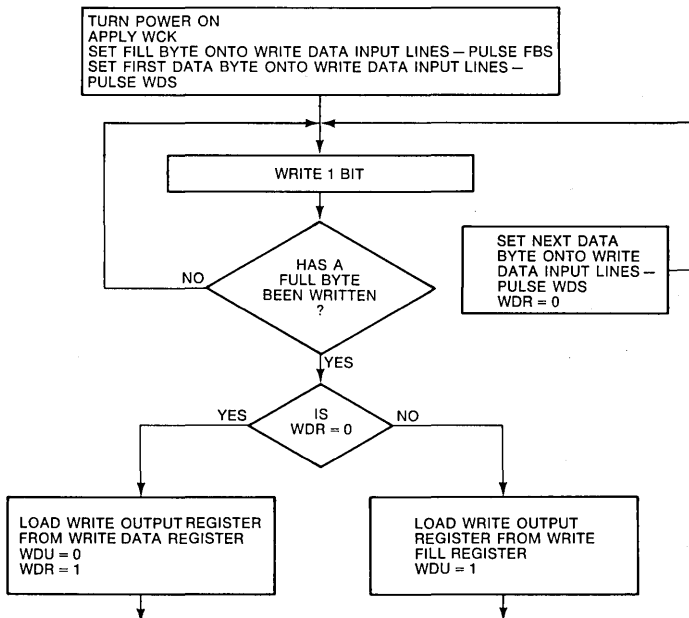
Byte Search

After byte synchronization has been established during a read operation, the processor may load a different byte into the Sync Byte Register. Whenever that byte occurs in the data being read, the Sync Byte Detected status line will go high. This feature permits the processor to search for the occurrence of a specific byte while reading a sector.

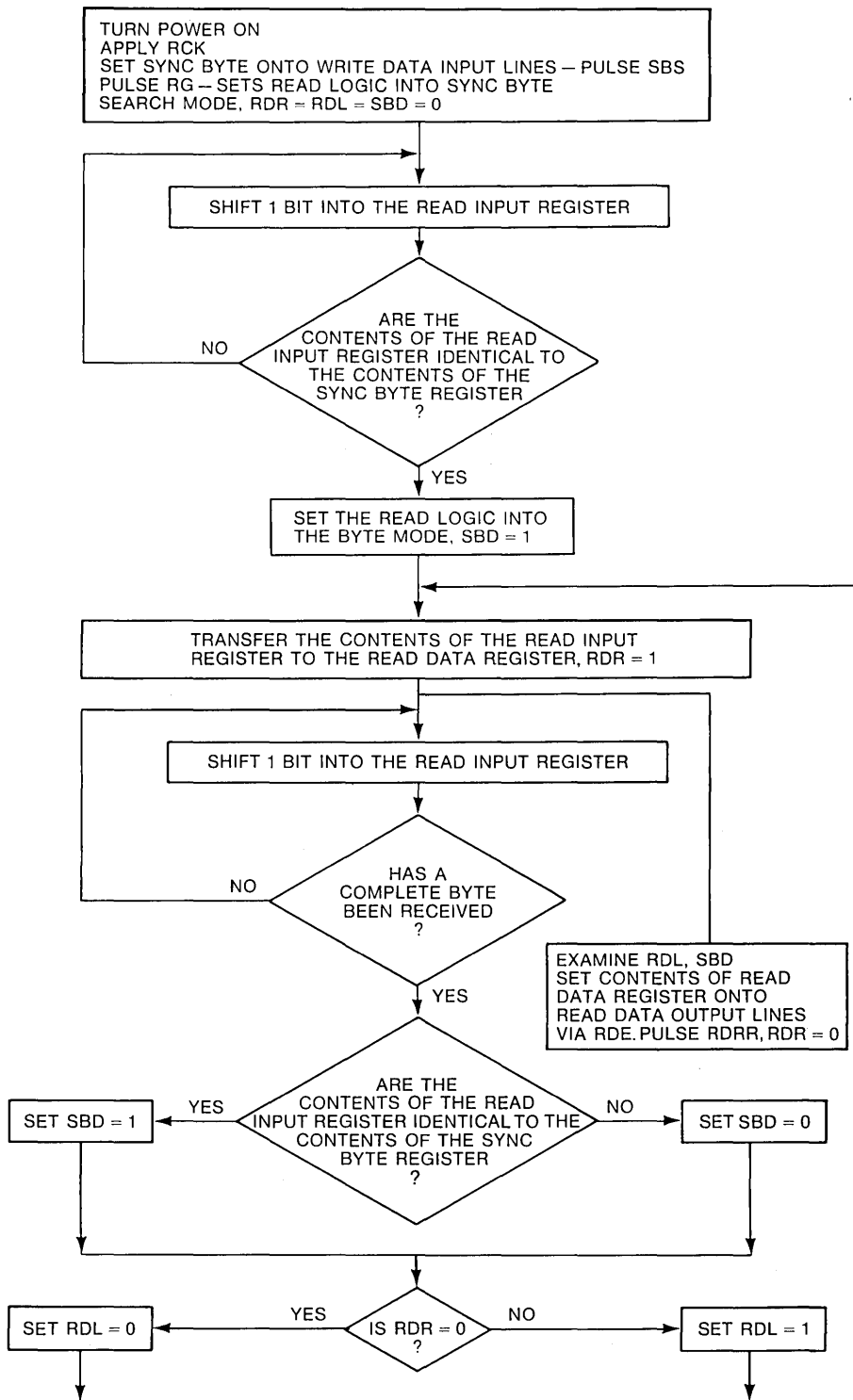
Multiple Byte Synchronization

Some systems use two or more contiguous sync bytes to establish byte synchronization. For these applications, the number of Read Data Requests received while Sync Byte Detected remains active-high may be counted by the processor to establish valid synchronization.

FLOW DIAGRAM — WRITE DATA



FLOW DIAGRAM — READ DATA



SECTION VI

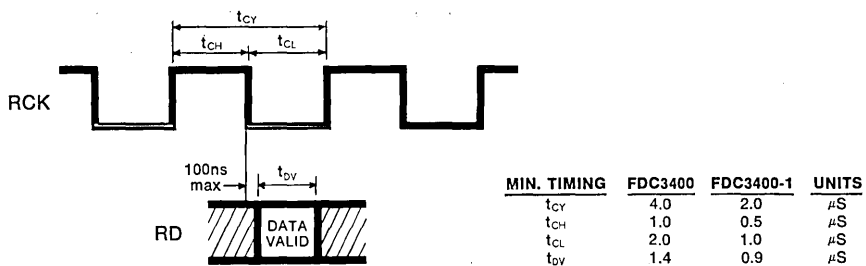
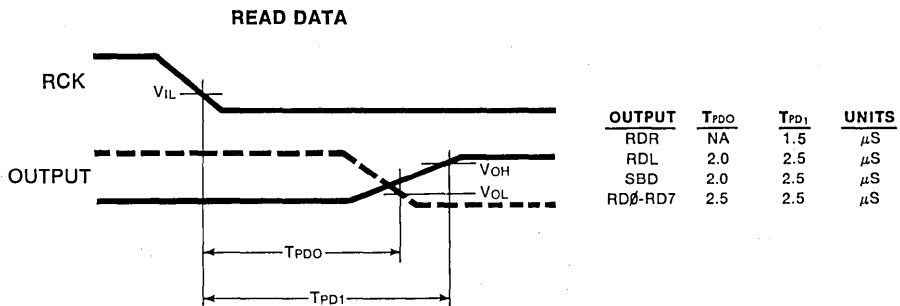
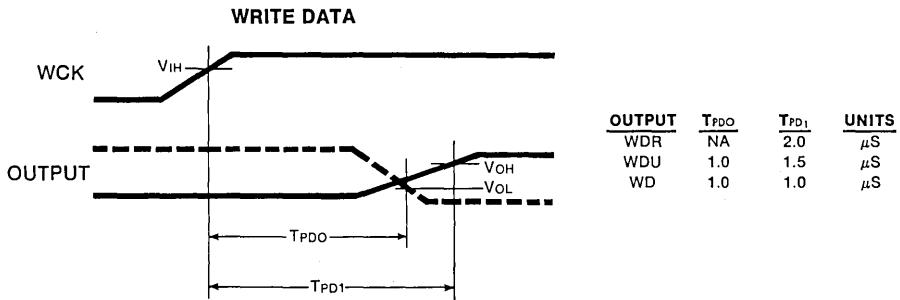
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	RD	Read Data	The Read Data input accepts the serial data stream from the floppy disk data separator.
2	RCK	Read Clock	The negative-going edge of the Read Clock input shifts Read Data into the Read Input Register.
3	RDRR	Read Data Request Reset	An active-high pulse input on the Read Data Request Reset input resets the RDR output to a low level.
4	RDE	Read Data Enable	An active-high level on the Read Data Enable line gates the outputs of the Read Data Register onto the Read Data Output lines.
5	RDR	Read Data Request	The Read Data Request output is made active-high when an assembled byte is transferred from the Read Input Register to the Read Data Register.
6	RDL	Read Data Lost	The Read Data Lost output is made active-high, if the byte presently in the Read Data Register is not read (RDR not reset) by the processor before the next byte is loaded into the Read Data Register.
7-14	RD7-RD \emptyset	Read Data Output	When enabled by RDE the tri-state Read Data Output lines present the data in the Read Data Register to the processor. When RDE is inactive-low the RD7-RD \emptyset lines are held at a high-impedance state.
15-19	NC		Not Connected
20	V _{cc}	Power Supply	+ 5 volt supply
21	NC		Not Connected
22	WDR	Write Data Request	The Write Data Request output is made active-high when the Write Data Register becomes empty and requires a data byte. It is reset to a low level when WDS occurs to load the Write Data Register. If WDR is not serviced by the time the next byte is required by the Write Output Register, the byte stored in the Write Fill Register is written onto the disk and the WDU line is made active high.
23	WD	Write Data	The Write Data output presents the serial stream of data to the external write data encoder. Each byte is normally provided from the Write Data Register provided that a WDS pulse occurs during the presently written byte. If WDS is not pulsed, the next byte to be written will be extracted from the Write Fill Register.
24	GND	Ground	Ground
25	WDU	Write Data Underrun	The Write Data Underrun output is set active-high when the processor fails to respond to the WDR signal within one byte time. When WDU occurs the data written on the disk is extracted from the Write Fill Register. This line is reset when WDS is pulsed.
26	V _{DD}	Power Supply	-12 volt supply
27-34	WD \emptyset -WD7	Write Data Input	The Write Data Input lines present information to the Write Data Register, the Write Fill Register, and the Sync Byte Register under control of their respective strobes. The strobes operate independently of each other. The LSB should always be placed on WD \emptyset .
35	RG	Read Gate	This input should be pulsed to a high-level after power turn on to reset RDR, SBD, and RDL to an inactive-low level. The high-to-low transition of RG sets the read logic into the sync byte search mode. In this mode the serial Read Data stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found by definition when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the SBD output is set active-high. The sync byte just read is then transferred into the Read Data Register; RDR is set high, and the read logic is set into the byte mode. In this mode each byte read is transferred into the Read Data Register.
36	SBD	Sync Byte Detected	The Sync Byte Detected output is set active-high each time the byte loaded into the Read Data Register is identical to the byte in the Sync Byte Register. This output is reset low the next time the Read Data Register is loaded with a byte which is not a sync byte.

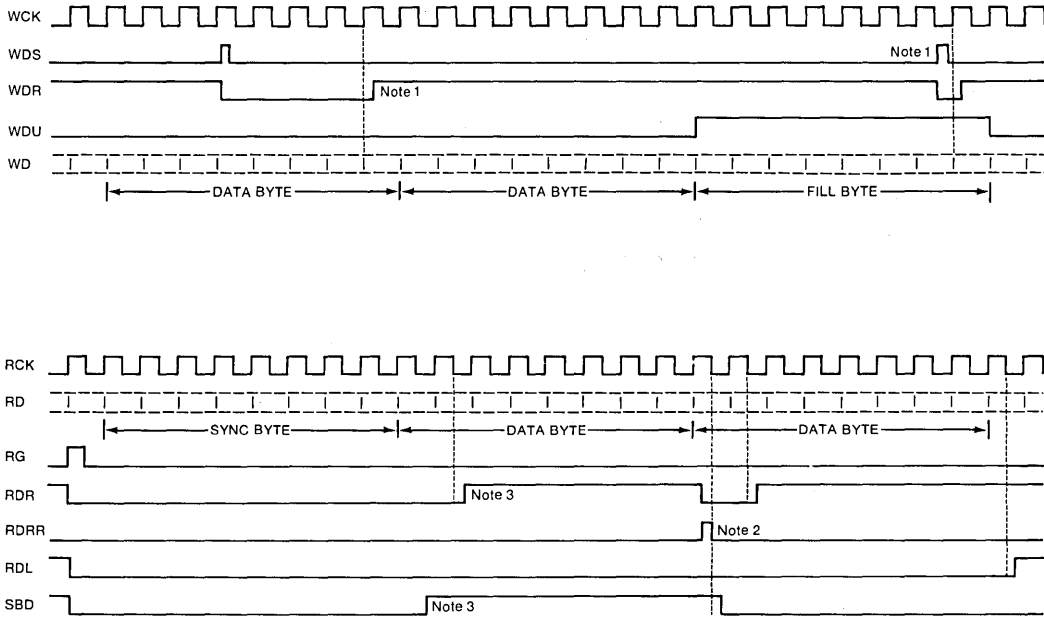
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
37	FBS	Fill Byte Strobe	The Fill Byte Strobe is an active-high input strobe which loads the byte on the WD0-WD7 lines into the Write Fill Register.
38	WCK	Write Clock	Each positive-going edge of this clock shifts one bit out of the Write Output Register onto WD.
39	WDS	Write Data Strobe	The Write Data Strobe is an active-high input strobe which loads the byte on the WD0-WD7 lines into the Write Data Register.
40	SBS	Sync Byte Strobe	The Sync Byte Strobe is an active-high input strobe which loads the byte on the WD0-WD7 lines into the Sync Byte Register.

ADDITIONAL TIMING INFORMATION (Typical Propagation Delays)



HSDH TIMING DIAGRAM



NOTE 1

The Write Output Register is loaded with the next byte at the positive clock transition corresponding to the leading edge of the last bit of the current byte on the WD output. WDR is set high approximately two microseconds after this clock transition. If it is desired that the next byte be extracted from the Write Data Register the leading edge of the WDS should occur at least one microsecond prior to this clock transition.

NOTE 2

In order to avoid an RDL indication the leading edge of the RDRR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input.

NOTE 3

The RDL, SBD and RD0-RD7 output are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input. The RDR output is set high at the next negative clock transition.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Load Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3V
Negative Voltage on any Pin, V_{CC}	-25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

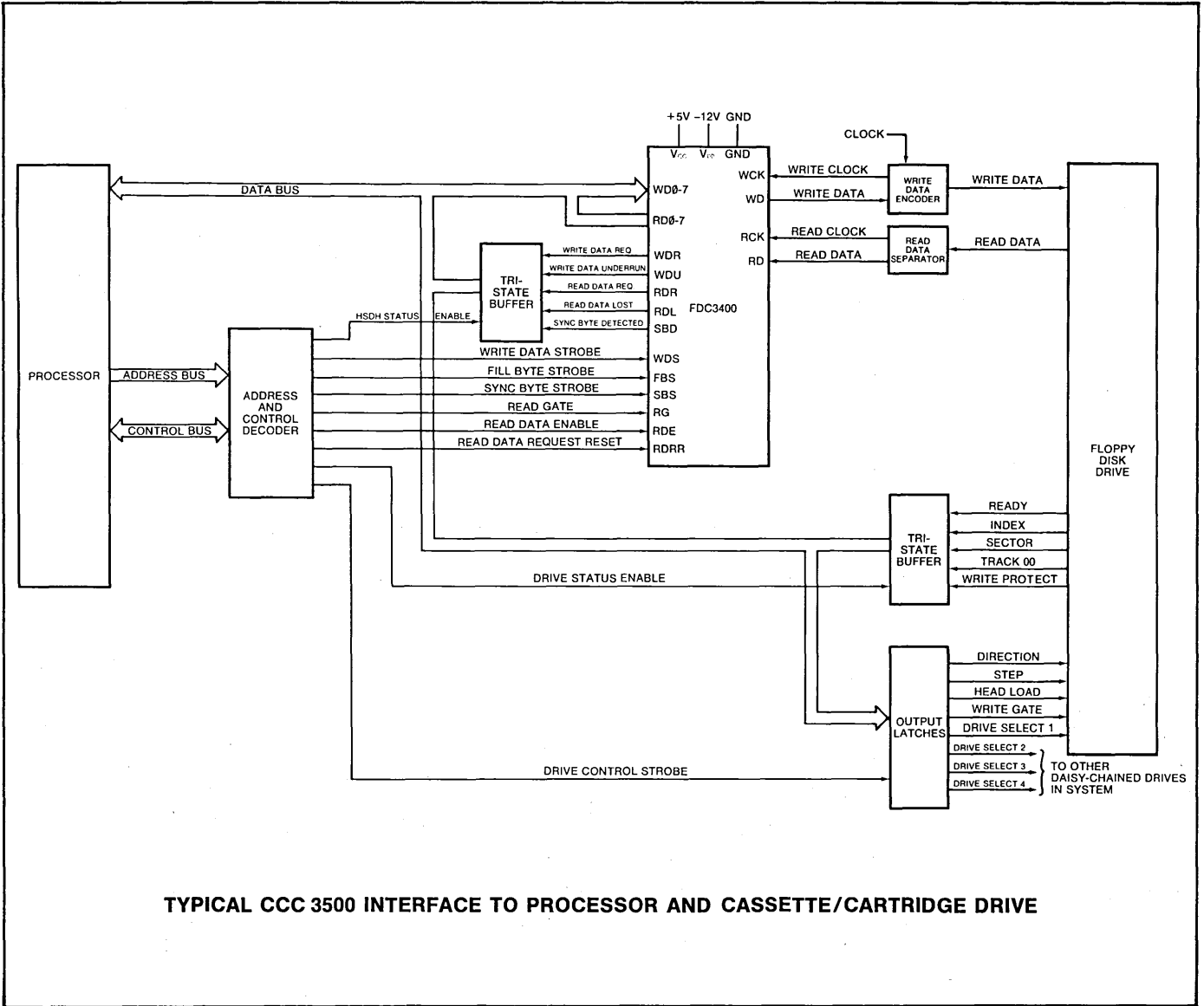
ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	$V_{CC}-1.5$		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	$I_{OL} = 1.6\text{mA}$
High-level, V_{OH}	2.4	4.0		V	$I_{OH} = -100\mu\text{A}$
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	See note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	μA	$RDE = V_{IL}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, I_{OS}^{**}			10	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	$V_{IN} = V_{CC}$, $f = 1\text{MHz}$
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pF	$RDE = V_{IL}$, $f = 1\text{MHz}$
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					
CLOCK FREQUENCY					
	DC		250	KHz	$T_A = +25^\circ\text{C}$ RCK, WCK
	DC		500	KHz	RCK, WCK, FDC3400-1
PULSE WIDTH					
Clock	1			μs	RCK, WCK
	0.5			μs	RCK, WCK, FDC3400-1
Read Gate	1			μs	RG
Write Data Strobe	200			ns	WDS
Fill Byte Strobe	200			ns	FBS
Sync Byte Strobe	200			ns	SBS
Read Data Request Reset	200			ns	RDRR
INPUT SET-UP TIME					
Write Data Inputs	0			ns	WD0-WD7
INPUT HOLD TIME					
Write Data Inputs	0			ns	WD0-WD7
STROBE TO OUTPUT DELAY					
Read Data Enable		180	250	ns	Load = 20pf + 1 TTL input RDE: T_{FD1} , T_{PC0}
OUTPUT DISABLE DELAY					
		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:

- Under steady state condition no current flows for TTL or MOS interfacing.
A switching current of 1.6mA maximum flows during a high to low transition of the input.
- The tri-state output has 3 states:
 - low-impedance to V_{CC}
 - low-impedance to GND
 - high-impedance OFF $\cong 10M$ ohms
 The OFF state is controlled by the RDE input.



TYPICAL CCC 3500 INTERFACE TO PROCESSOR AND CASSETTE/CARTRIDGE DRIVE

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