FAIRCHILD SEMICONDUCTOR®

March 2013

FDD050N03B

N-Channel PowerTrench® MOSFET

30 V, 90 A, 5.0 mΩ

Features

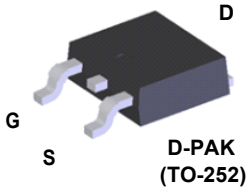
- $R_{DS(on)}$ = 3.7 mΩ (Typ.)@ V_{GS} = 10 V, I_D = 25 A
- Fast Switching Speed
- Low Gate Charge, Q_G = 33 nC(Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

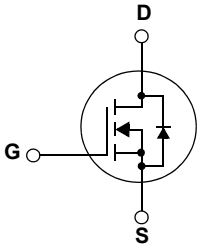
This N-Channel MOSFET is produced using Fairchild Semiconductor®'s advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FDD050N03B	Unit
V_{DSS}	Drain to Source Voltage		30	V
V_{GSS}	Gate to Source Voltage		±16	V
I_D	Drain Current	- Continuous (T_C = 25°C, Silicon Limited)	90*	A
		- Continuous (T_C = 100°C, Silicon Limited)	63*	
		- Continuous (T_C = 25°C, Package Limited)	50	
I_{DM}	Drain Current	- Pulsed (Note 1)	360	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	72	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	2	V/ns
P_D	Power Dissipation	(T_C = 25°C)	65	W
		- Derate above 25°C	0.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 50A.

Thermal Characteristics

Symbol	Parameter		FDD050N03B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.		2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	(Note 5)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD050N03B	FDD050N03B	D-PAK	330mm	16mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_C = 25^oC$	30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	13	-	$mV/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24V$, $V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 16V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	1.25	2.0	3.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 25A$	-	3.7	5.0	mΩ
		$V_{GS} = 4.5V$, $I_D = 15A$	-	5.2	8.1	
g_{FS}	Forward Transconductance	$V_{DS} = 5V$, $I_D = 50A$	-	169	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15V$, $V_{GS} = 0V$, f = 1MHz	-	2160	2875	pF
C_{oss}	Output Capacitance		-	805	1070	pF
C_{rss}	Reverse Transfer Capacitance		-	85	130	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DD} = 15V$, $I_D = 50A$, $V_{GS} = 10V$ (Note 4)	-	33	43	nC
Q_{gs}	Gate to Source Gate Charge		-	7.8	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	3.8	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	4.6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15V$, $I_D = 50A$, $V_{GS} = 10V$, $R_{GEN} = 4.7\Omega$ (Note 4)	-	14.5	39	ns
t_r	Turn-On Rise Time		-	4.5	18	ns
$t_{d(off)}$	Turn-Off Delay Time		-	30	70	ns
t_f	Turn-Off Fall Time		-	4.5	19	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	90*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	360	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 50A$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 50A$, $dI_F/dt = 100A/\mu s$	-	33	-	ns
Q_{rr}	Reverse Recovery Charge		-	19	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 1mH, $I_{AS} = 12A$, $V_{DD} = 27V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \le 50A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics
5. When mounted on a 1 in^2 pad of 2 oz copper

Typical Performance Characteristics

Figure 1. On-Region Characteristics

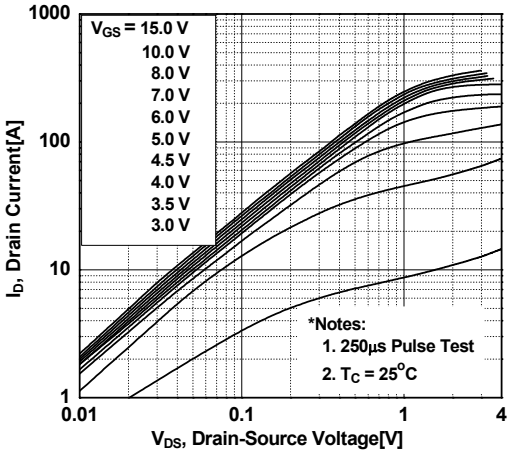


Figure 2. Transfer Characteristics

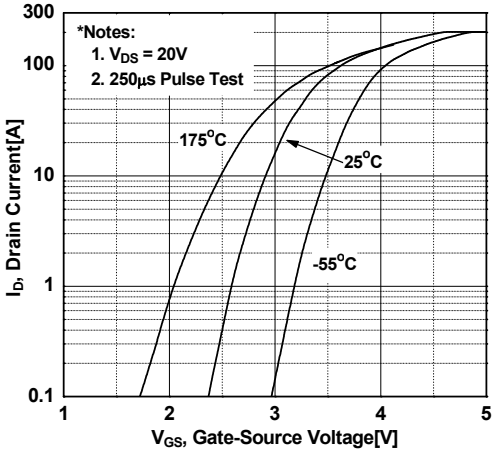


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

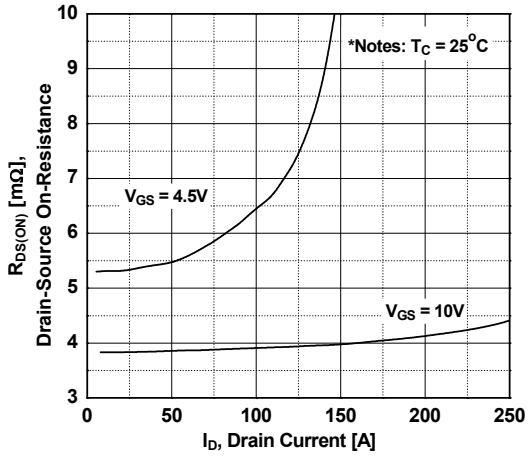


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

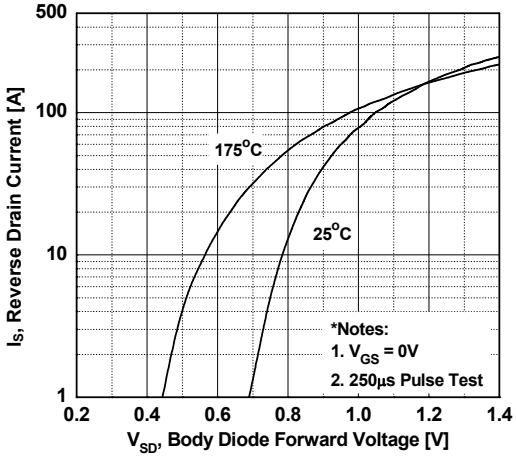


Figure 5. Capacitance Characteristics

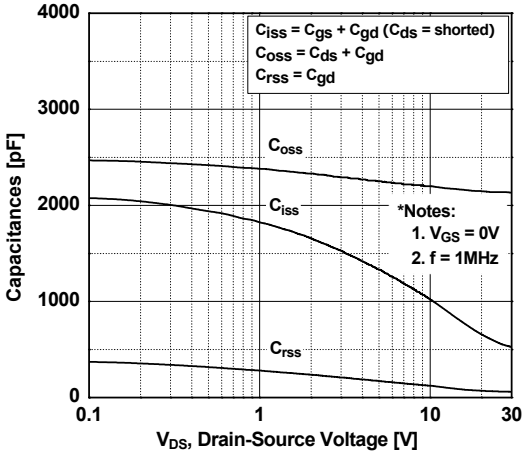
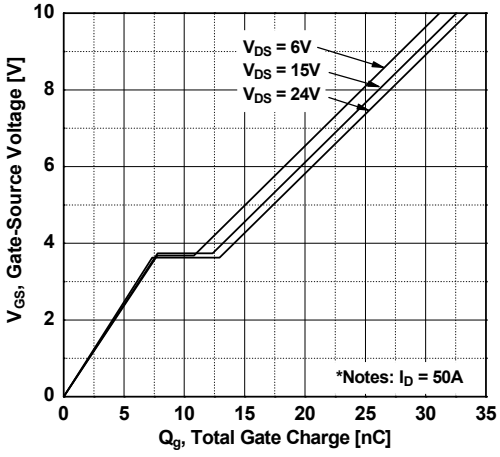


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

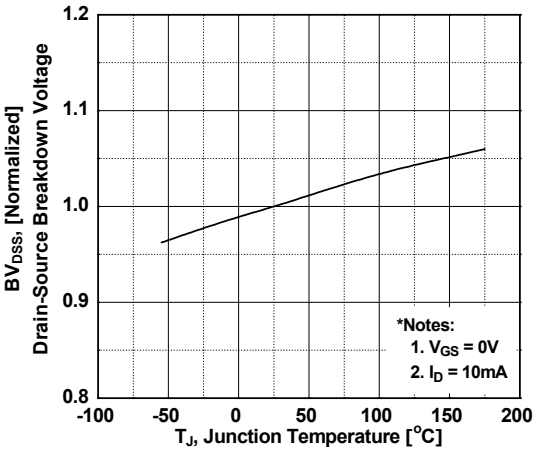


Figure 8. On-Resistance Variation vs. Temperature

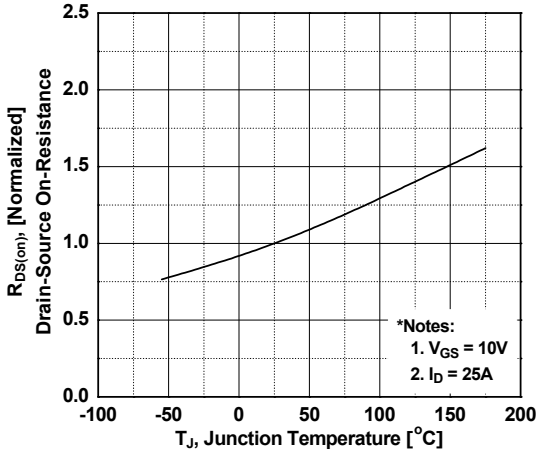


Figure 9. Maximum Safe Operating Area

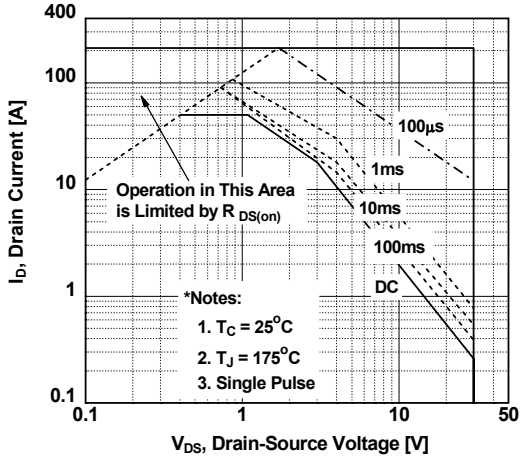


Figure 10. Maximum Drain Current vs. Case Temperature

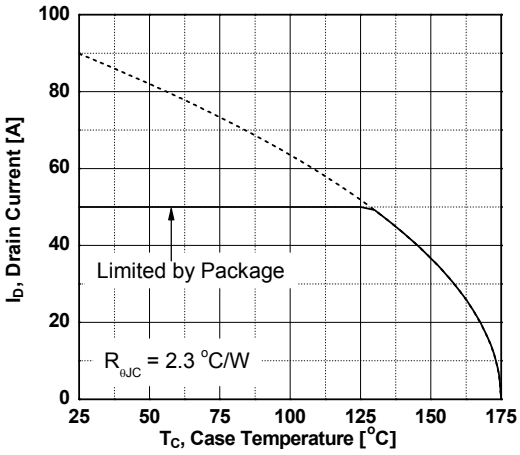
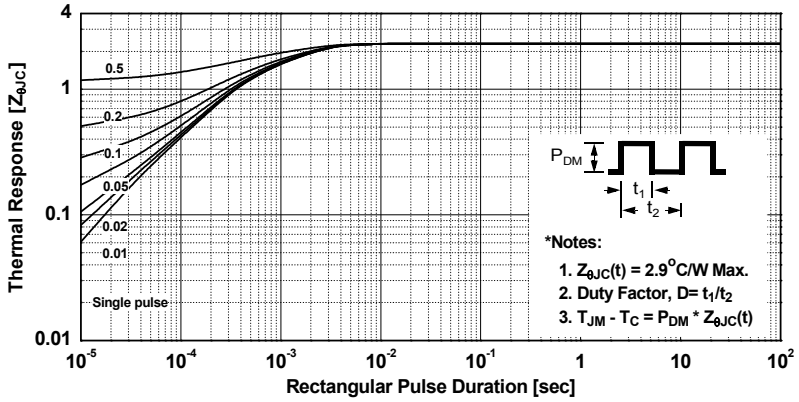
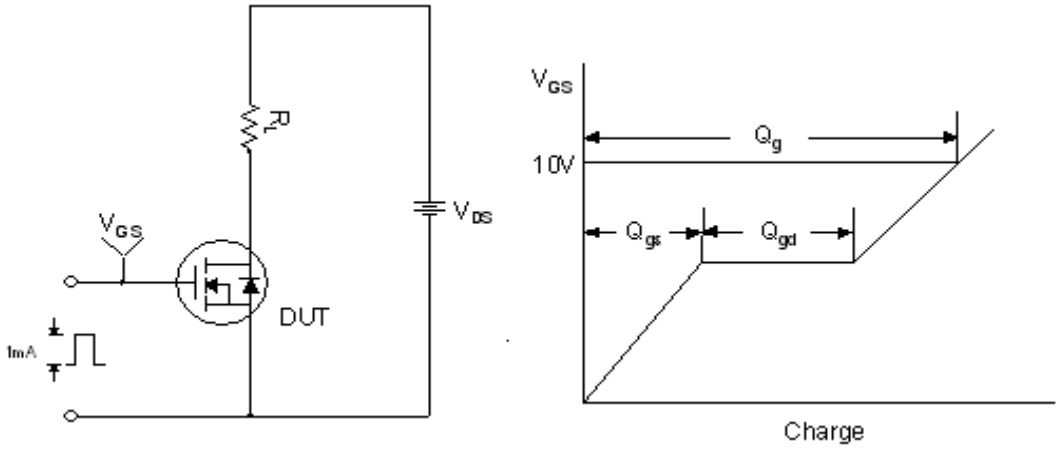


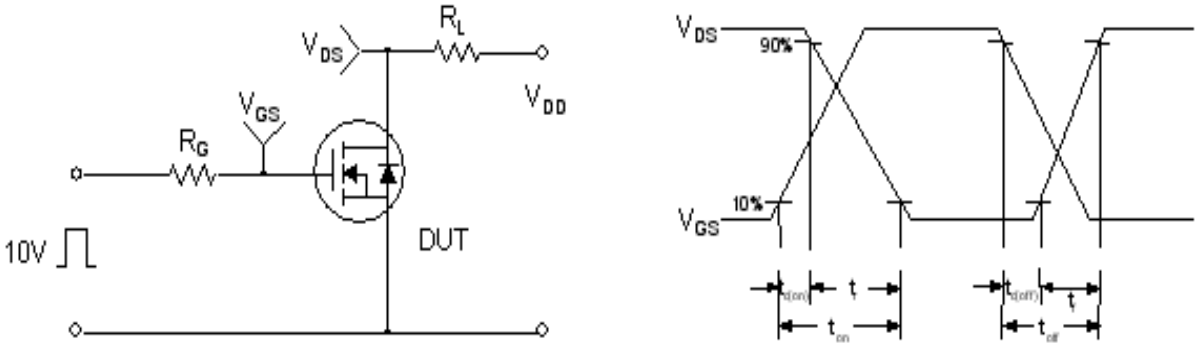
Figure 11. Transient Thermal Response Curve



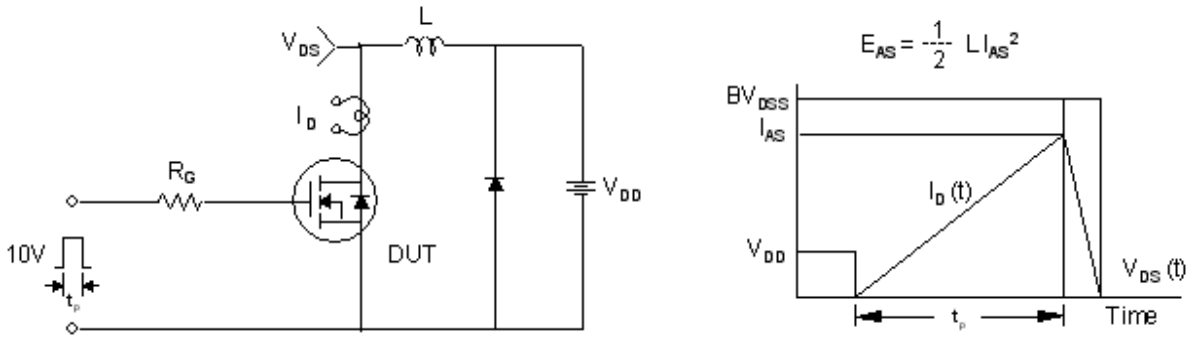
Gate Charge Test Circuit & Waveform



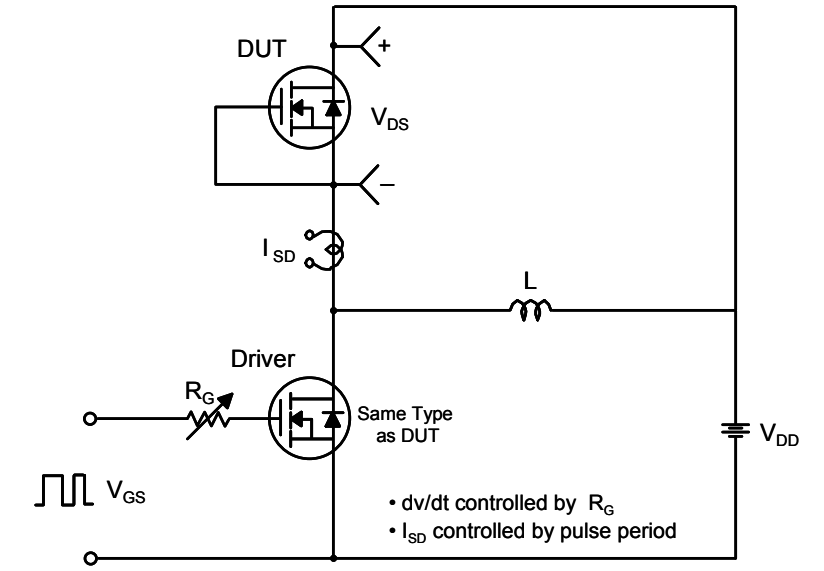
Resistive Switching Test Circuit & Waveforms

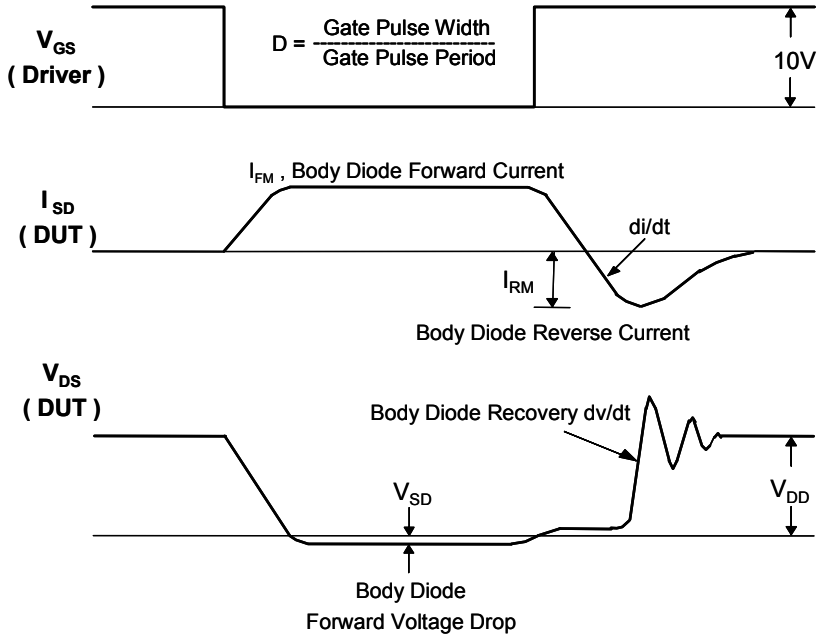


Unclamped Inductive Switching Test Circuit & Waveforms



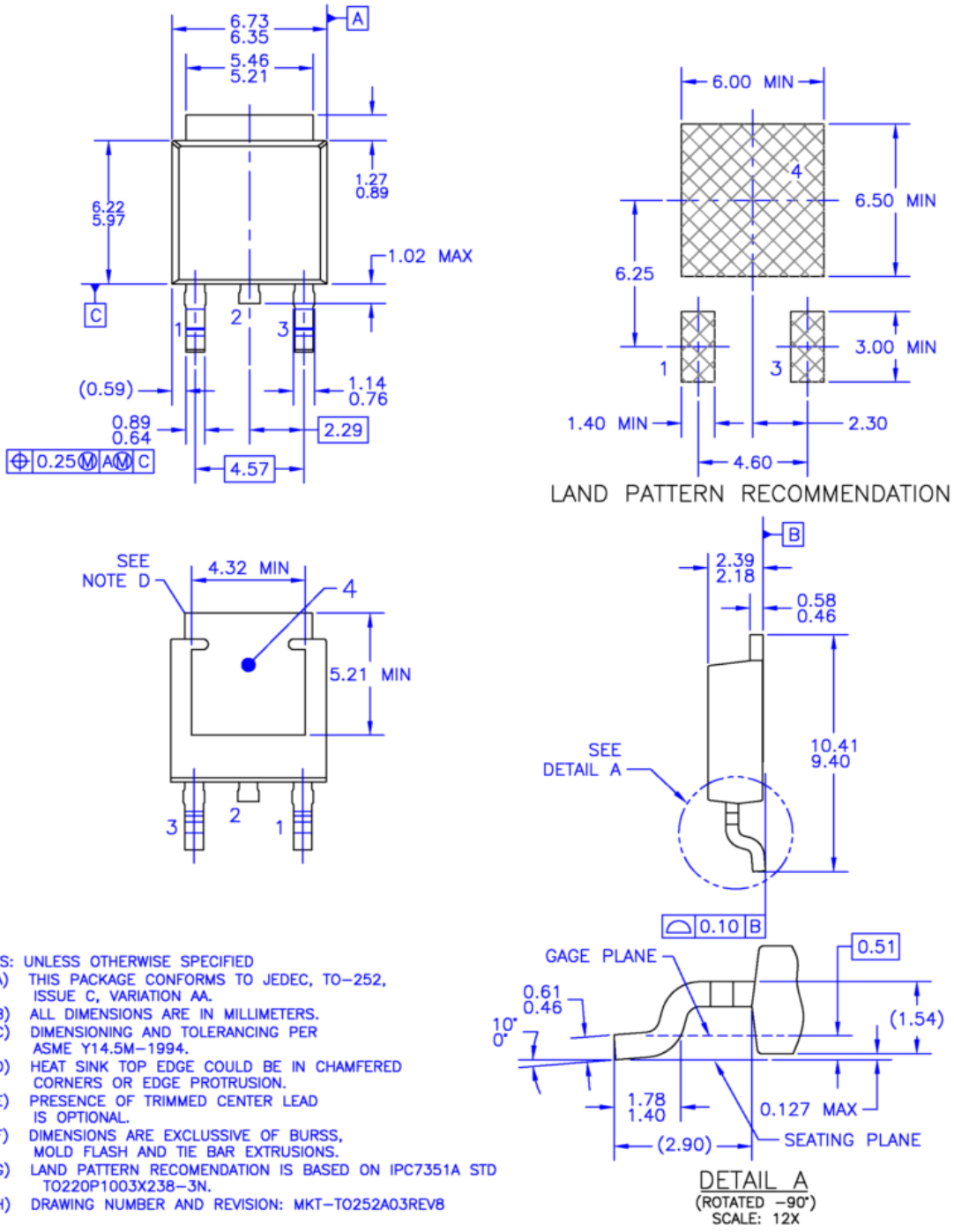
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I64