March 2015

# FDD6635

## 35V N-Channel PowerTrench® MOSFET

### General Description

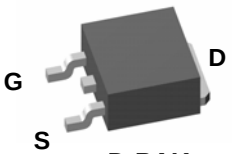
This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench technology to deliver low Rdson and optimized Bvdss capability to offer superior performance benefit in the applications.

### Applications

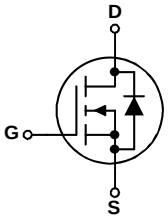
- Inverter
- Power Supplies

### Features

- 59 A, 35 V $R_{DS(ON)}$ = 10 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 13 mΩ @ $V_{GS}$ = 4.5 V
- Fast Switching
- RoHS compliant




D-PAK
(TO-252)




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 35 | V |
| $V_{DS(Avalanche)}$ | Drain-Source Avalanche Voltage (maximum) | (Note 4) | 40 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Continuous Drain Current @$T_C$=25°C | (Note 3) | 59 | A |
| | @$T_A$=25°C | (Note 1a) | 15 | |
| | Pulsed | (Note 1a) | 100 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | (Note 5) | 113 | mJ |
| $P_D$ | Power Dissipation @$T_C$=25°C | (Note 3) | 55 | W |
| | @$T_A$=25°C | (Note 1a) | 3.8 | |
| | @$T_A$=25°C | (Note 1b) | 1.6 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 2.7 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 96 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| FDD6635 | FDD6635 | D-PAK (TO-252) | 13'' | 16mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** (Note 2) | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 35 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | 32 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 28 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.9 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | –5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 15 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 13 A<br>$V_{GS}$ = 10 V, $I_D$ = 15 A, $T_J$=125°C | | 8.2<br>10.2<br>12.4 | 10<br>13<br>16 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 15 A | | 53 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1400 | | pF |
| $C_{oss}$ | Output Capacitance | | | 317 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 137 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 1.4 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 11 | 20 | ns |
| $t_r$ | Turn–On Rise Time | | | 6 | 12 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 28 | 45 | ns |
| $t_f$ | Turn–Off Fall Time | | | 14 | 25 | ns |
| $Q_{g\ (TOT)}$ | Total Gate Charge, $V_{GS}$ = 10V | $V_{DS}$ = 20 V, $I_D$ = 15 A | | 26 | 36 | nC |
| $Q_g$ | Total Gate Charge, $V_{GS}$ = 5V | | | 13 | 18 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 3.9 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 5.3 | | nC |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 15 A (Note 2) | | 0.8 | 1.2 | V |
| trr | Diode Reverse Recovery Time | IF = 15 A, diF/dt = 100 A/µs | | 26 | | ns |
| Qrr | Diode Reverse Recovery Charge | | | 16 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

**3.** Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where $P_D$ is maximum power dissipation at $T_C$ = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS}$ = 10V. Package current limitation is 21A

**4.** BV(avalanche) Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

**5.** Starting $T_J$ = 25°C, L = 1mH, $I_{AS}$ = 15A, $V_{DD}$ = 35V, $V_{GS}$ = 10V

## Typical Characteristics

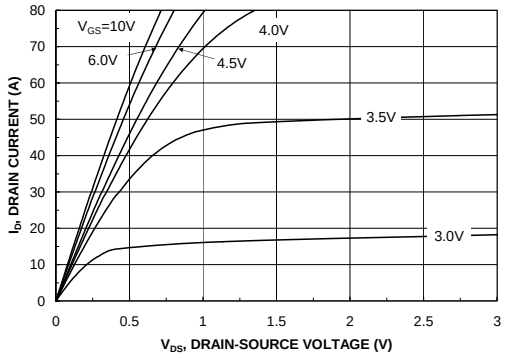



**Figure 1. On-Region Characteristics**

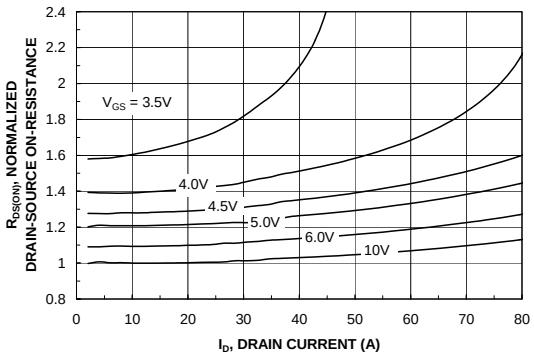



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage**

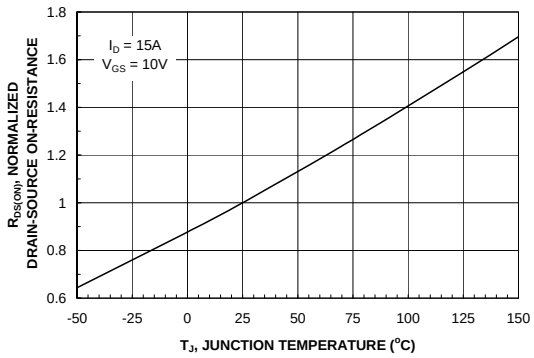



**Figure 3. On-Resistance Variation with Temperature**

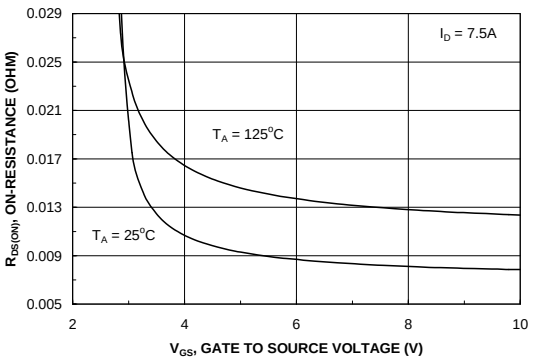



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage**

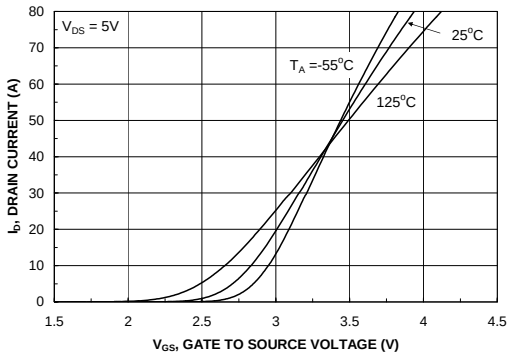



**Figure 5. Transfer Characteristics**

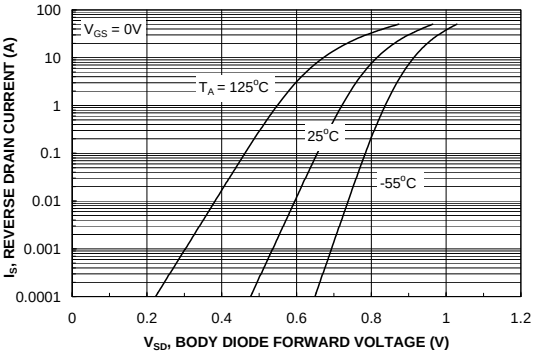



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## Typical Characteristics

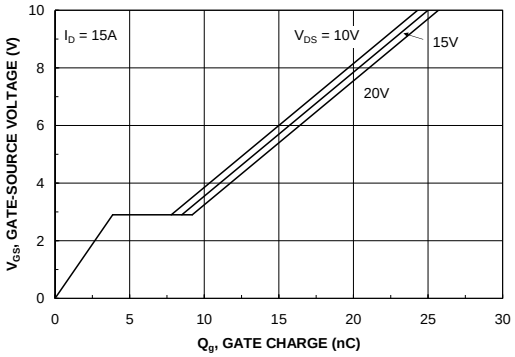



**Figure 7. Gate Charge Characteristics**

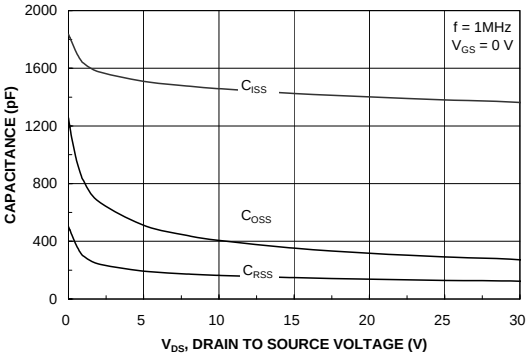



**Figure 8. Capacitance Characteristics**

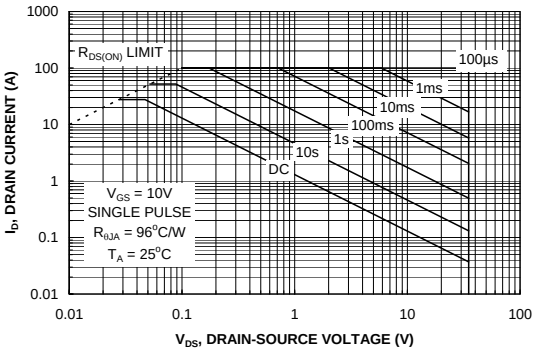



**Figure 9. Maximum Safe Operating Area**

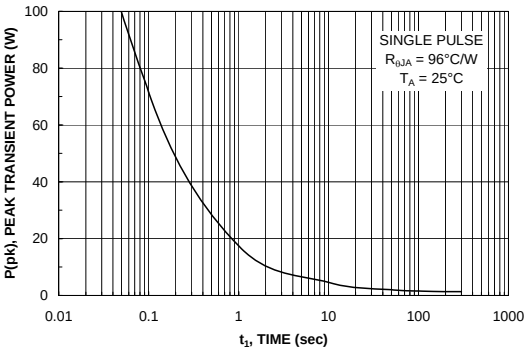



**Figure 10. Single Pulse Maximum Power Dissipation**

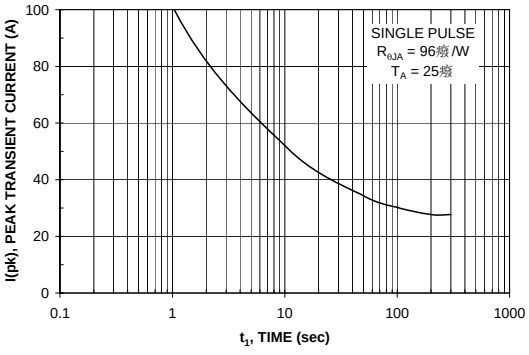



**Figure 11. Single Pulse Maximum Peak Current**

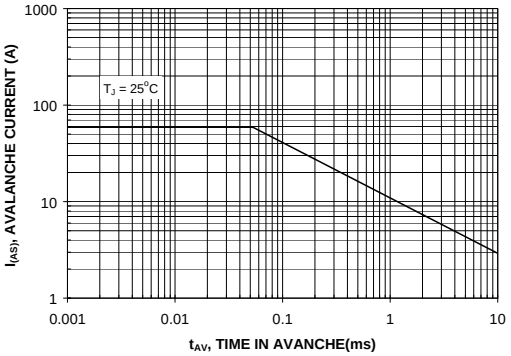



**Figure 12. Unclamped Inductive Switching Capability**

## Typical Characteristics

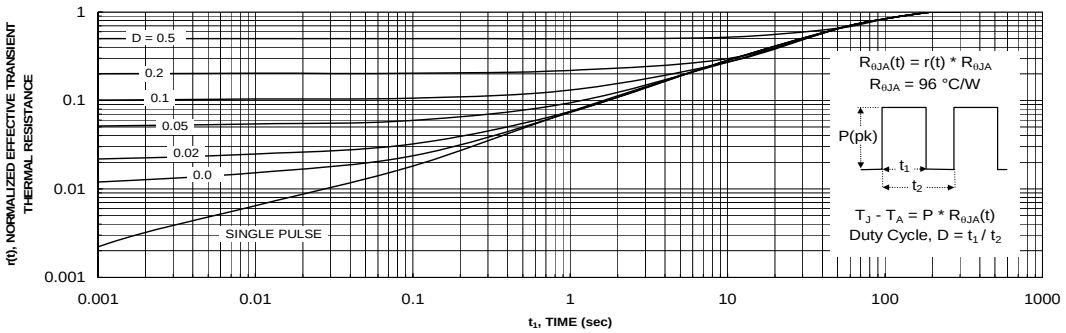



**Figure 13. Transient Thermal Response Curve**

**Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.**

## Test Circuits and Waveforms

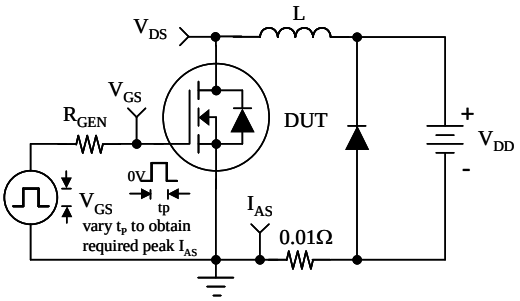



**Figure 14. Unclamped Inductive Load Test Circuit**

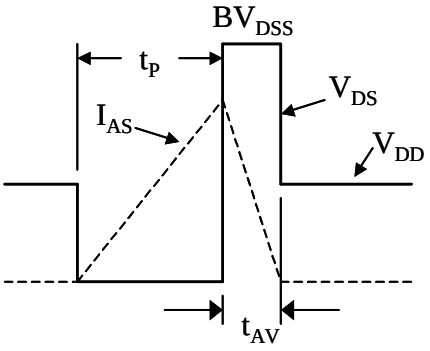



**Figure 15. Unclamped Inductive Waveforms**

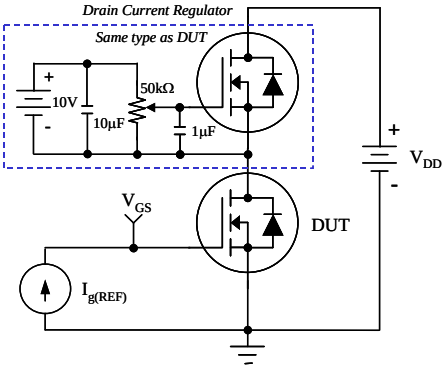



**Figure 16. Gate Charge Test Circuit**

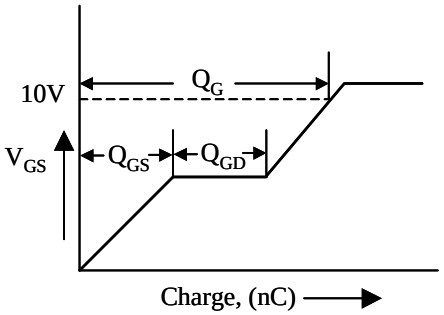



**Figure 17. Gate Charge Waveform**

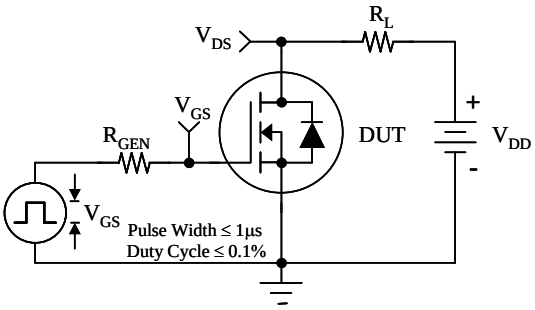



**Figure 18. Switching Time Test Circuit**

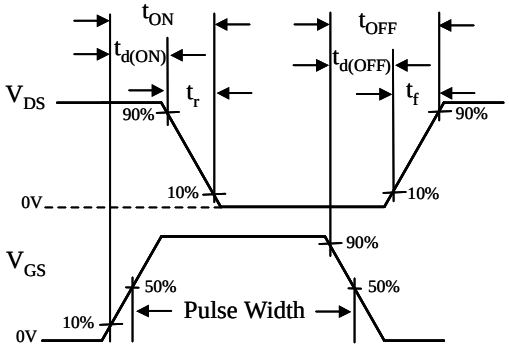
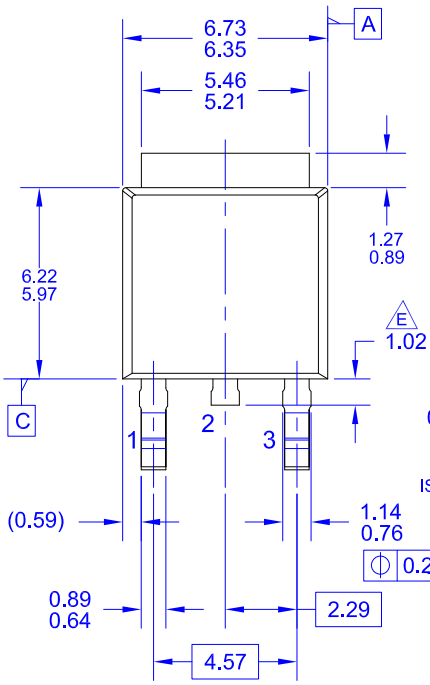
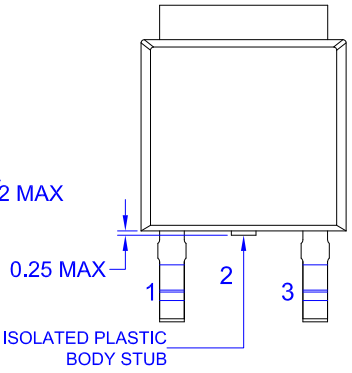


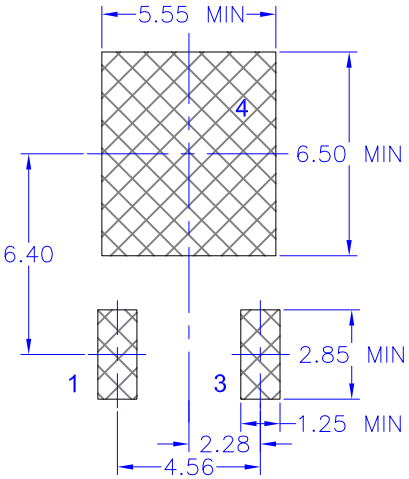

**Figure 19. Switching Time Waveforms**



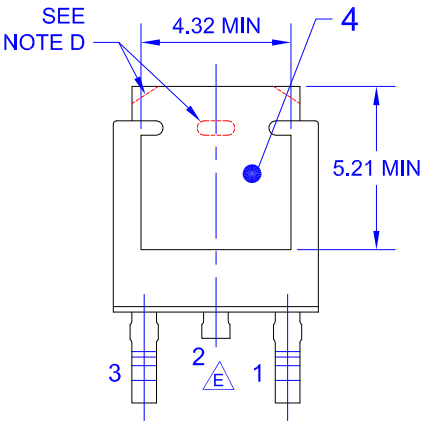

NON-DIODE PRODUCTS VERSION



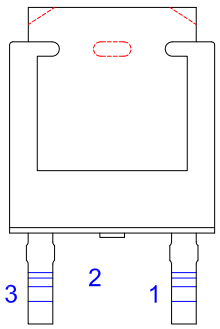

DIODE PRODUCTS VERSION




LAND PATTERN RECOMMENDATION




NON-DIODE PRODUCTS VERSION

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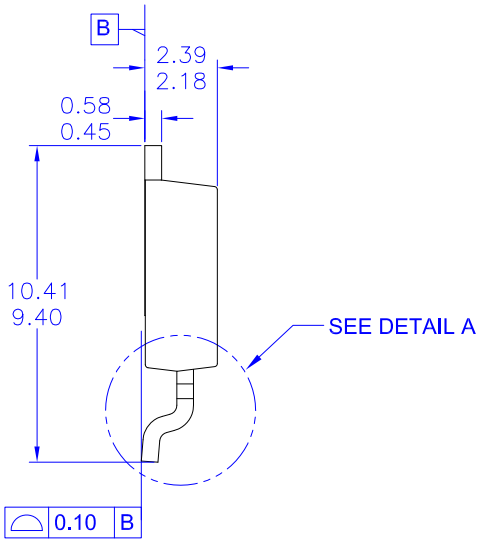
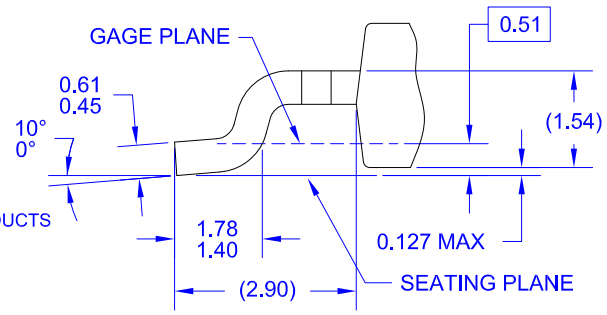



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11

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