



FDD6685

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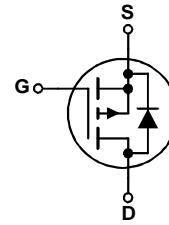
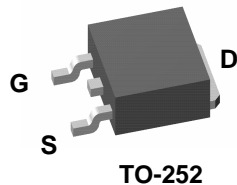
30V P-Channel PowerTrench[®] MOSFET

General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 25V).

Features

- -40 A, -30 V. $R_{DS(ON)} = 20\text{ m}\Omega @ V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 30\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Qualified to AEC Q101



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-30	V
V _{GSS}	Gate-Source Voltage	±25	V
I _D	Continuous Drain Current @ T _C =25°C (Note 3) @ T _A =25°C (Note 1a) Pulsed, PW ≤ 100µs (Note 1b)	-40	A
		-11	
		-100	
P _D	Power Dissipation for Single Operation (Note 1) (Note 1a) (Note 1b)	52	W
		3.8	
		1.6	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +175	°C

Thermal Characteristics

R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	2.9	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	°C/W

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at <http://www.aecouncil.com/>
Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDD6685	FDD6685	13"	16mm	2500 units

Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 4)

E_{AS}	Single Pulse Drain-Source Avalanche Energy	$I_D = -11\text{ A}$		42		mJ
I_{AS}	Maximum Drain-Source Avalanche Current			-11		A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-24		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -11\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -9\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -11\text{ A}, T_J = 125^\circ\text{C}$		14 21 20	20 30	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-20			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -11\text{ A}$		26		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1715		pF
C_{oss}	Output Capacitance			440		pF
C_{rss}	Reverse Transfer Capacitance			225		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		3.6		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		17	31	ns
t_r	Turn-On Rise Time			11	21	ns
$t_{d(off)}$	Turn-Off Delay Time			43	68	ns
t_f	Turn-Off Fall Time			21	34	ns
Q_g	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -11\text{ A},$ $V_{GS} = -5\text{ V}$		17	24	nC
Q_{gs}	Gate-Source Charge			9		nC
Q_{gd}	Gate-Drain Charge			4		nC

Drain-Source Diode Characteristics and Maximum Ratings

V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -3.2\text{ A}$ (Note 2)		-0.8	-1.2	V
T_{rr}	Diode Reverse Recovery Time	$I_F = -11\text{ A},$ $diF/dt = 100\text{ A}/\mu\text{s}$		26		ns
Q_{rr}	Diode Reverse Recovery Charge			13		nC

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted on a 1in^2 pad of 2 oz copper



b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$

- Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(on)}}}$ where P_D is maximum power dissipation at $T_C = 25^\circ\text{C}$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10\text{V}$.

- Starting $T_J = 25^\circ\text{C}$, $L = 0.69\text{mH}$, $I_{AS} = -11\text{A}$

Typical Characteristics

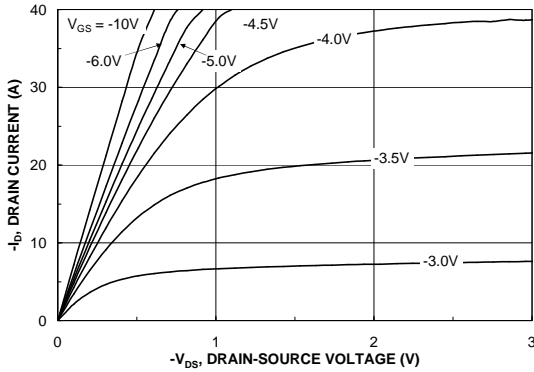


Figure 1. On-Region Characteristics.

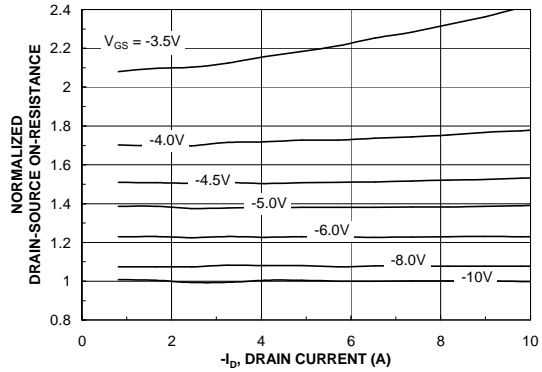


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

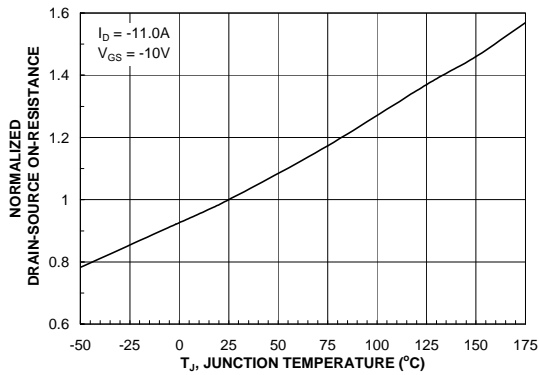


Figure 3. On-Resistance Variation with Temperature.

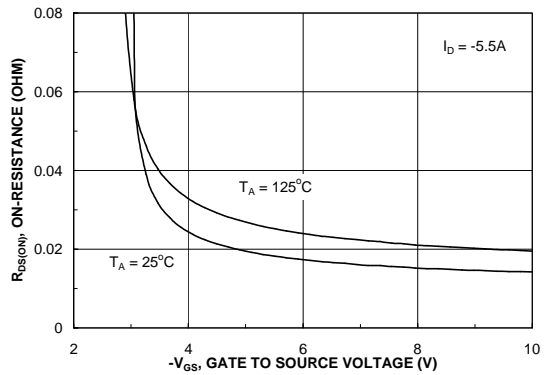


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

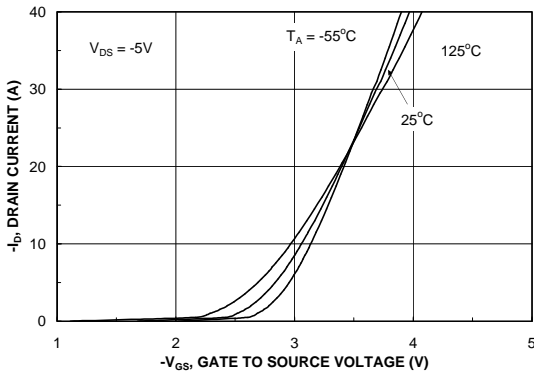


Figure 5. Transfer Characteristics.

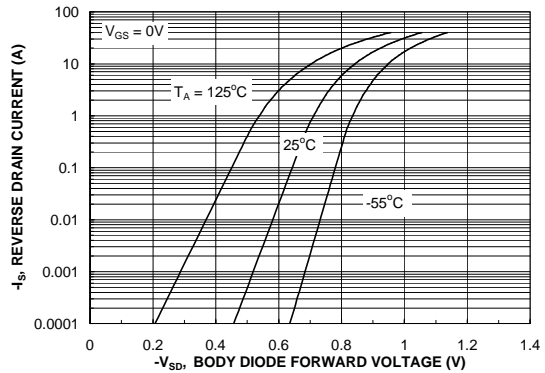


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

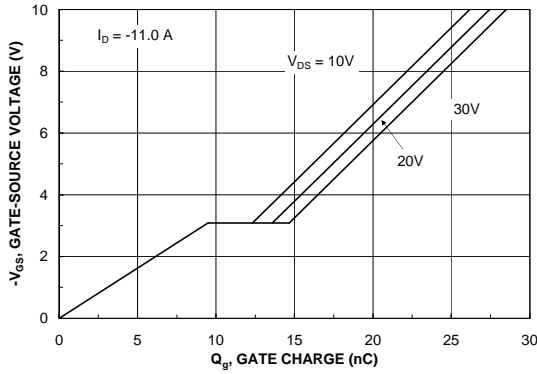


Figure 7. Gate Charge Characteristics.

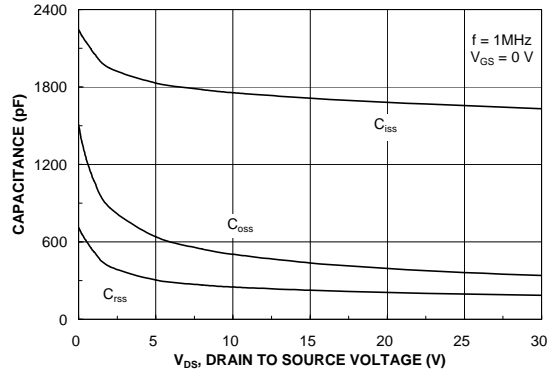


Figure 8. Capacitance Characteristics.

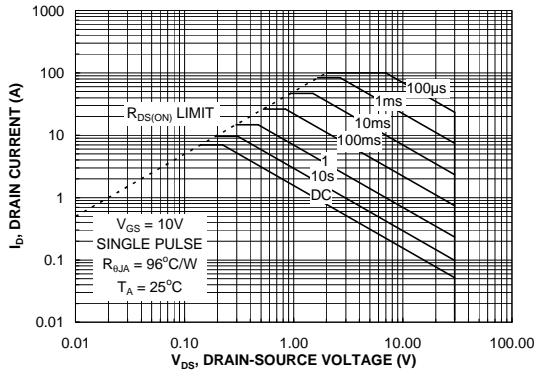


Figure 9. Maximum Safe Operating Area.

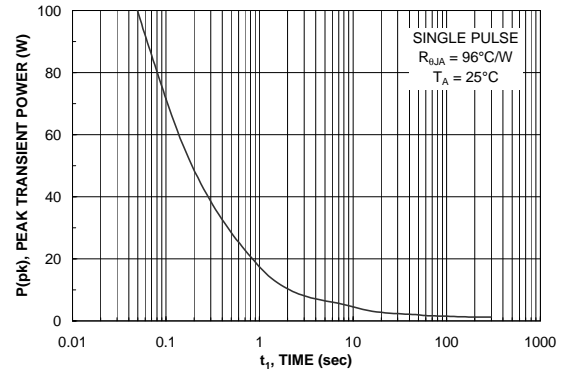


Figure 10. Single Pulse Maximum Power Dissipation.

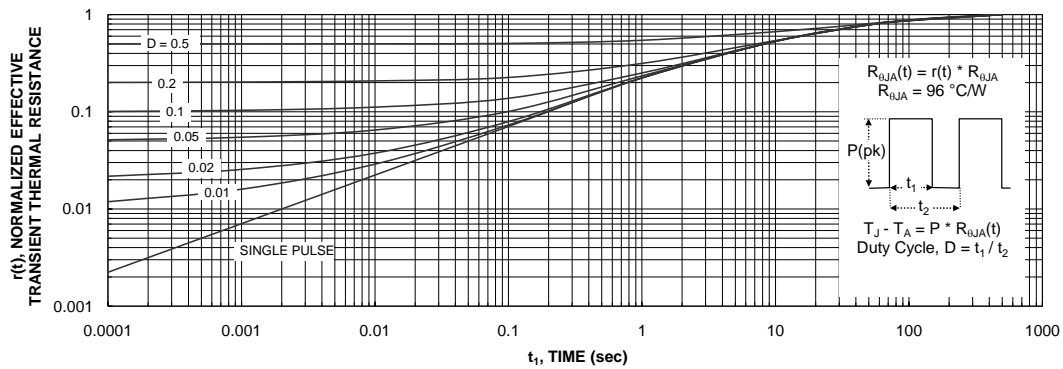


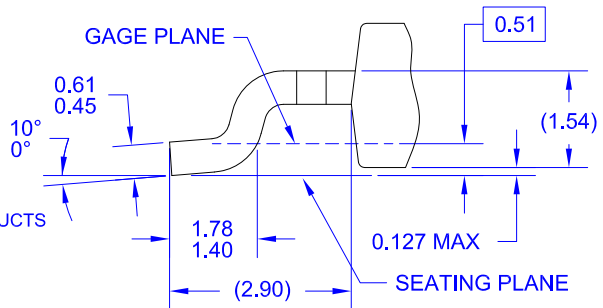
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X





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