

**FAIRCHILD**  
SEMICONDUCTOR®

August 2009

## FDG1024NZ

### Dual N-Channel PowerTrench® MOSFET 20 V, 1.2 A, 175 mΩ

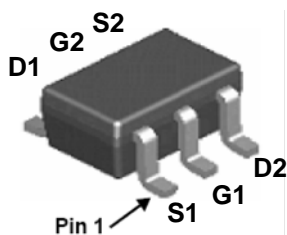
#### Features

- Max  $r_{DS(on)}$  = 175 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 1.2$  A
- Max  $r_{DS(on)}$  = 215 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 1.0$  A
- Max  $r_{DS(on)}$  = 270 mΩ at  $V_{GS} = 1.8$  V,  $I_D = 0.9$  A
- Max  $r_{DS(on)}$  = 389 mΩ at  $V_{GS} = 1.5$  V,  $I_D = 0.8$  A
- HBM ESD protection level >2 kV (Note 3)
- Very low level gate drive requirements allowing operation in 3 V circuits ( $V_{GS(th)} < 1.5$  V)
- Very small package outline SC70-6
- RoHS Compliant

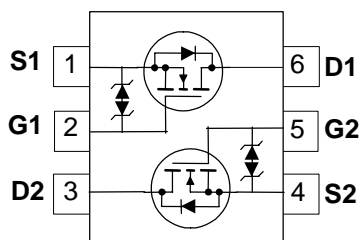


#### General Description

This dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.



SC70-6



#### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	$\pm 8$	V
$I_D$	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	1.2
	-Pulsed		6
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	0.36
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	0.30
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	350	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	415	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.24	FDG1024NZ	SC70-6	7"	8 mm	3000 units

FDG1024NZ Dual N-Channel Power Trench® MOSFET

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		14		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\ \text{V}$ , $V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\ \text{V}$ , $V_{DS} = 0\ \text{V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	0.4	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\ \text{V}$ , $I_D = 1.2\ \text{A}$		160	175	m $\Omega$
		$V_{GS} = 2.5\ \text{V}$ , $I_D = 1.0\ \text{A}$		185	215	
		$V_{GS} = 1.8\ \text{V}$ , $I_D = 0.9\ \text{A}$		232	270	
		$V_{GS} = 1.5\ \text{V}$ , $I_D = 0.8\ \text{A}$		321	389	
		$V_{GS} = 4.5\ \text{V}$ , $I_D = 1.2\ \text{A}$ , $T_J = 125\text{ }^\circ\text{C}$		220	259	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\ \text{V}$ , $I_D = 1.2\ \text{A}$		4		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$		115	150	pF
$C_{oss}$	Output Capacitance			25	35	pF
$C_{rss}$	Reverse Transfer Capacitance			20	25	pF
$R_g$	Gate Resistance			4.6		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\ \text{V}$ , $I_D = 1.2\ \text{A}$ , $V_{GS} = 4.5\ \text{V}$ , $R_{GEN} = 6\ \Omega$		3.7	10	ns
$t_r$	Rise Time			1.7	10	ns
$t_{d(off)}$	Turn-Off Delay Time			11	19	ns
$t_f$	Fall Time			1.5	10	ns
$Q_g$	Total Gate Charge		$V_{GS} = 4.5\ \text{V}$ , $V_{DD} = 10\ \text{V}$ , $I_D = 1.2\ \text{A}$		1.8	2.6
$Q_{gs}$	Gate to Source Charge			0.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.4		nC

**Drain-Source Diode Characteristics**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			0.3	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = 0.3\ \text{A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 1.2\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$		10	20	ns
$Q_{rr}$	Reverse Recovery Charge			1.9	10	nC

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a. 350  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

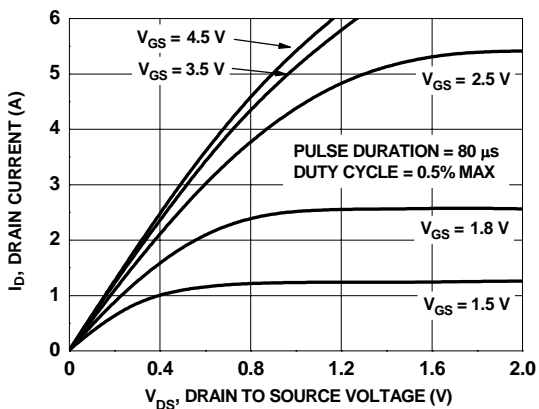


b. 415  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

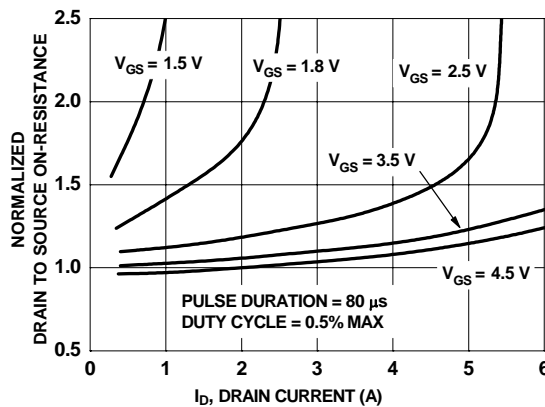
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

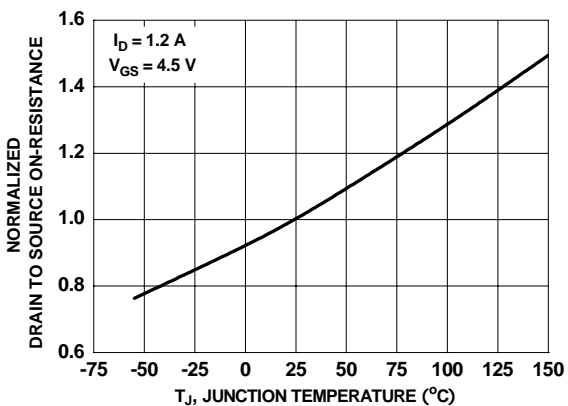
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



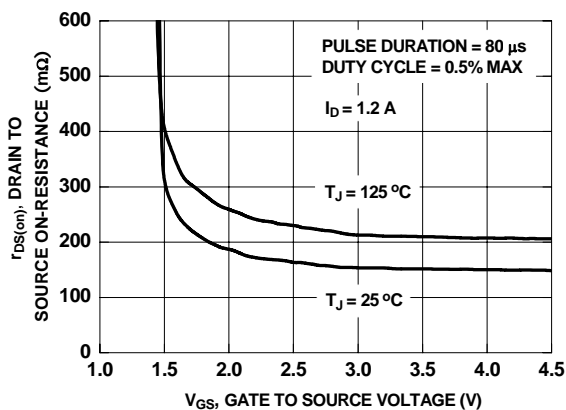
**Figure 1. On-Region Characteristics**



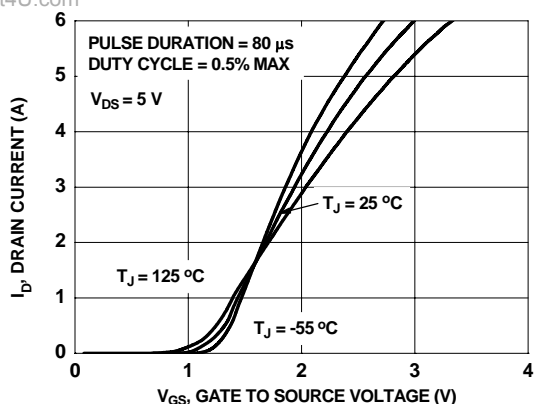
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



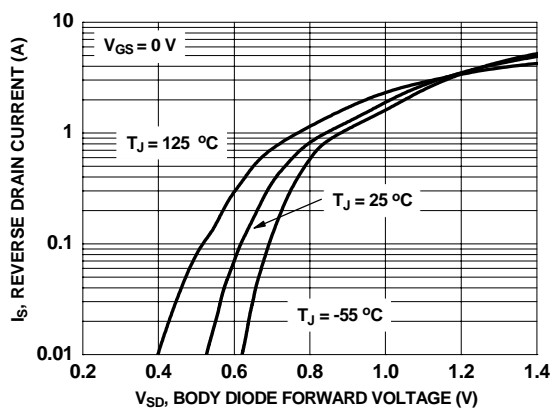
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**



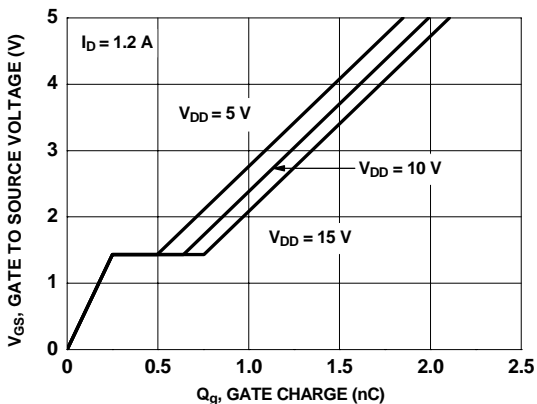
**Figure 5. Transfer Characteristics**



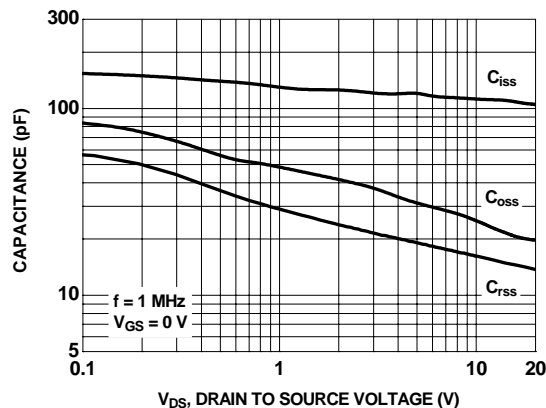
**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

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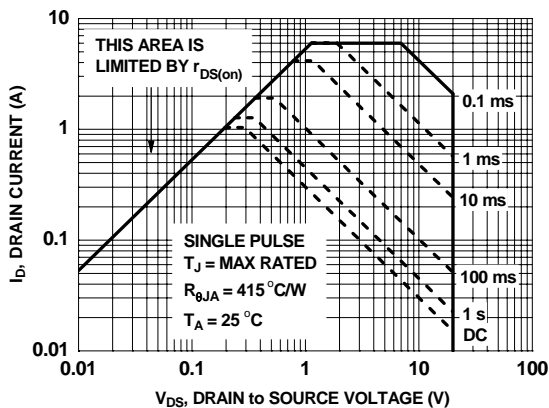
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



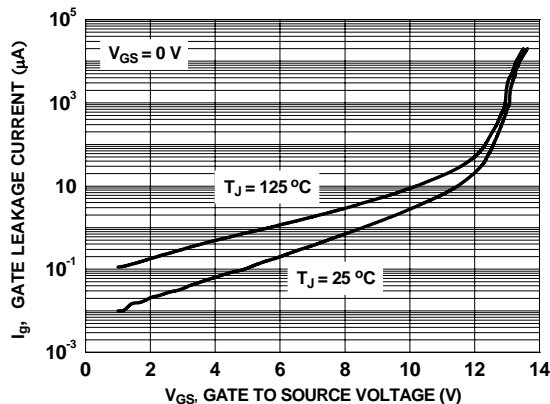
**Figure 7. Gate Charge Characteristics**



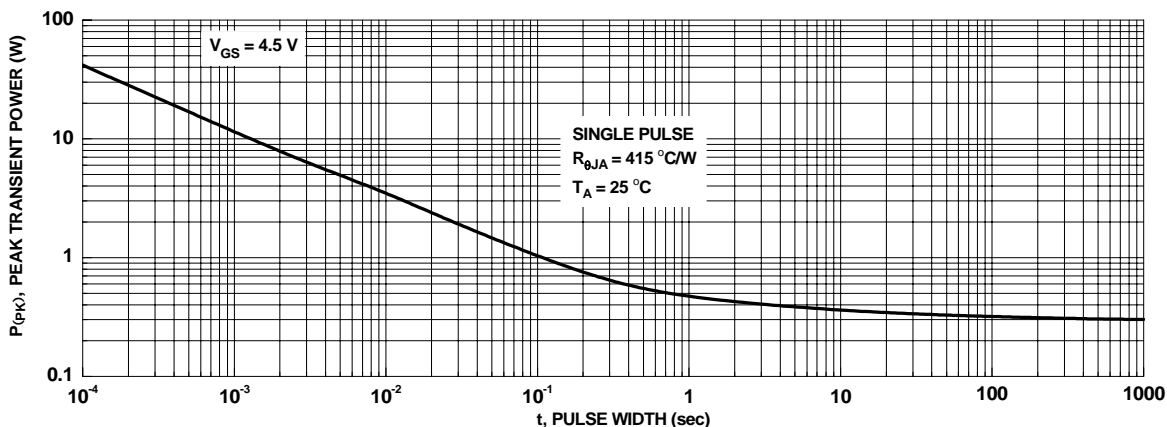
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

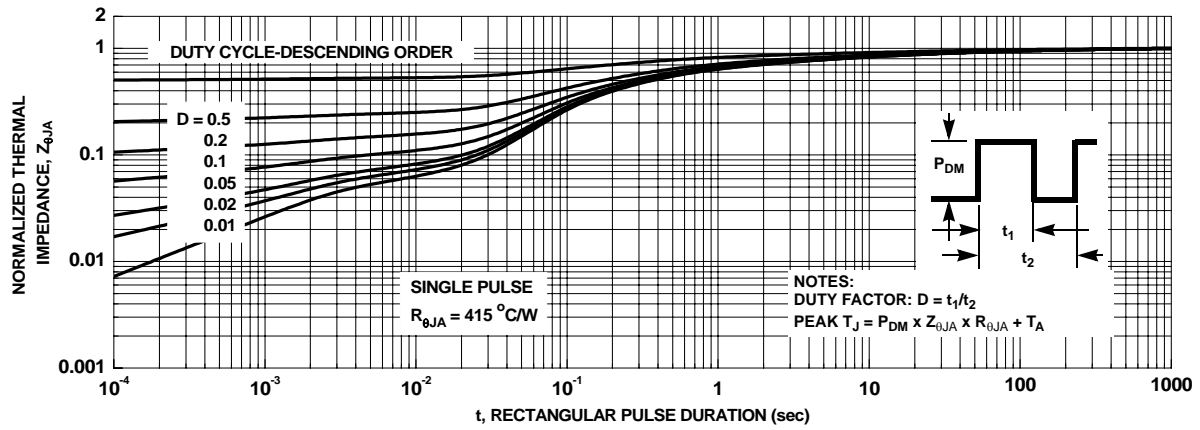


**Figure 10. Gate Leakage Current vs Gate to Source Voltage**



**Figure 11. Single Pulse Maximum Power Dissipation**

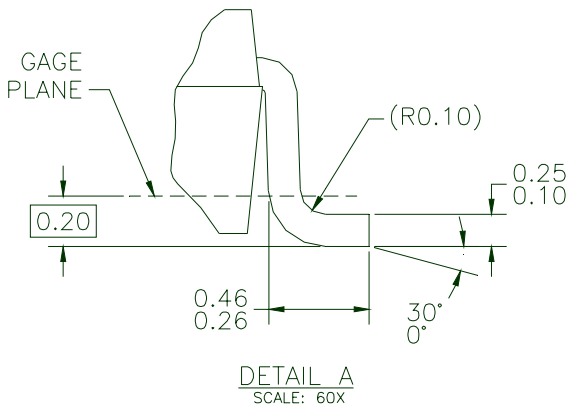
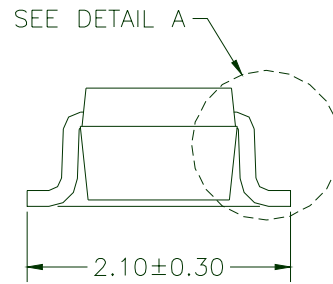
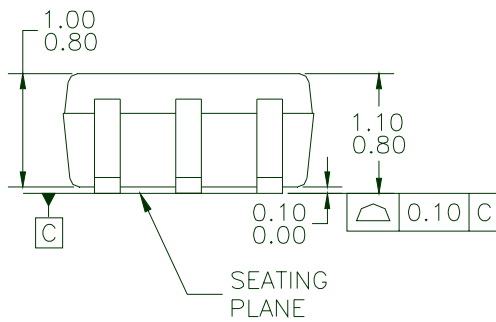
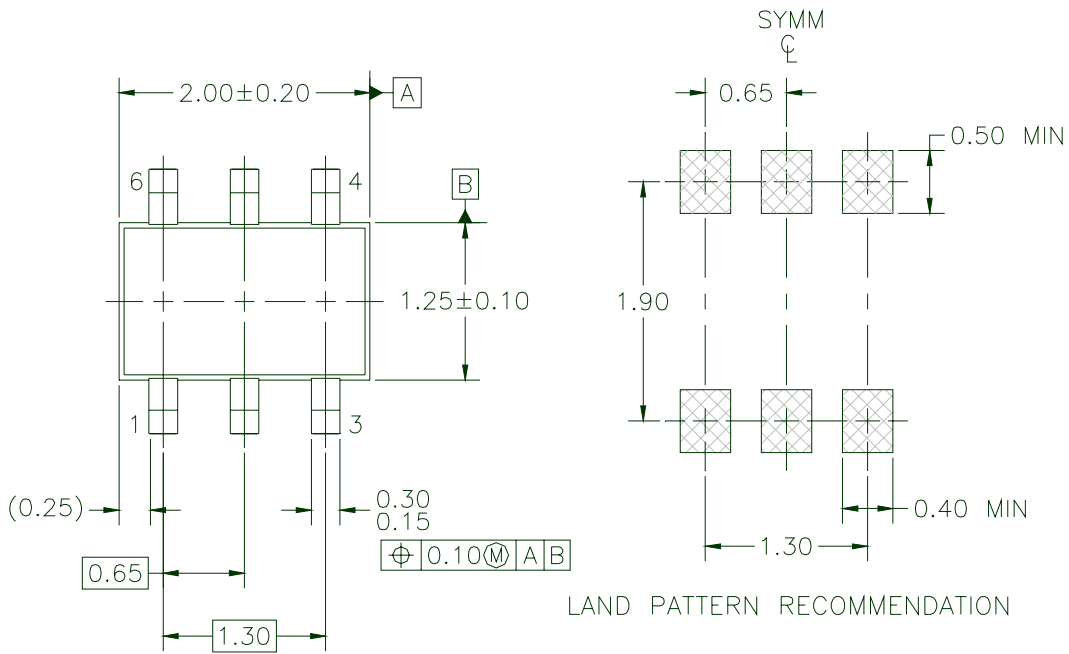
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Transient Thermal Response Curve**

FDG1024NZ Dual N-Channel Power Trench<sup>®</sup> MOSFET

**Dimensional Outline and Pad Layout**



NOTES: UNLESS OTHERWISE SPECIFIED







- A) THIS PACKAGE CONFORMS TO EIAJ SC-88, 1996.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

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| EfficientMax™  | ISOPLANAR™  | SmartMax™  | TinyPWM™  |
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