

FDH45N50F

N-Channel UniFET™ FRFET® MOSFET

500 V, 45 A, 120 mΩ

Features

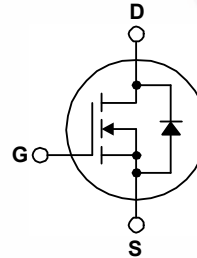
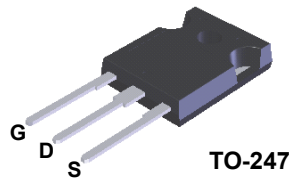
- $R_{DS(on)} = 105 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 22.5 \text{ A}$
- Low Gate Charge (Typ. 105 nC)
- Low C_{rss} (Typ. 62 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability

Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FDH45N50F_F133	Unit
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	45	A
		- Continuous ($T_C = 100^\circ\text{C}$)	28.4	A
I_{DM}	Drain Current	- Pulsed (Note 1)	180	A
V_{GSS}	Gate-Source voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1868	mJ
I_{AR}	Avalanche Current (Note 1)		45	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		50	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	625	W
		- Derate Above 25°C	5	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDH45N50F_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDH45N50F_F133	FDH45N50F	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.5	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	25 250	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 22.5\text{ A}$	--	0.105	0.12	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 22.5\text{ A}$	--	49.0	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	--	5100	6630	pF
C_{oss}	Output Capacitance		--	790	1030	pF
C_{rSS}	Reverse Transfer Capacitance		--	62	--	pF
C_{oss}	Output Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	--	161	--	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	--	342	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 48\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	--	140	290	ns
t_r	Turn-On Rise Time		--	500	1010	ns
$t_{d(off)}$	Turn-Off Delay Time		--	215	440	ns
t_f	Turn-Off Fall Time		(Note 4)	--	245	500
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 48\text{ A},$ $V_{GS} = 10\text{ V}$	--	105	137	nC
Q_{gs}	Gate-Source Charge		--	33	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	45	--
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	45	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	180	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 45\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 45\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$	--	188	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.64	--	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 1.46\text{ mH}, I_{AS} = 48\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 45\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

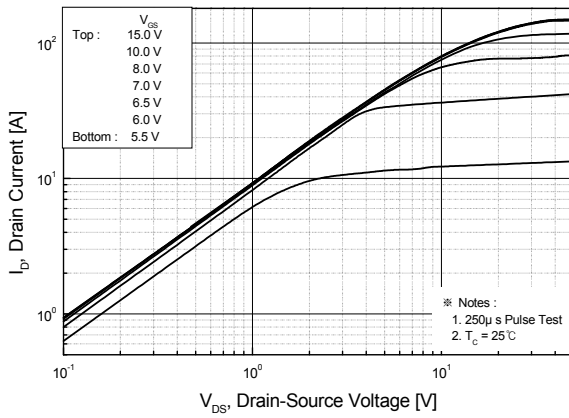


Figure 2. Transfer Characteristics

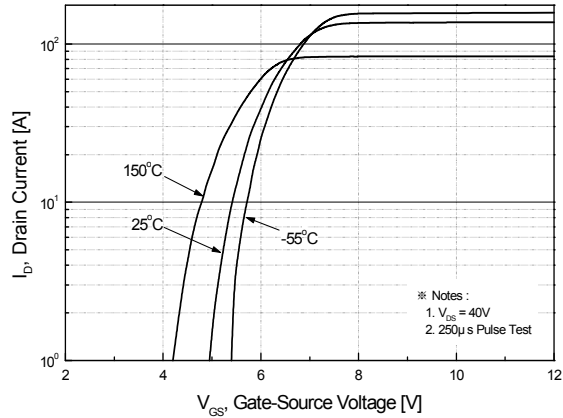


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

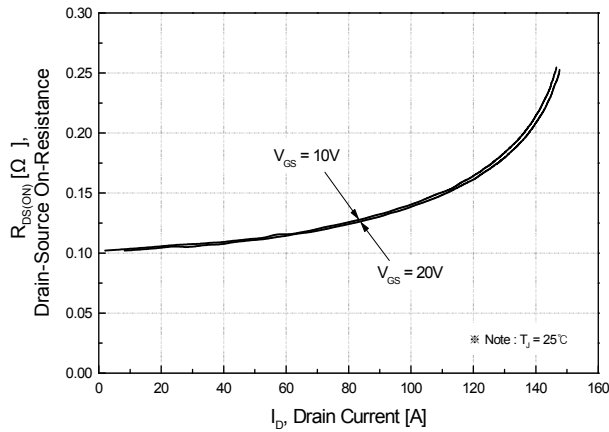


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

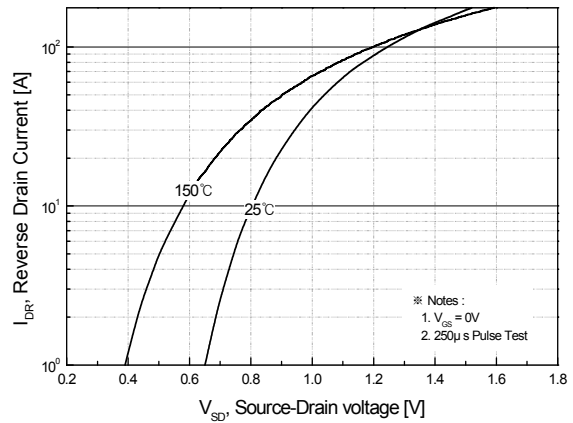


Figure 5. Capacitance Characteristics

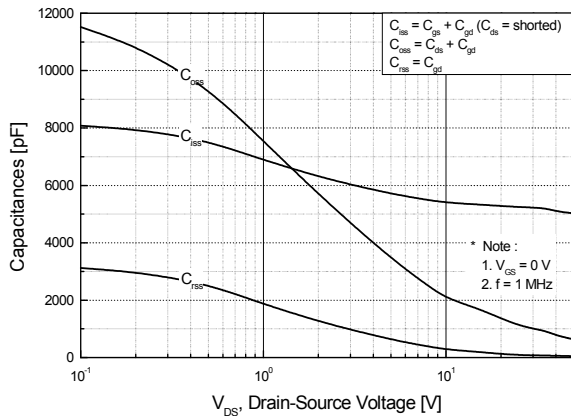
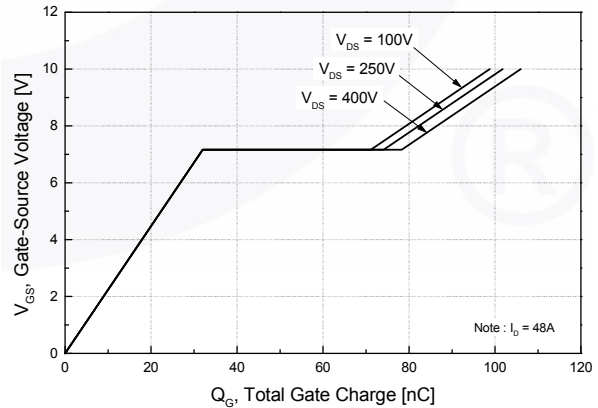


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

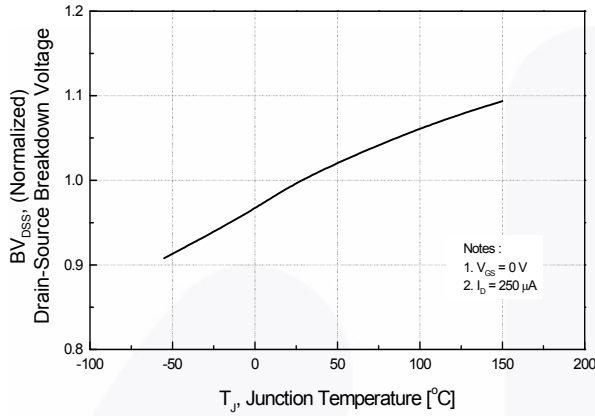


Figure 8. On-Resistance Variation vs. Temperature

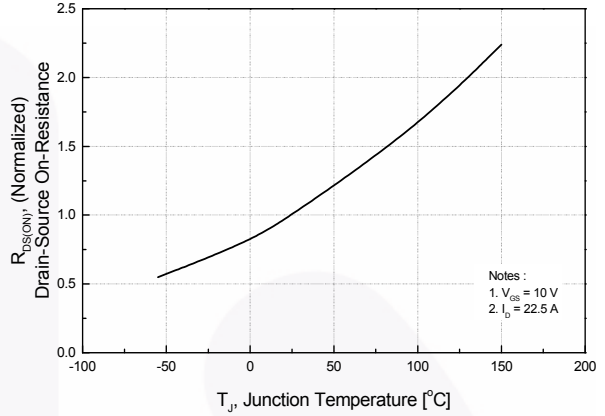


Figure 9. Maximum Safe Operating Area

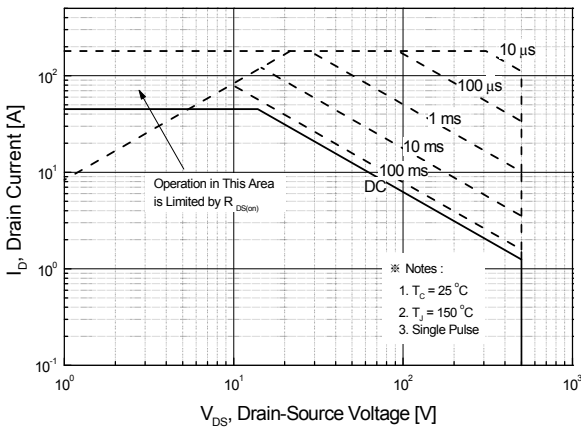


Figure 10. Maximum Drain Current vs. Case Temperature

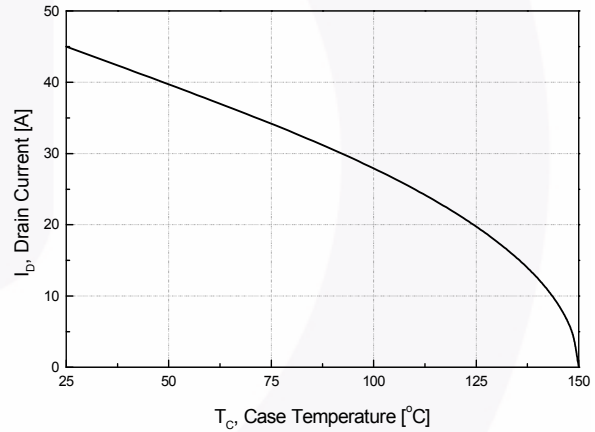


Figure 11. Typical Drain Current Slope vs. Gate Resistance

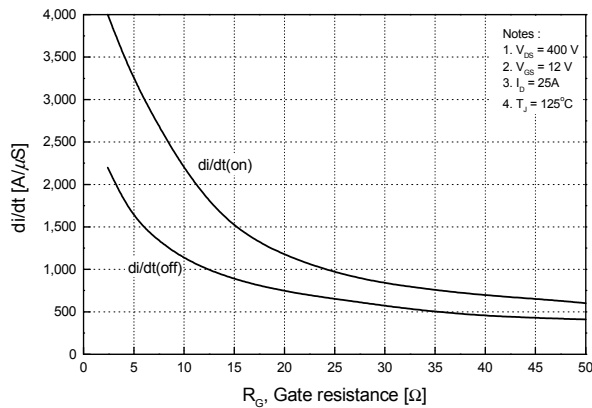
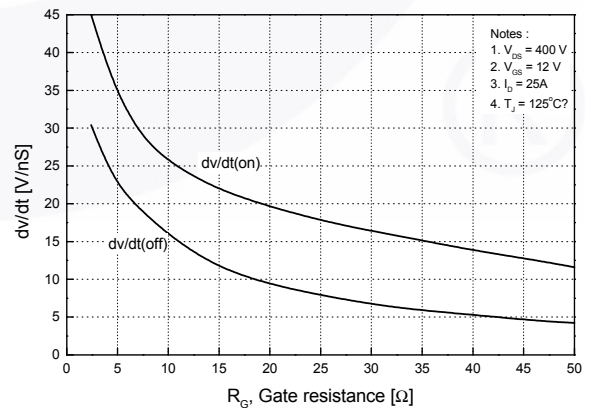


Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance



Typical Performance Characteristics (Continued)

Figure 13. Typical Switching Losses vs. Gate Resistance

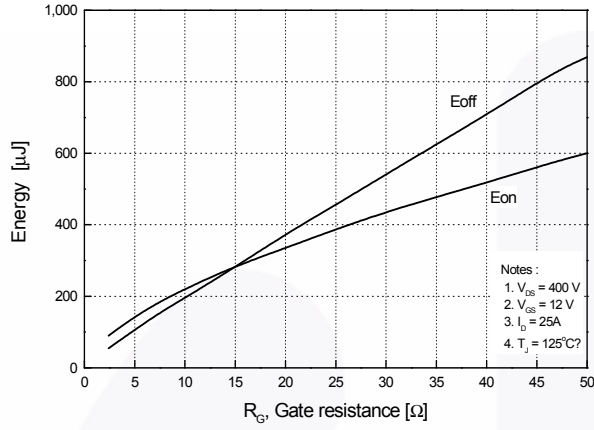


Figure 14. Unclamped Inductive Switching Capability

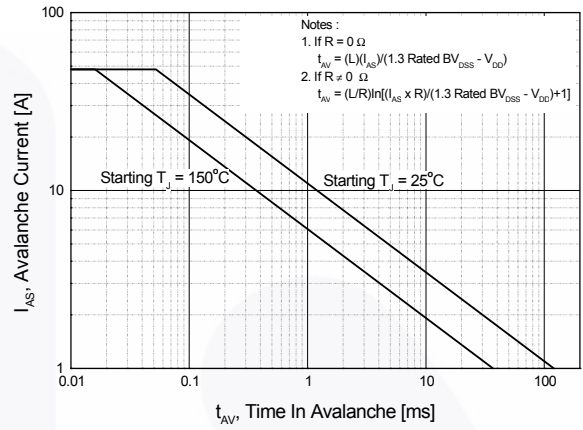
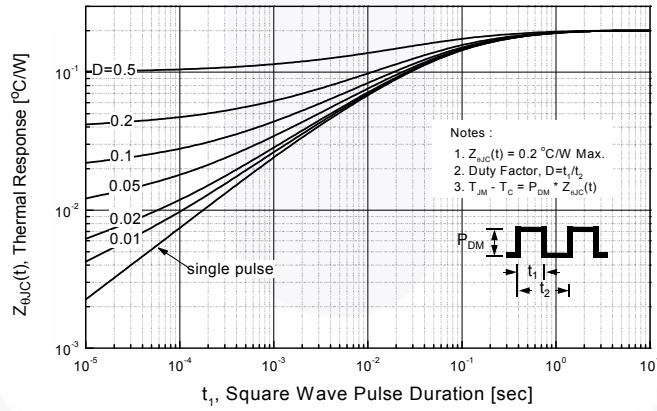


Figure 15. Transient Thermal Resistance Curve



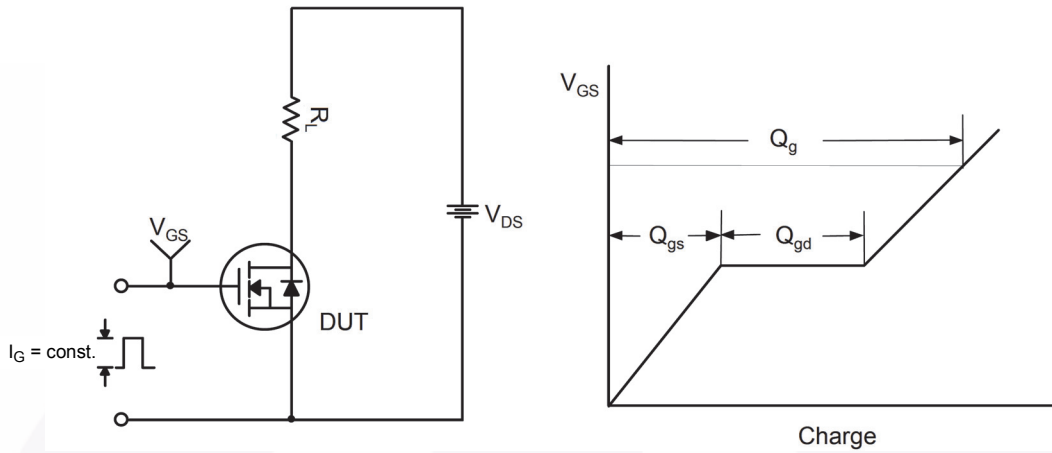


Figure 16. Gate Charge Test Circuit & Waveform



Figure 17. Resistive Switching Test Circuit & Waveforms



Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms

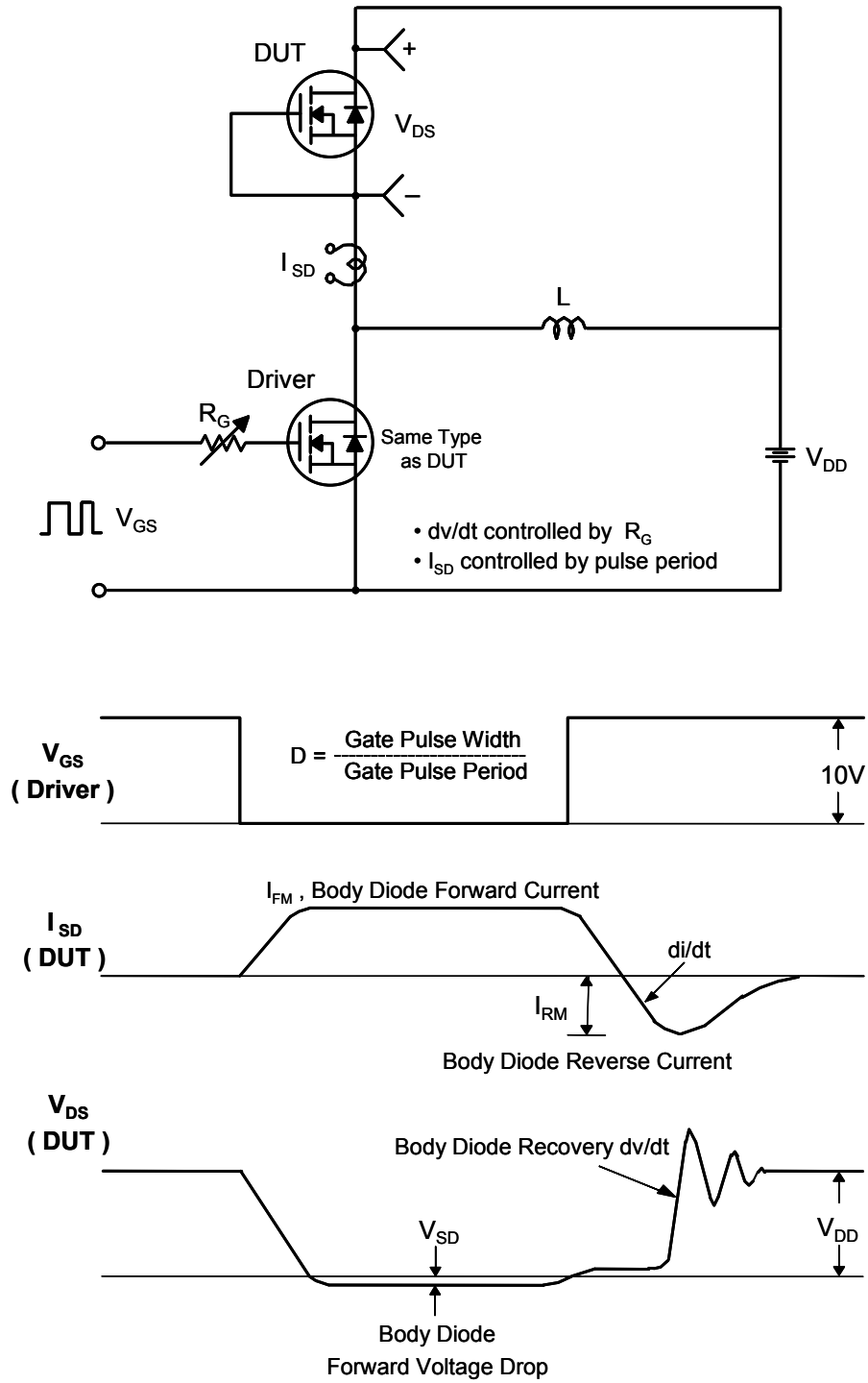
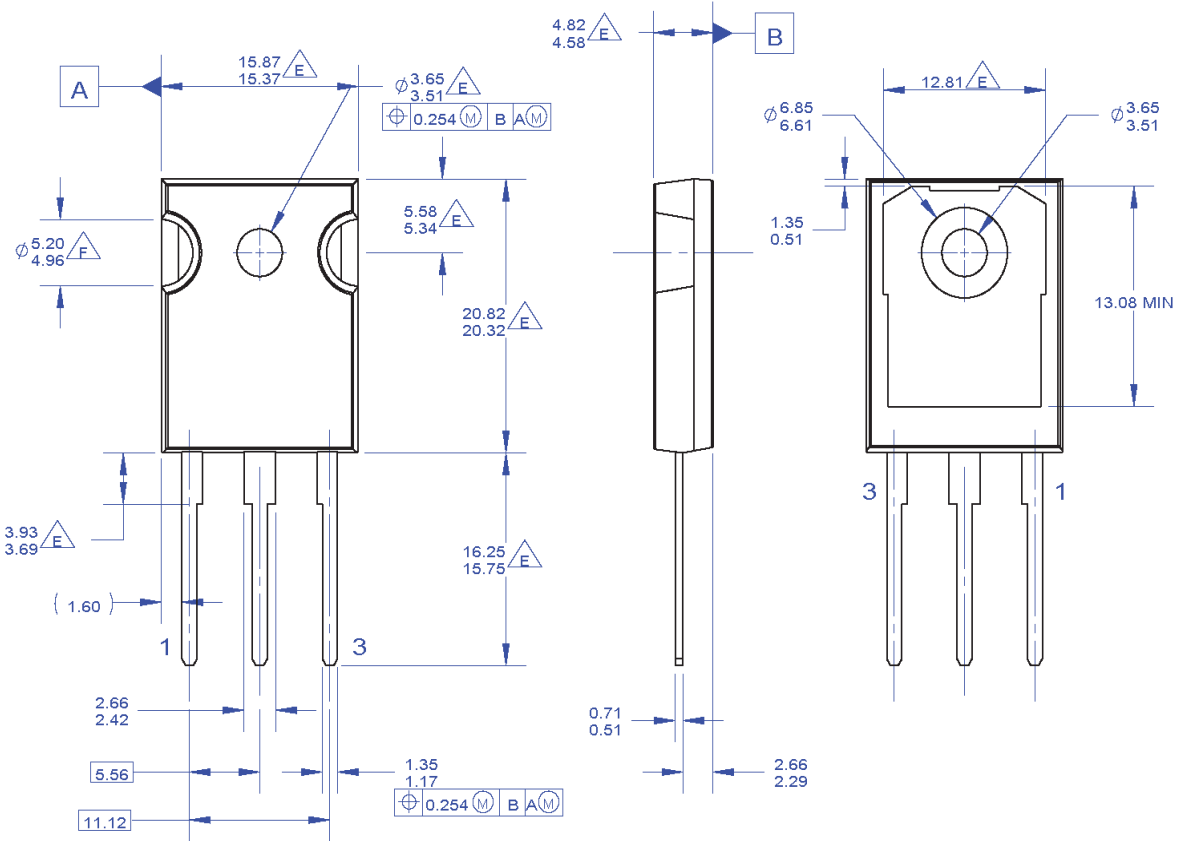


Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

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- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

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Figure 20. TO-247, Molded, 3-Lead, Jedec Variation AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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