

FDP045N10A / FDI045N10A

N-Channel PowerTrench® MOSFET

100 V, 164 A, 4.5 mΩ

Features

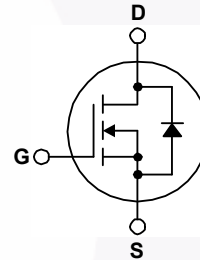
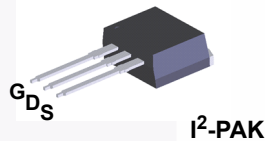
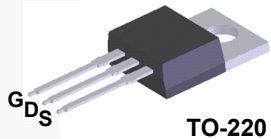
- $R_{DS(on)} = 3.8 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- Fast Switching Speed
- Low Gate Charge, $Q_G = 54 \text{ nC}$ (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP045N10A_F102 FDI045N10A_F102	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	164*
		- Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	116
		- Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	120
I_{DM}	Drain Current	- Pulsed (Note 1)	656
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	637
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	263
		- Derate Above 25°C	1.75
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP045N10A_F102 FDI045N10A_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.57	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP045N10A_F102	FDP045N10A	TO-220	Tube	N/A	N/A	50 units
FDI045N10A_F102	FDI045N10A	I ² -PAK	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.07	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 80 \text{ V}, T_C = 150^\circ\text{C}$	-	-	1 500	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 100 \text{ A}$	-	3.8	4.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 100 \text{ A}$	-	132	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$	-	3960	5270	pF
C_{oss}	Output Capacitance		-	925	1230	pF
C_{rss}	Reverse Transfer Capacitance		-	34	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	1520	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10 \text{ V}, V_{DS} = 50 \text{ V},$ $I_D = 100 \text{ A}$	-	54	74	nC
Q_{gs}	Gate to Source Gate Charge		-	17	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	13	-
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	1.9	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 100 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	23	56	ns
t_r	Turn-On Rise Time		-	26	62	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	110	ns
t_f	Turn-Off Fall Time		(Note 4)	-	15	40

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	164*	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	656	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 100 \text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DD} = 50 \text{ V}, I_{SD} = 100 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	75	-	ns
Q_{rr}	Reverse Recovery Charge		-	120	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 3 \text{ mH}, I_{AS} = 20.6 \text{ A}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

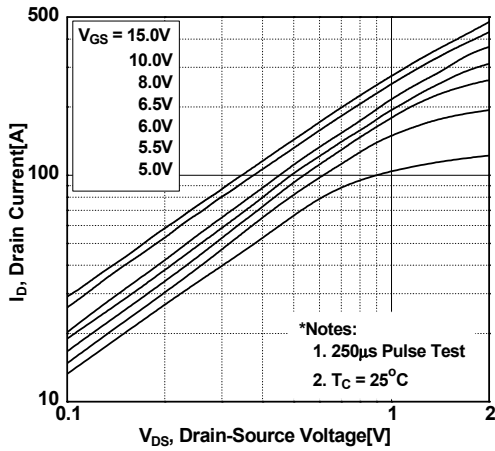


Figure 2. Transfer Characteristics

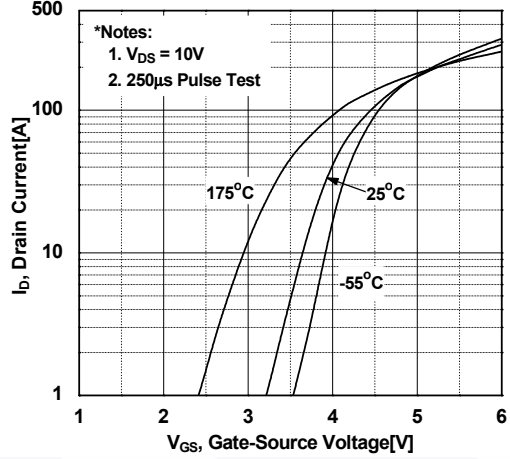


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

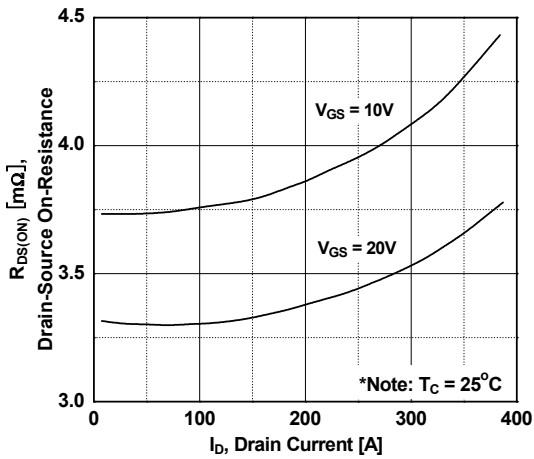


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

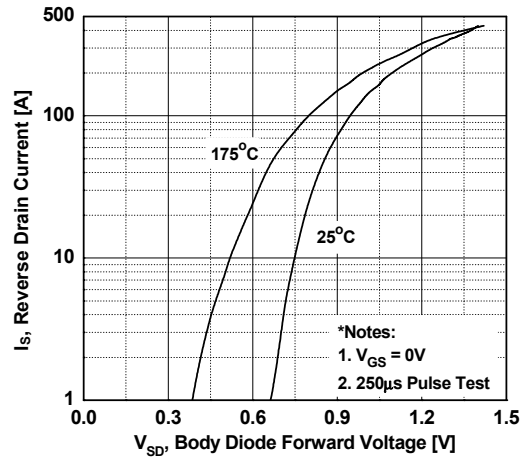


Figure 5. Capacitance Characteristics

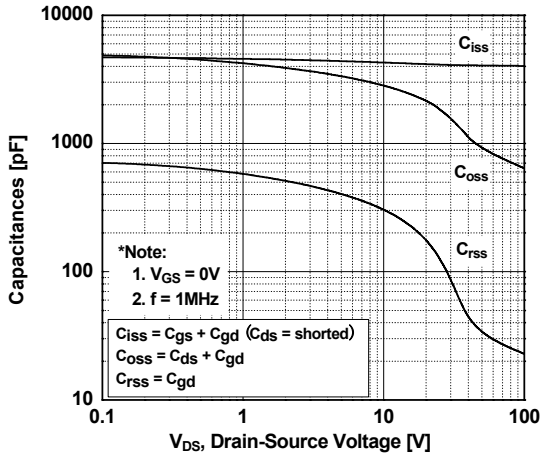
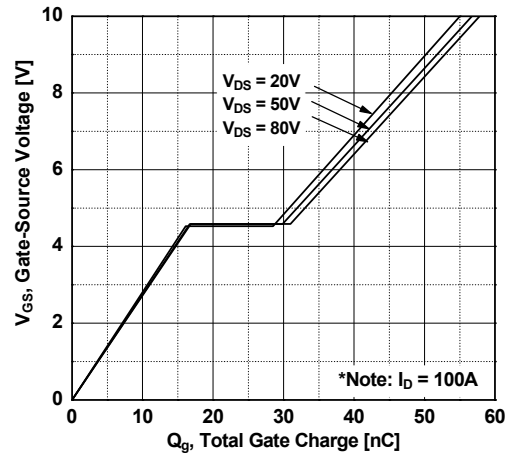


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

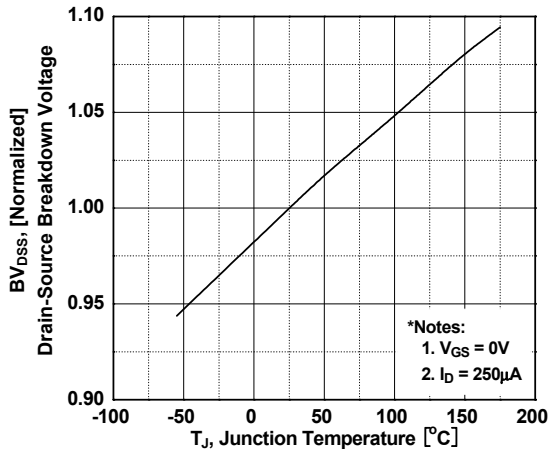


Figure 8. On-Resistance Variation vs. Temperature

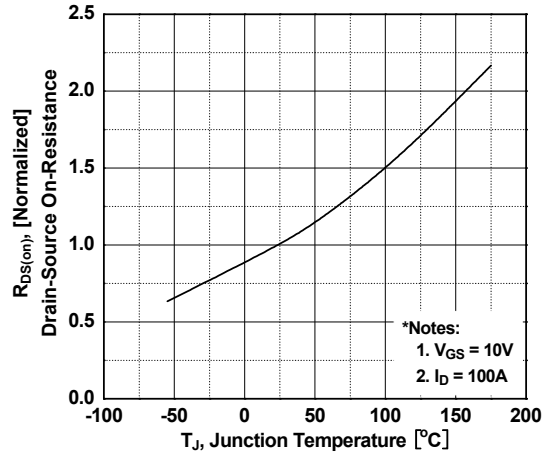


Figure 9. Maximum Safe Operating Area

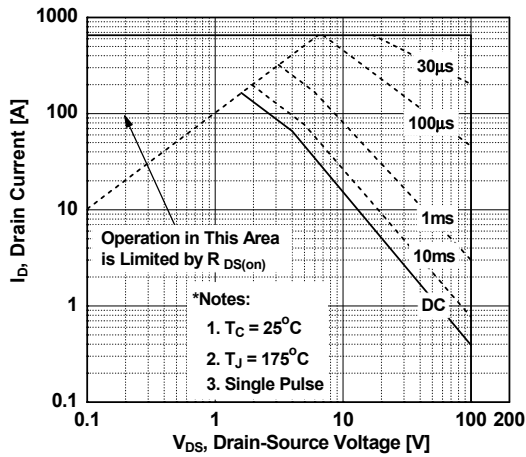


Figure 10. Maximum Drain Current vs. Case Temperature

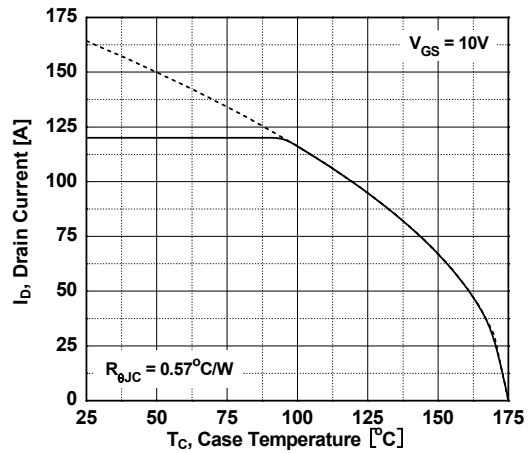


Figure 11. Eoss vs. Drain to Source Voltage

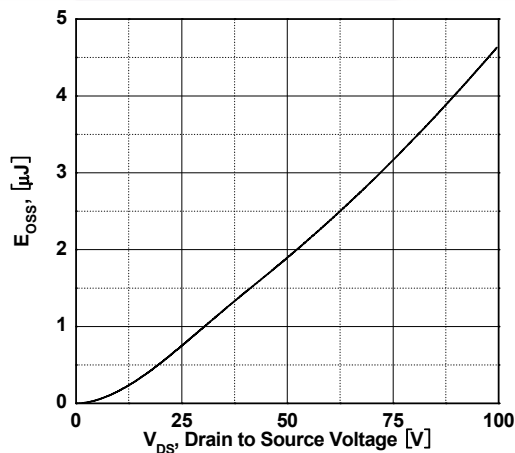
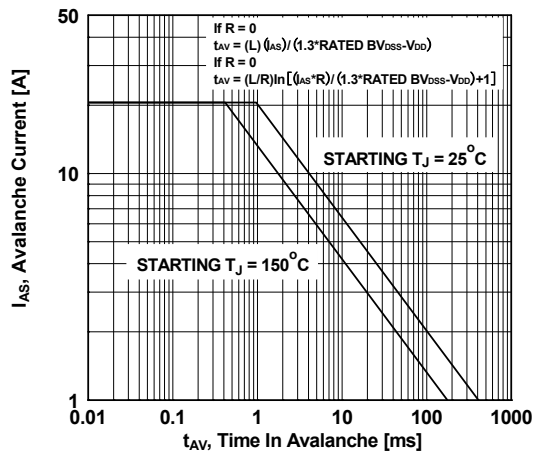
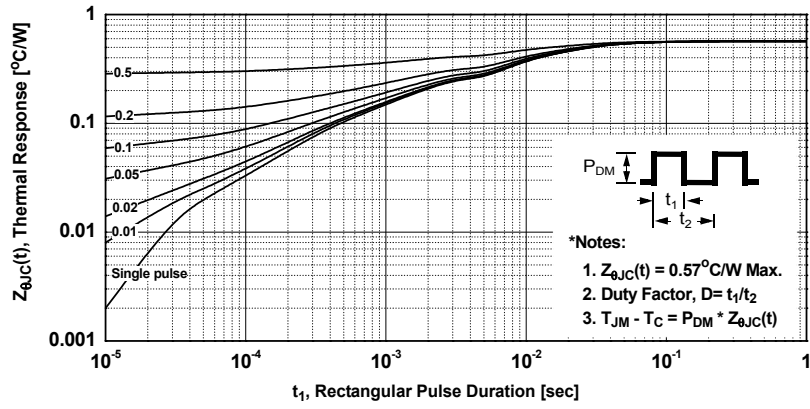


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



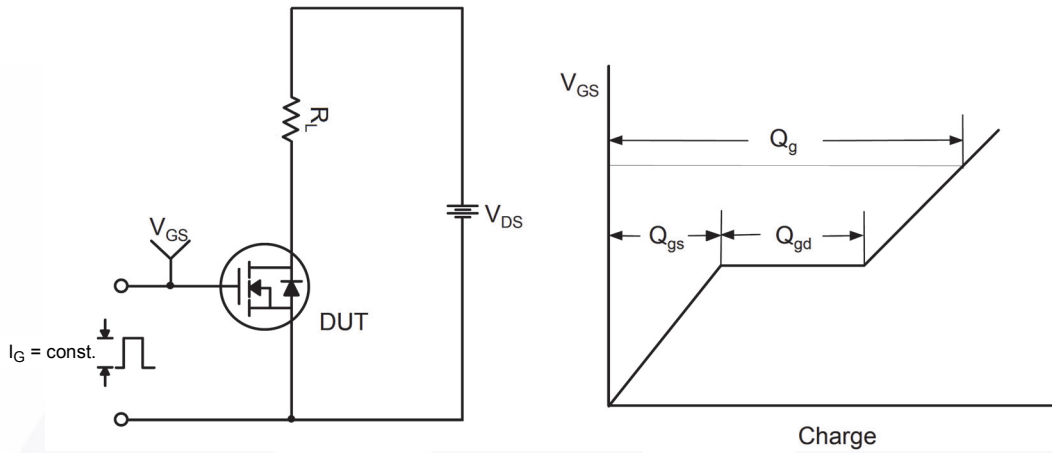


Figure 14. Gate Charge Test Circuit & Waveform



Figure 15. Resistive Switching Test Circuit & Waveforms



Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

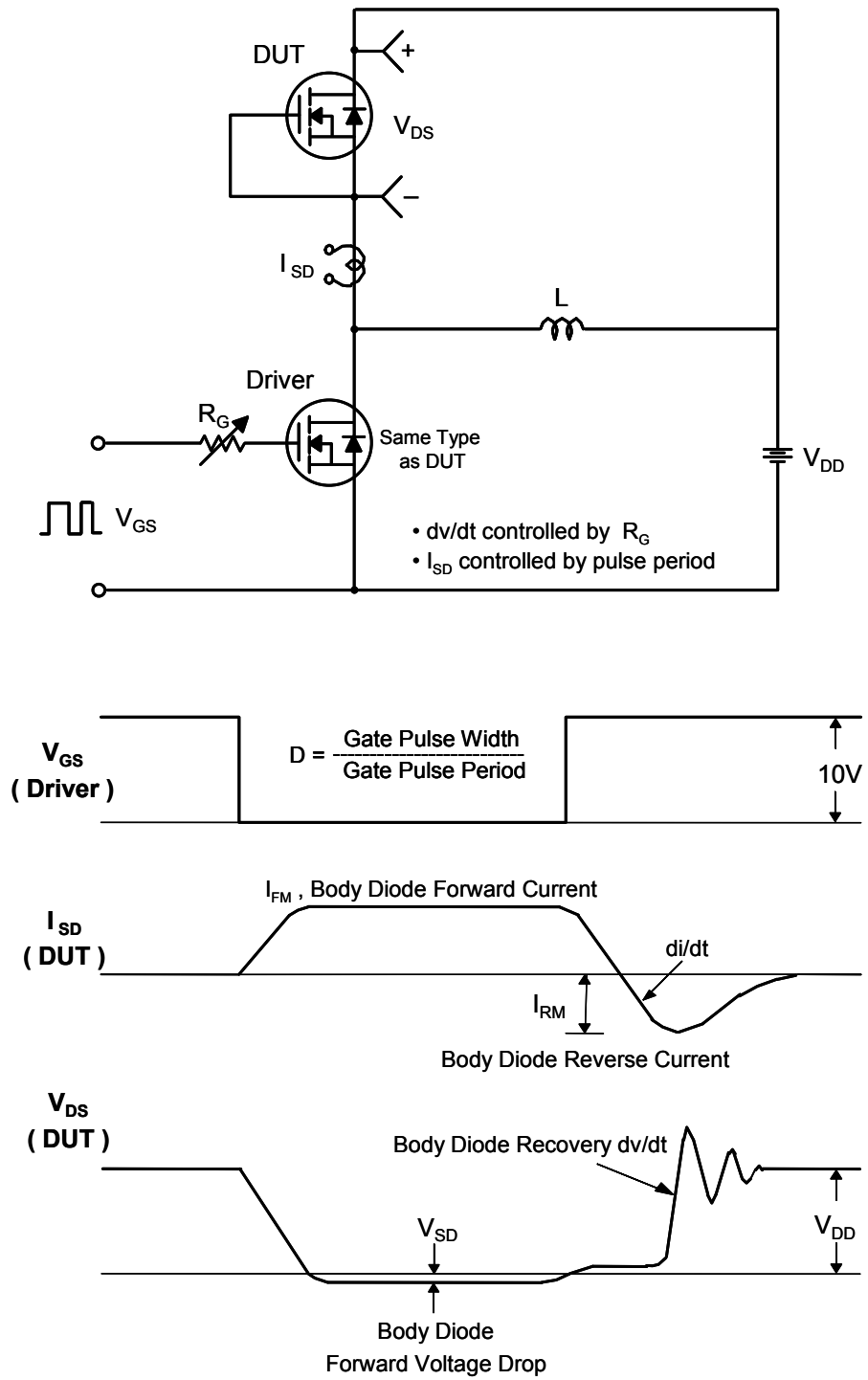


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

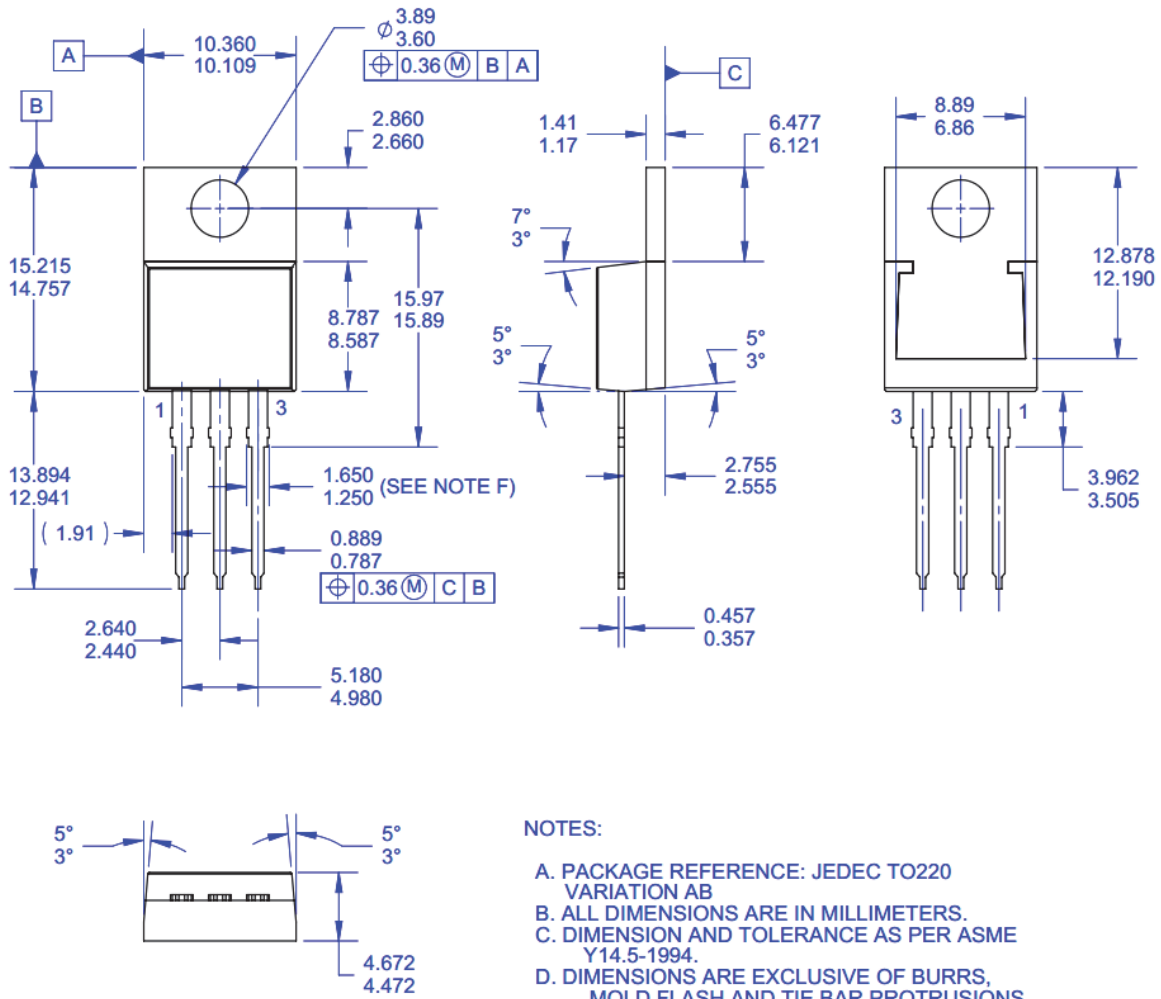


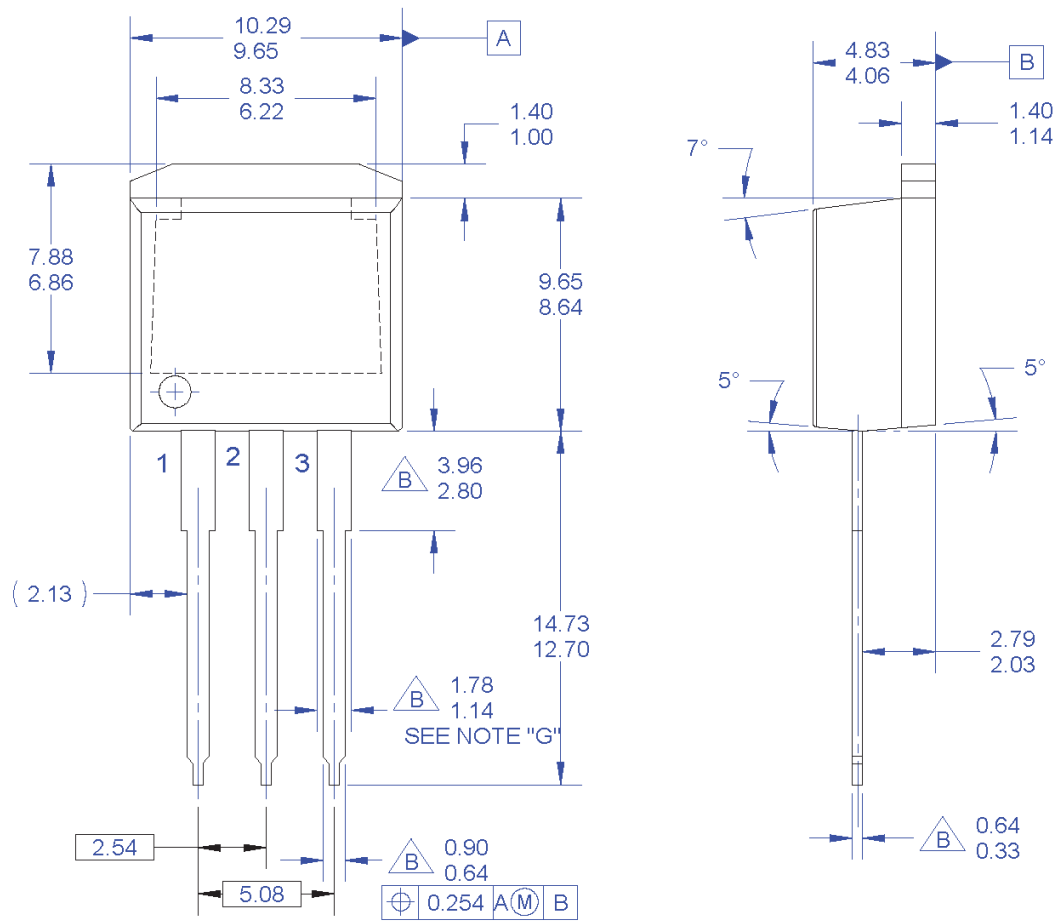
Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

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Mechanical Dimensions



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- Δ B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

Figure 19. TO262 (I²PAK), Molded, 3-Lead, Jedec Variation AA

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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