

FDM3300NZ

Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

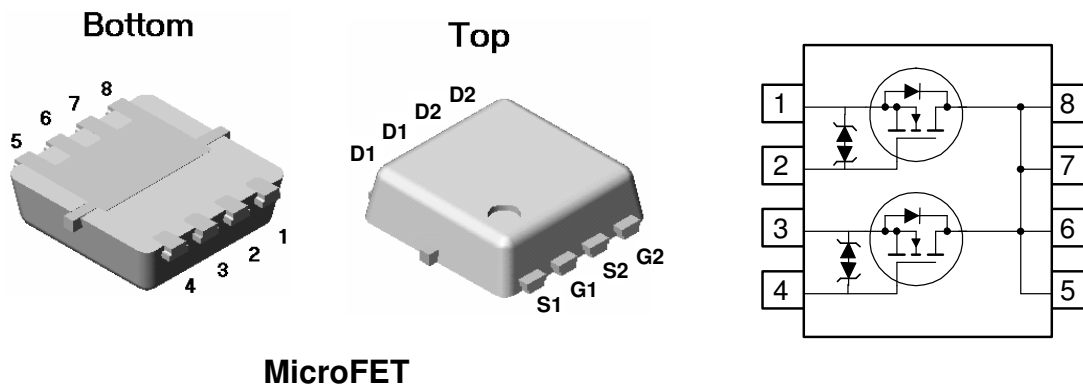
This dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS(ON)}$ @ $V_{GS} = 2.5V$ on special MicroFET lead frame with all the drains on one side of the package.

Applications

- Li-Ion Battery Pack

Features

- 10 A, 20 V $R_{DS(ON)} = 23\text{ m}\Omega$ @ $V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 28\text{ m}\Omega$ @ $V_{GS} = 2.5\text{ V}$
- > 2000v ESD Protection
- Low Profile – 1mm maximum – in the new package MicroFET 3.3x3.3 mm



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	±12	V
I _D	Drain Current – Continuous (Note 1a)	10	A
		40	
P _D	Power Dissipation (Steady State) (Note 1a)	2.5	W
		1.2	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1b)	108	
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
3300N	FDM3300NZ	7"	12mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		10.7		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage,	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		–3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 9\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}, T_J = 125^\circ\text{C}$		16 20 22	23 28 31	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 2.5\text{ V}, V_{DS} = 5\text{ V}$	10			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		35		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1210		pF
C_{oss}	Output Capacitance			330		pF
C_{rss}	Reverse Transfer Capacitance			180		pF
R_G	Gate Resistance	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		2.3		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		10	20	ns
t_r	Turn–On Rise Time			14	25	ns
$t_{d(off)}$	Turn–Off Delay Time			26	42	ns
t_f	Turn–Off Fall Time			13	23	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 4.5\text{ V}$		12	17	nC
Q_{gs}	Gate–Source Charge			2		nC
Q_{gd}	Gate–Drain Charge			4		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				2	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 10\text{ A},$		20		nS
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$		6		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

(a). $R_{\theta JA} = 52^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

(b). $R_{\theta JA} = 108^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

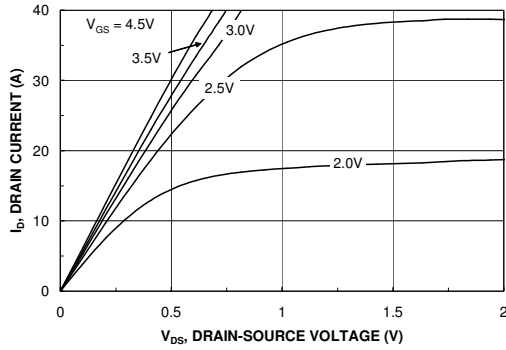


Figure 1. On-Region Characteristics.

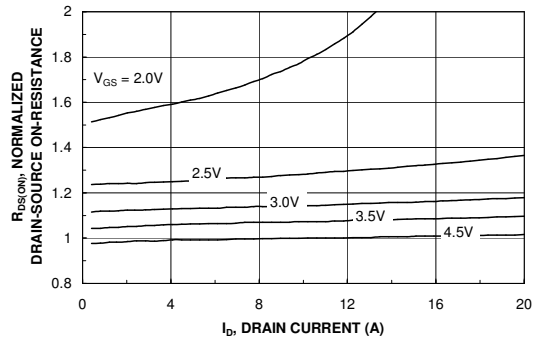


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

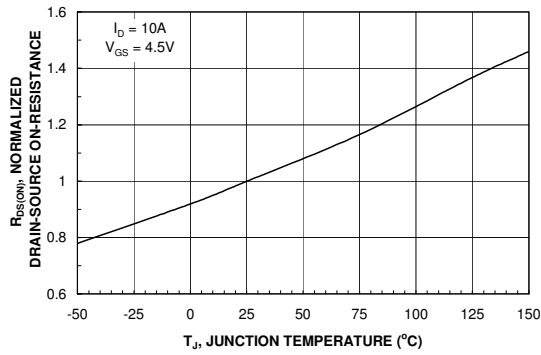


Figure 3. On-Resistance Variation with Temperature.

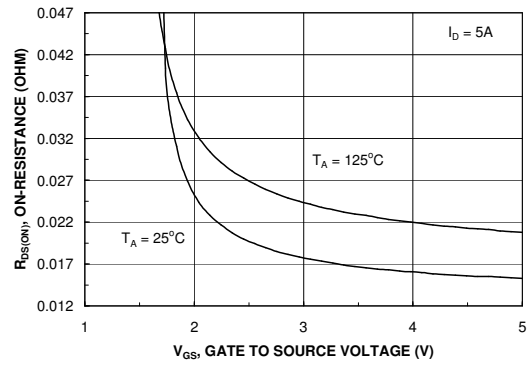


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

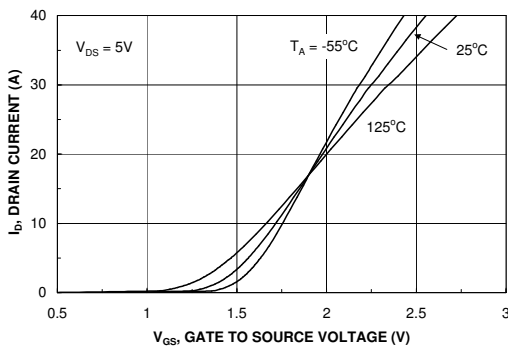


Figure 5. Transfer Characteristics.

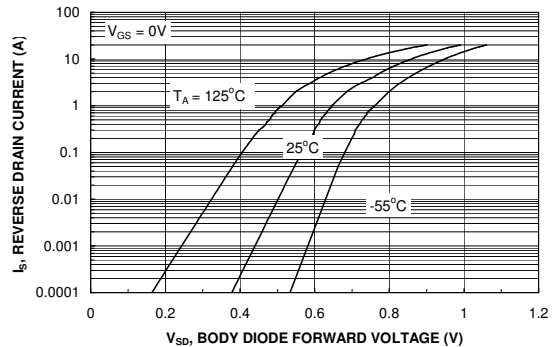


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

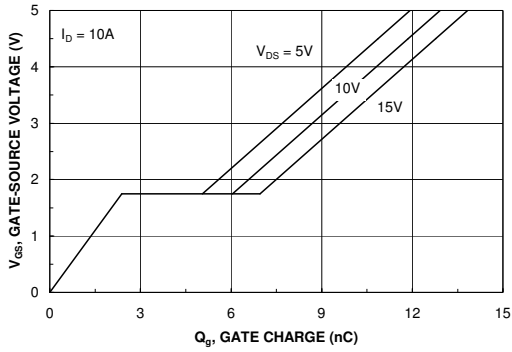


Figure 7. Gate Charge Characteristics.

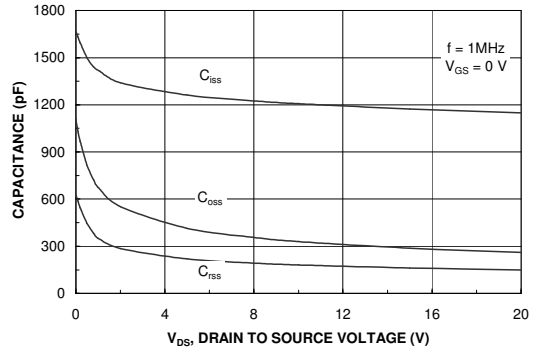


Figure 8. Capacitance Characteristics.

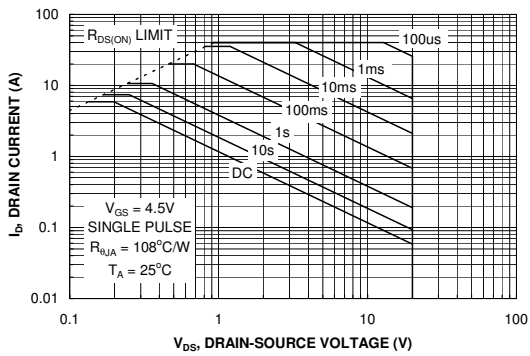


Figure 9. Maximum Safe Operating Area.

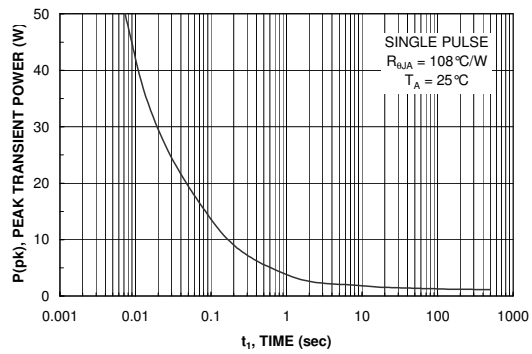


Figure 10. Single Pulse Maximum Power Dissipation.

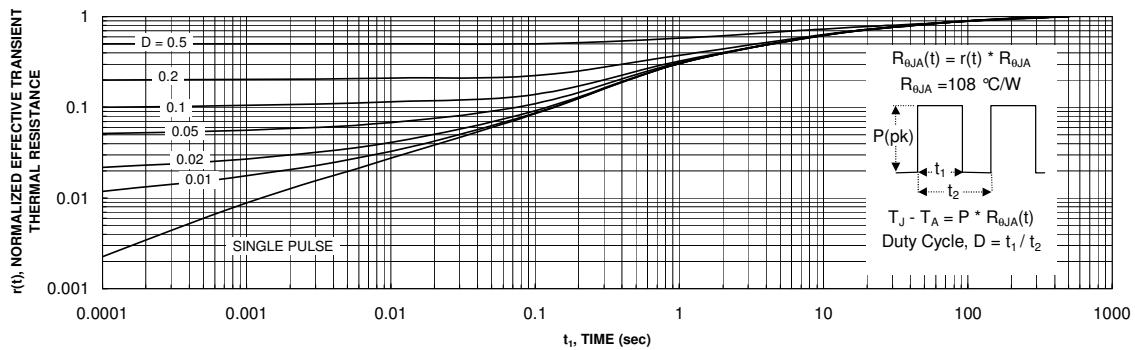


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

PSPICE Electrical Model N-Channel

```
.SUBCKT FDM3300NZ 2 1 3
*NOM TEMP=25 DEG C
*FEB 26, 2003
```

```
CA 12 8 1E-9
CB 15 14 1.2E-9
CIN 6 8 10.8E-10
```

```
DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD
```

```
EBREAK 11 7 17 18 23.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1
```

```
IT 8 17 1
```

```
LGATE 1 9 3.84E-9
LDRAIN 2 5 1.00E-9
LSOURCE 3 7 4E-9
```

```
RLGATE 1 9 38.4
RLDRAIN 2 5 10
RLSOURCE 3 7 40
```

```
MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD
```

```
RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 8.3E-3
RGATE 9 20 4.2
RSLC1 5 51 RSLCMOD 1E-6
RSLC2 5 50 1E3
RSOURCE 8 7 RSOURCEMOD 3.9E-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1
```

```
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD
```

```
VBAT 22 19 DC 1
```

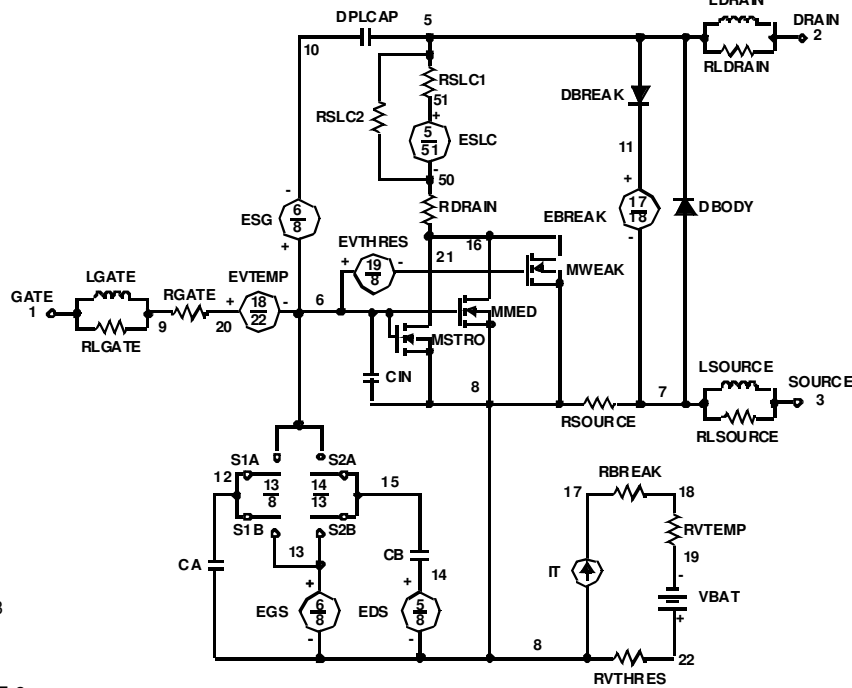
```
ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))^(PWR(V(5,51)/(1E-6*115),3))}}
```

```
.MODEL DBODYMOD D (IS=2E-12 RS=9.9E-3 N=0.90 TRS1=2.1E-3 TRS2=1.0E-6 CJO=4.5E-10 TT=1E-9 M=0.45 IKF=0.3 XTI=2.0)
.MODEL DBREAKMOD D (RS=1E-1 TRS1=1.12E-3 TRS2=1.25E-6)
.MODEL DPLCAPMOD D (CJO=45E-11 IS=1E-30 N=10 M=0.4)
```

```
.MODEL MMEDMOD NMOS (VTO=1.05 KP=8 IS=1E-30 N=10 TOX=1 L=1U W=1U RG=4.2)
.MODEL MSTROMOD NMOS (VTO=1.31 KP=82 IS=1E-30 N=10 TOX=1 L=1U W=1U)
.MODEL MWEAKMOD NMOS (VTO=0.81 KP=0.05 IS=1E-30 N=10 TOX=1 L=1U W=1U RG=42 RS=.1)
.MODEL RBREAKMOD RES (TC1=0.56E-3 TC2=1.00E-7)
.MODEL RDRAINMOD RES (TC1=4.6E-3 TC2=10E-6)
.MODEL RSLCMOD RES (TC1=2.5E-3 TC2=8E-6)
.MODEL RSOURCEMOD RES (TC1=1.0E-3 TC2=1E-6)
.MODEL RVTHRESMOD RES (TC1=-1.85E-3 TC2=-7E-6)
.MODEL RVTEMPMOD RES (TC1=-0.7E-3 TC2=0.50E-6)
```

```
.MODEL S1AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-4 VOFF=-3)
.MODEL S1BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-3 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-1.0 VOFF=-0.6)
.MODEL S2BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=0.6 VOFF=-1.0)
.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



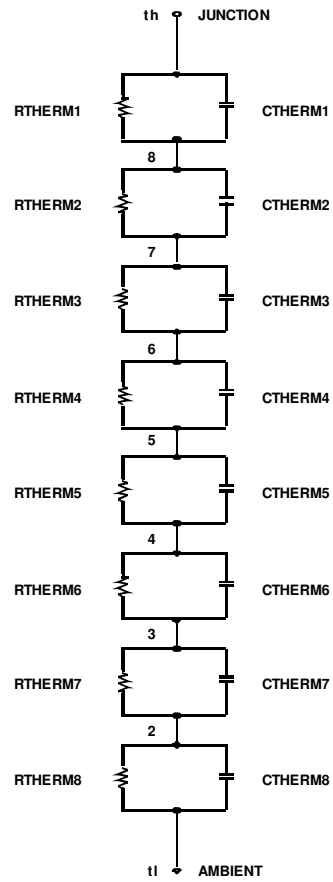
SPICE Thermal Model

```
.SUBCKT FDM3300NZ_THERM TH TL
*Thermal Model Subcircuit
*Feb 26, 2003
```

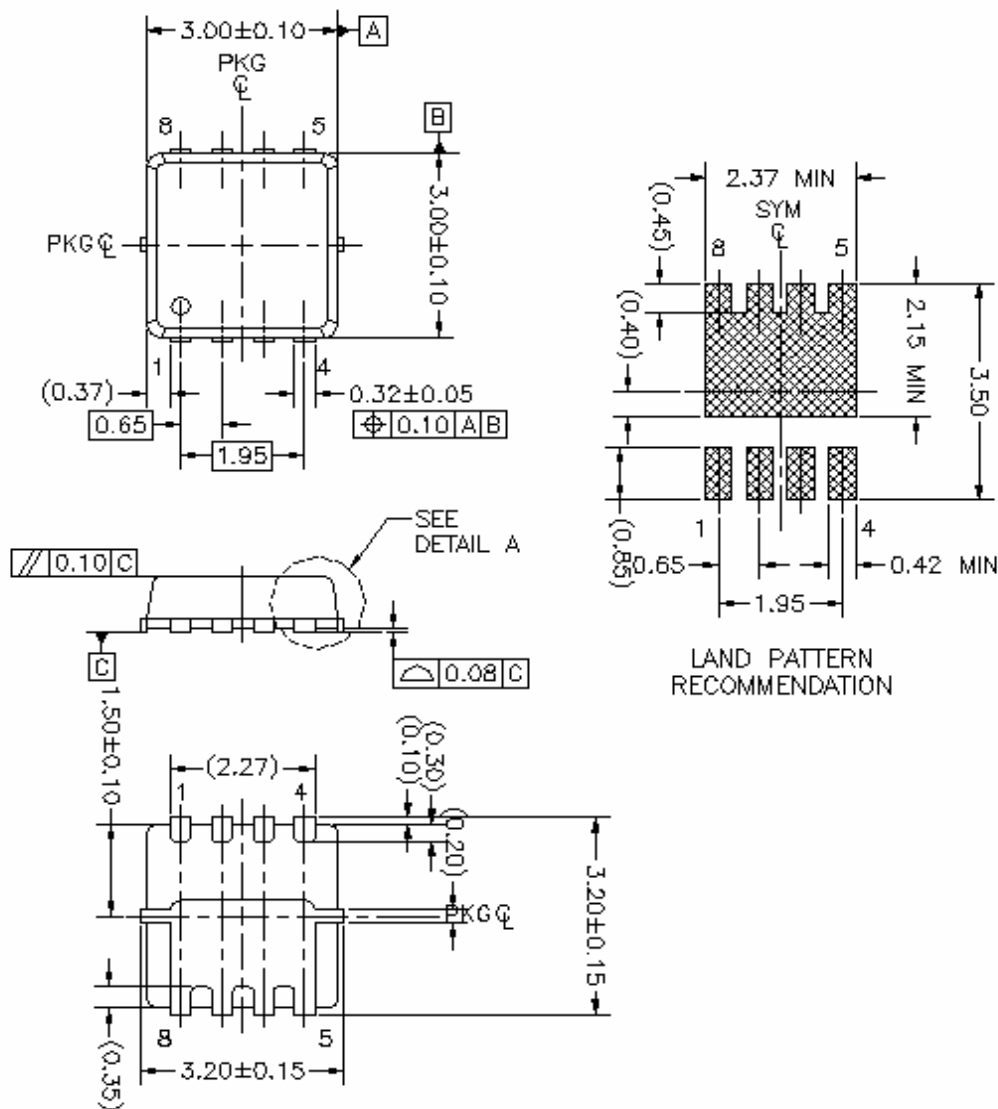
```
CTHERM1 TH 8 3
CTHERM2 8 7 5
CTHERM3 7 6 7
CTHERM4 6 5 13.2
CTHERM5 5 4 25.4
CTHERM6 4 3 36.21
CTHERM7 3 2 47.54
CTHERM8 2 TL 208.21

R THERM1 TH 8 0.04
R THERM2 8 7 0.05
R THERM3 7 6 0.06
R THERM4 6 5 0.07
R THERM5 5 4 0.085
R THERM6 4 3 0.095
R THERM7 3 2 0.25
R THERM8 2 TL 0.35

.ENDS
```

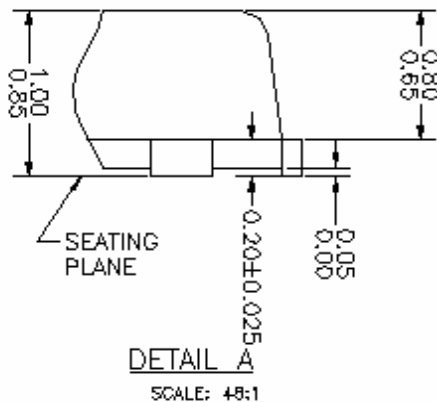


Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.



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CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
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EnSigna™	µC™	OCX™	RapidConfigure™	UHC™
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Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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