

FDMA2002NZ

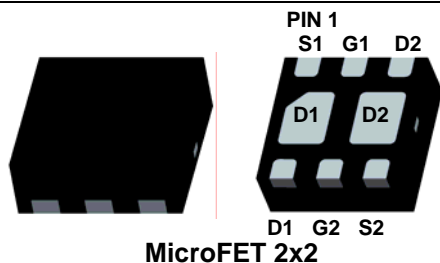
Dual N-Channel PowerTrench® MOSFET

General Description

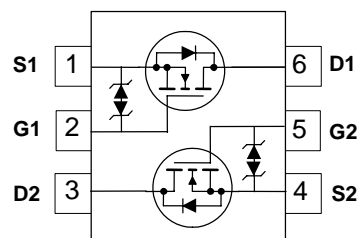
This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET 2x2 offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- 2.9 A, 30 V $R_{DS(ON)} = 123 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 140 \text{ m}\Omega @ V_{GS} = 3.0 \text{ V}$
 $R_{DS(ON)} = 163 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- RoHS Compliant



www.DataSheet4U.com



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$)	2.9	A
	– Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 2.5\text{V}$)	2.7	
	– Pulsed	10	
P_D	Power Dissipation for Single Operation (Note 1a)	1.5	W
	Power Dissipation for Single Operation (Note 1b)	0.65	
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	83 (Single Operation)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	193 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	68 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	145 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
002	FDMA2002NZ	7"	8mm	3000 units

Electrical Characteristics
 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		25		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$		75	123	m Ω
		$V_{GS} = 3.0\text{ V}, I_D = 2.7\text{ A}$		84	140	
		$V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}$		92	163	
		$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}, T_C = 85^\circ\text{C}$		95	166	
		$V_{GS} = 3.0\text{ V}, I_D = 2.7\text{ A}, T_C = 150^\circ\text{C}$		138	203	
		$V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}, T_C = 150^\circ\text{C}$		150	268	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		190	220	pF
C_{oss}	Output Capacitance			30	40	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		6	12	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			12	21	ns
t_f	Turn–Off Fall Time			2	10	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 2.9\text{ A},$ $V_{GS} = 4.5\text{ V}$		2.4	3.0	nC
Q_{gs}	Gate–Source Charge			0.35		nC
Q_{gd}	Gate–Drain Charge			0.75		nC

Drain–Source Diode Characteristics and Maximum Ratings

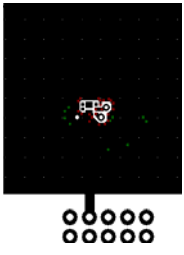
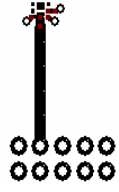
I_S	Maximum Continuous Drain–Source Diode Forward Current			2.9	A	
V_{SD}	Drain–Source Diode Forward Voltage	$I_S = 2.0\text{ A}$		0.9	1.2	V
		$I_S = 1.1\text{ A}$		0.8	1.2	
t_{rr}	Diode Reverse Recovery Time	$I_F = 2.9\text{ A},$		10	ns	
Q_{rr}	Diode Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$		2	nC	

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
 - (a) $R_{\theta JA} = 83^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
 - (b) $R_{\theta JA} = 193^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper
 - (c) $R_{\theta JA} = 68^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
 - (d) $R_{\theta JA} = 145^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

	<p>a) 83°C/W when mounted on a 1 in² pad of 2 oz copper</p>		<p>b) 193°C/W when mounted on a minimum pad of 2 oz copper</p>
---	---	---	---

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

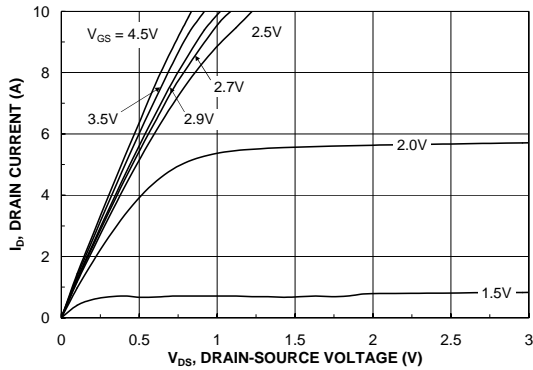


Figure 1. On-Region Characteristics.

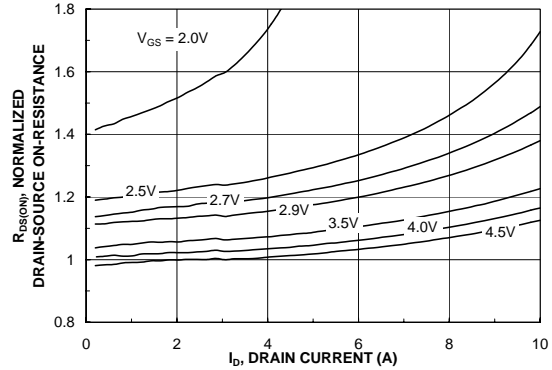


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

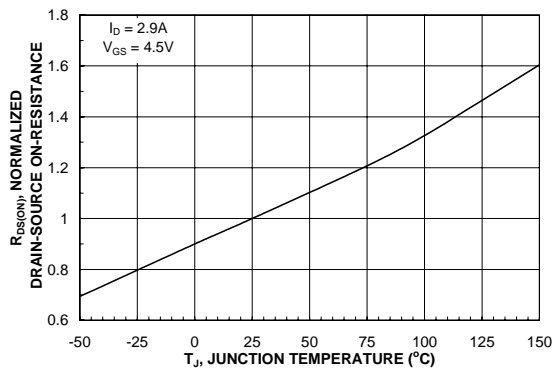


Figure 3. On-Resistance Variation with Temperature.

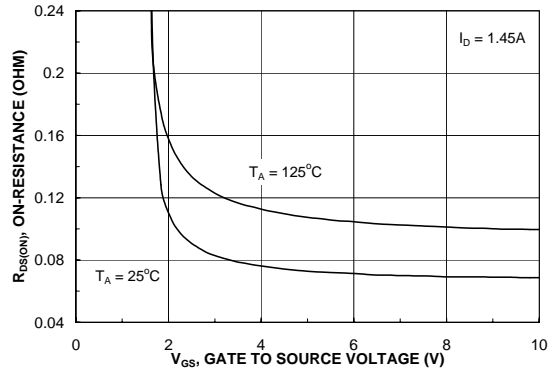


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

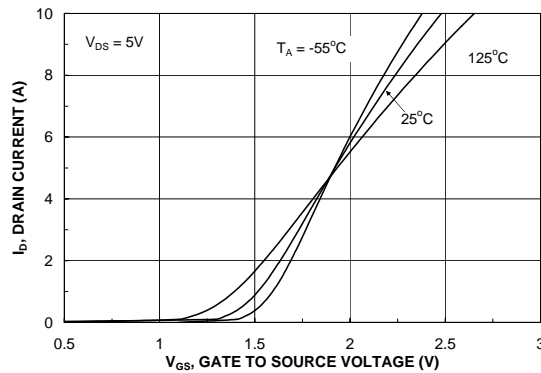


Figure 5. Transfer Characteristics.

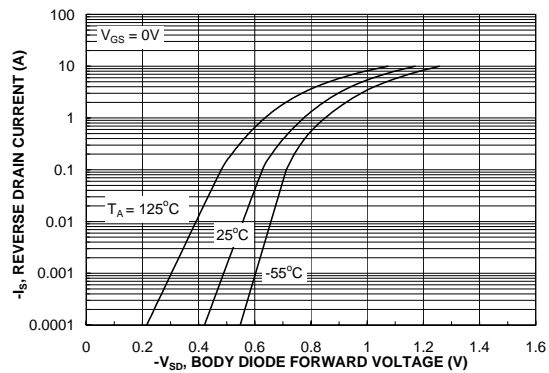


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

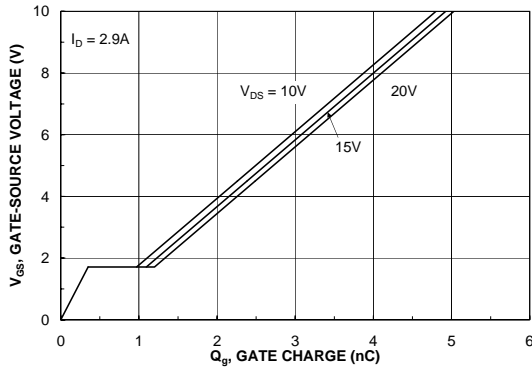


Figure 7. Gate Charge Characteristics.

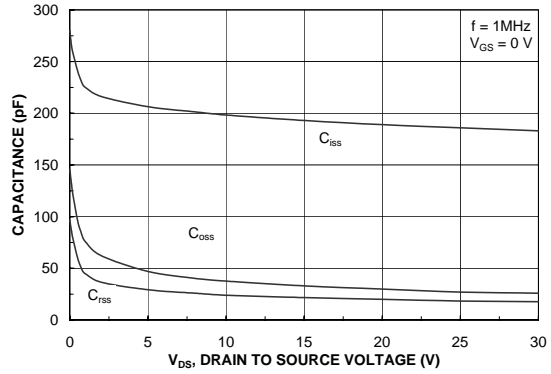


Figure 8. Capacitance Characteristics.

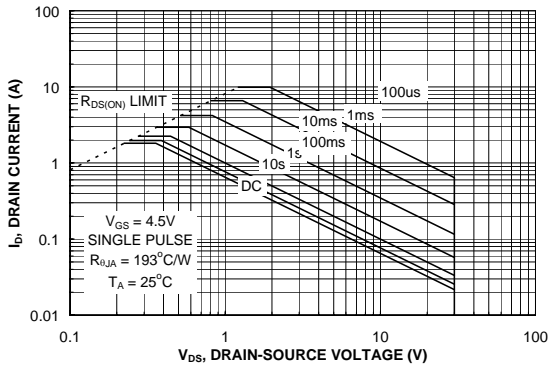


Figure 9. Maximum Safe Operating Area.

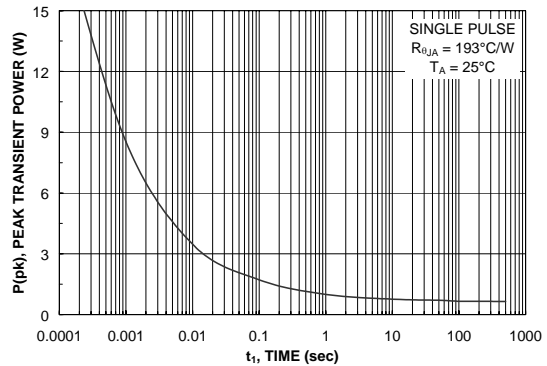


Figure 10. Single Pulse Maximum Power Dissipation.

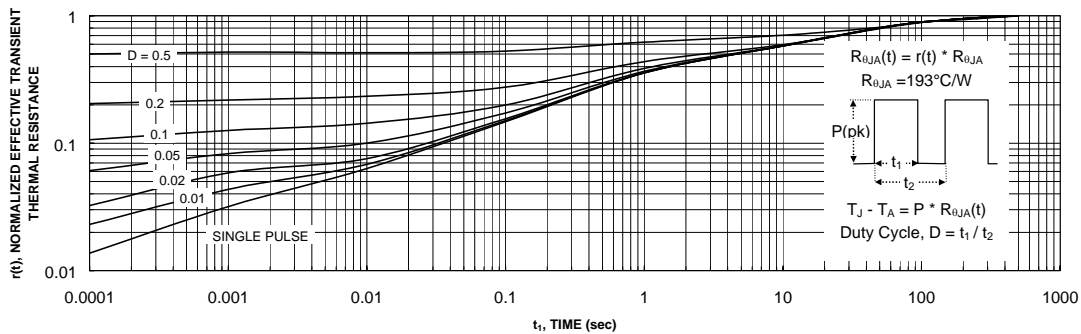
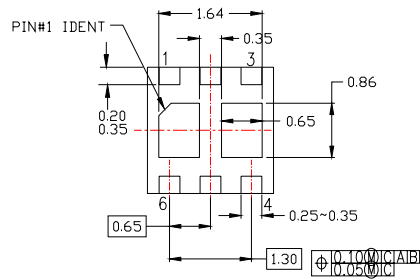
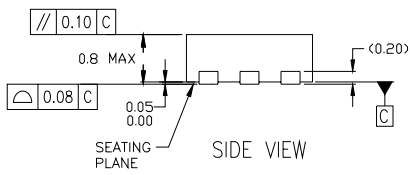
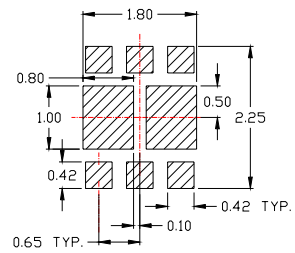
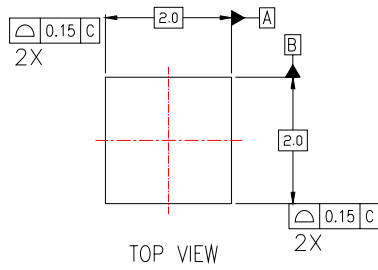


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC, DATED 11/2001
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP06JrevB

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerEdge™	SuperFET™
ActiveArray™	FASTr™	LittleFET™	PowerSaver™	SuperSOT™-3
Bottomless™	FPST™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
Build it Now™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CoolFET™	GlobalOptoisolator™	MicroPak™	QST™	SyncFET™
CROSSVOLT™	GTO™	MICROWIRE™	QT Optoelectronics™	TCM™
DOMET™	HiSeC™	MSX™	Quiet Series™	TinyLogic®
EcoSPARK™	I ² C™	MSXPro™	RapidConfigure™	TINYOPTO™
E ² CMOS™	i-Lo™	OCX™	RapidConnect™	TruTranslation™
EnSigna™	ImpliedDisconnect™	OCXPro™	μSerDes™	UHC™
FACT™	IntelliMAX™	OPTOLOGIC®	ScalarPump™	UniFET™
FACT Quiet Series™		OPTOPLANAR™	SILENT SWITCHER®	UltraFET®
Across the board. Around the world.™		PACMAN™	SMART START™	VCX™
The Power Franchise®		POP™	SPM™	Wire™
Programmable Active Droop™		Power247™	Stealth™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.