February 2015

FDMA6676PZ

Single P-Channel PowerTrench® MOSFET

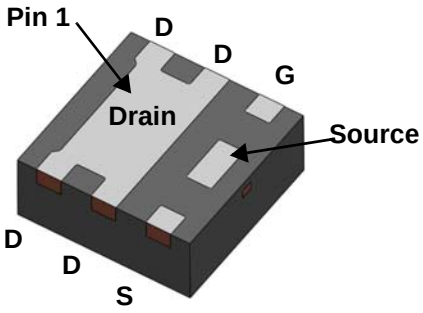
-30 V, -11 A, 13.5 mΩ

Features

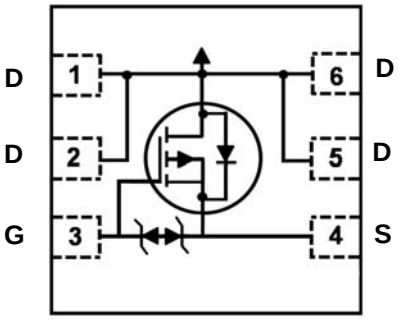
- Max $r_{DS(on)}$ = 13.5 mΩ @ V_{GS} = -10 V
- 25V V_{GS} Extended Operating Rating
- 30V V_{DS} Blocking
- 2x2mm Form Factor
- Low Profile - 0.8 mm maximum
- Integrated Protection Diode
- RoHS Compliant
- Halogen Free

General Description

This device is an ultra low resistance P-Channel FET. It is designed for power line load switching applications and reverse polarity protection. It is especially optimized for voltage rails that can climb as high as 25V. Typical end systems include laptop computers, tablets and mobile phone. Applications include battery protection, input power line protection and charge path protection, including USB and other charge paths. The FDMA6676PZ has an enhanced V_{GS} rating of 25V specifically designed to simplify installation. When used as reverse polarity protection, with gate tied to ground and drain tied to V input, it is designed to support operating input voltages that can raise as high as 25V without the need for external Zener protection on the gate. Its small 2x2x0.8 form factor make it an ideal part for mobile and space constrained applications.



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-30	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current -Continuous	T_A = 25 °C	(Note 1a)	-11	A
	-Pulsed		(Note 3)	-165	
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	2.4	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

Package Marking and Ordering Information

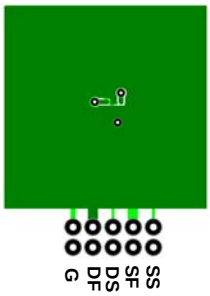
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
676	FDMA6676PZ	MicroFET 2X2	7 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-1.2	-2	-2.6	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		5.9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -11 A		11	13.5	mΩ
		V_{GS} = -4.5 V, I_D = -8 A		19	27	
		V_{GS} = -10 V, I_D = -11 A, T_J = 125 °C		14.5	21	
g_{FS}	Forward Transconductance	V_{DD} = -5 V, I_D = -11 A		38		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		1440	2160	pF
C_{oss}	Output Capacitance			477	720	pF
C_{rss}	Reverse Transfer Capacitance			458	690	pF
R_g	Gate Resistance			12		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15 V, I_D = -11 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		8.8	18	ns
t_r	Rise Time			19	34	ns
$t_{d(off)}$	Turn-Off Delay Time			87	139	ns
t_f	Fall Time			72	115	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -15 V, I_D = -11 A		33	46	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to -4.5 V; V_{DD} = -15 V, I_D = -11 A		20	28	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -15 V, I_D = -11 A		4.5		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = -15 V, I_D = -11 A		13		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.7	-1.2	V
		V_{GS} = 0 V, I_S = -11 A (Note 2)		-0.9	-1.4	V
t_{rr}	Reverse Recovery Time	I_F = -11 A, di/dt = 100 A/μs		31	50	ns
Q_{rr}	Reverse Recovery Charge			9	18	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Pulse Id refers to Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25 °C unless otherwise noted

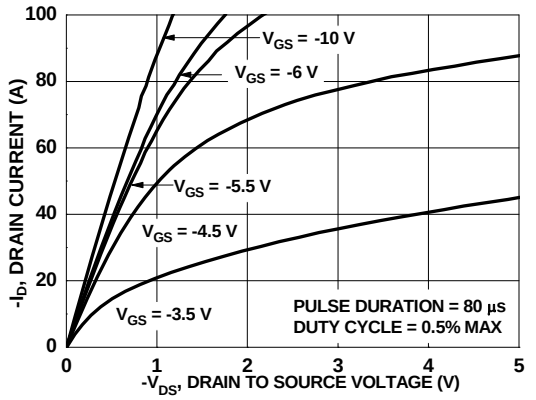


Figure 1. On-Region Characteristics

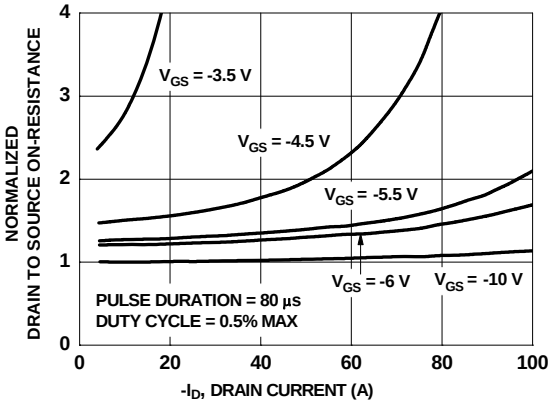


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

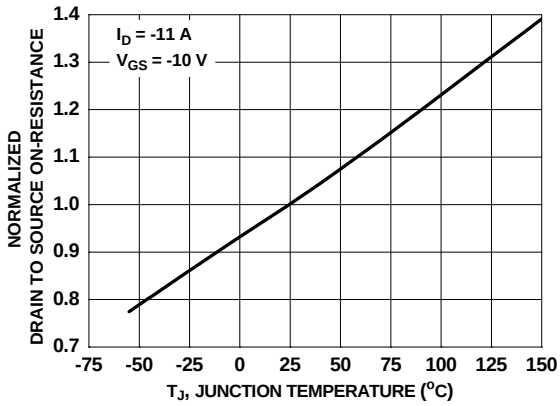


Figure 3. Normalized On-Resistance vs Junction Temperature

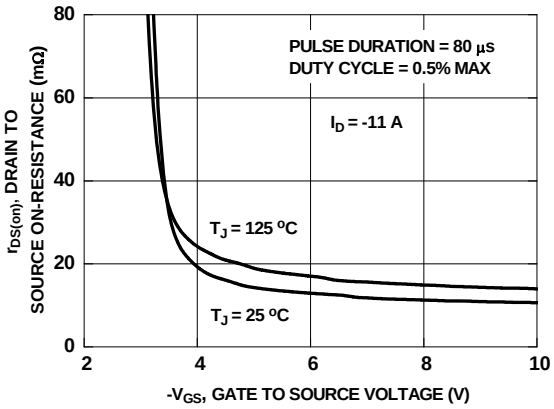


Figure 4. On-Resistance vs Gate to Source Voltage

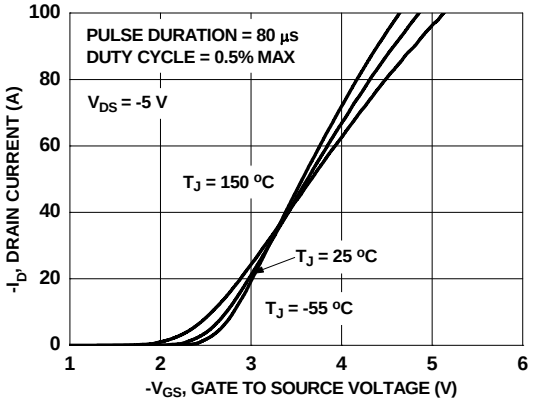


Figure 5. Transfer Characteristics

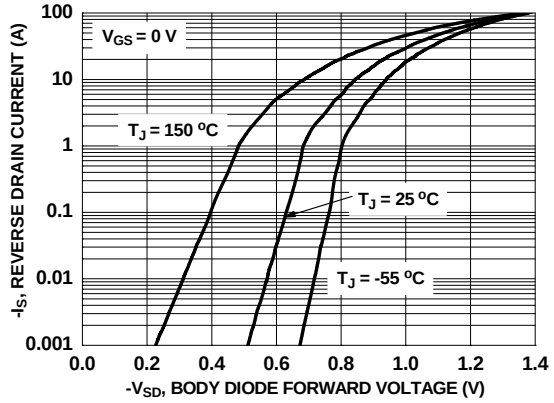


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

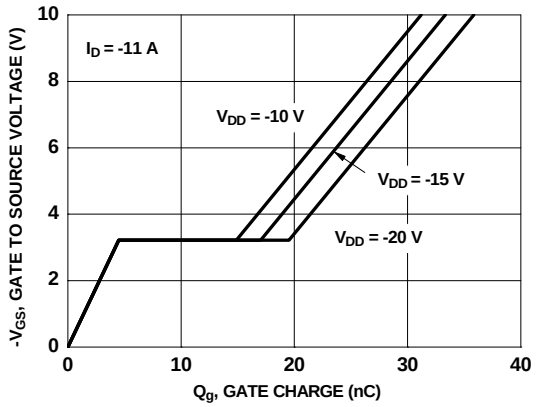


Figure 7. Gate Charge Characteristics

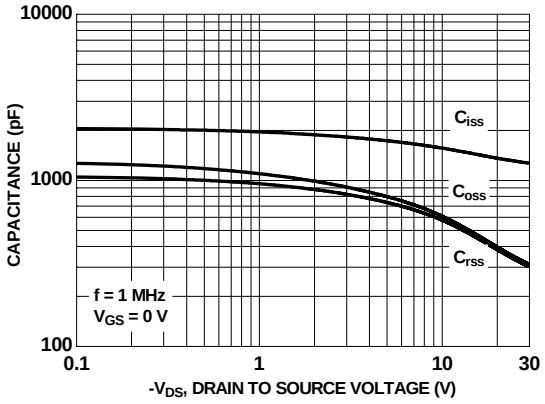


Figure 8. Capacitance vs Drain to Source Voltage

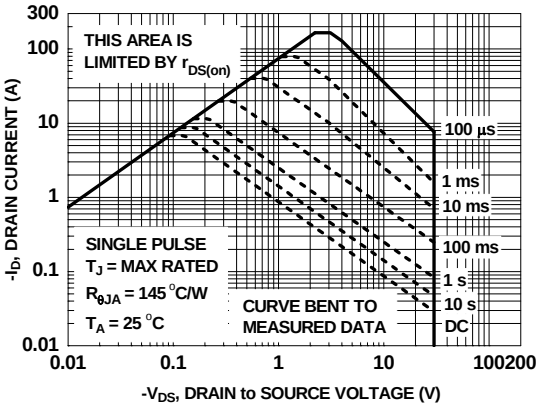


Figure 9. Forward Bias Safe Operating Area

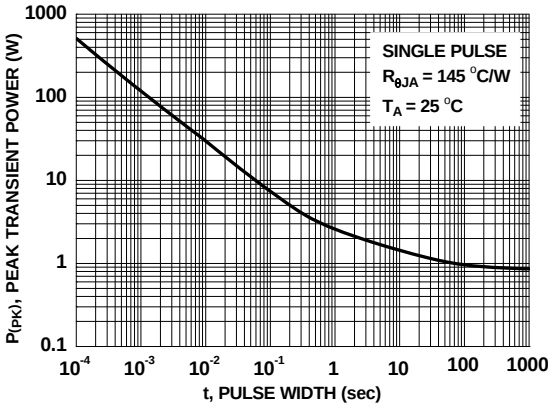


Figure 10. Single Pulse Maximum Power Dissipation

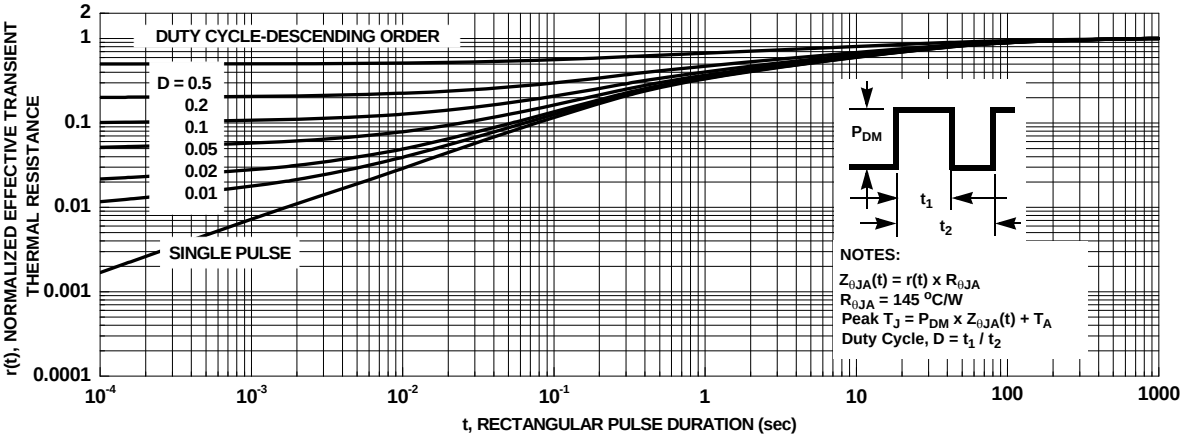
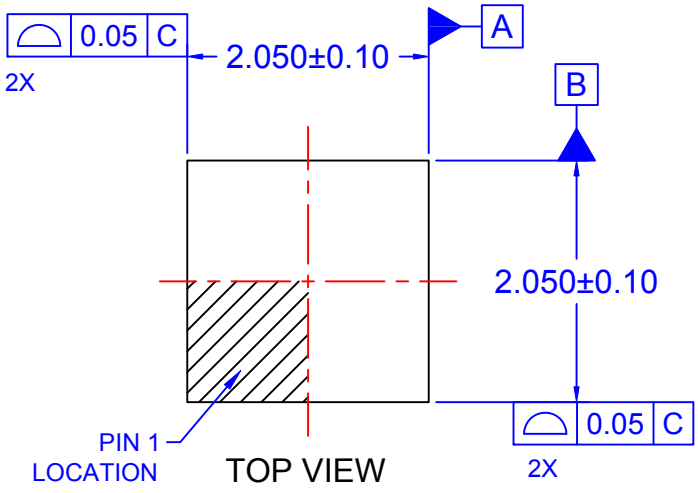
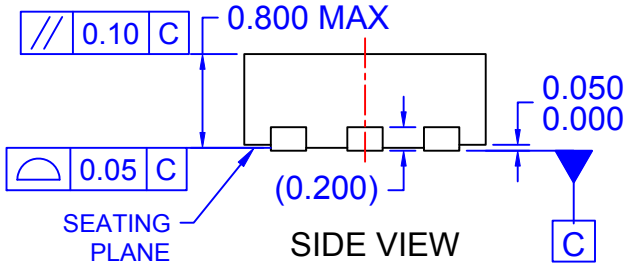
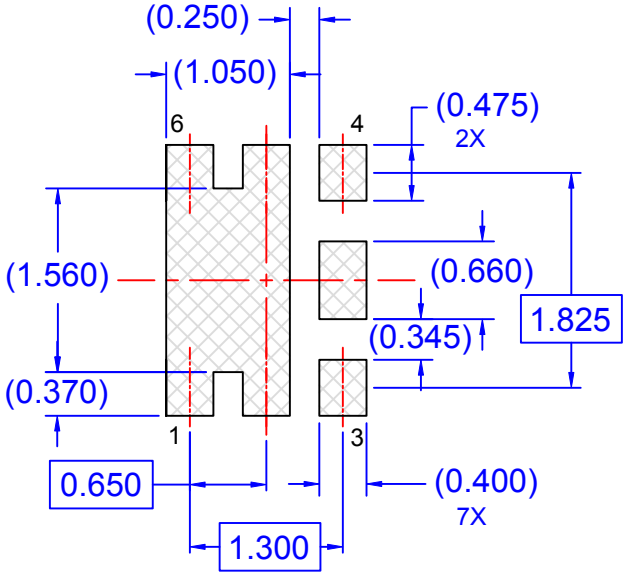


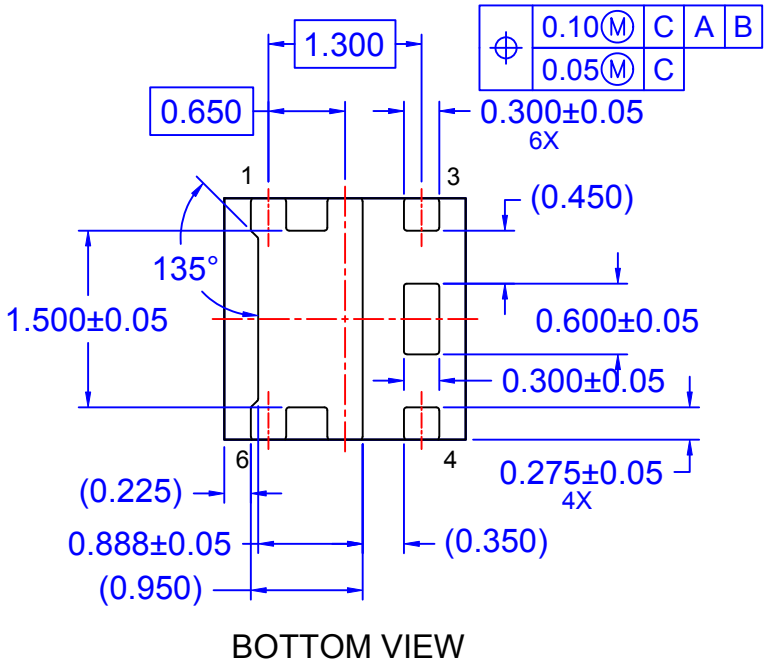
Figure 11. Junction-to-Ambient Transient Thermal Response Curve







LAND PATTERN
RECOMMENDATION



BOTTOM VIEW

NOTES:
A) THIS PACKAGE IS NON-JEDEC
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