MOSFET – Single, P-Channel, POWERTRENCH®

-30 V, -11 A, 13.5 mΩ

FDMA6676PZ

Description

This device is an ultra low resistance P−Channel FET. It is designed for power line load switching applications and reverse polarity protection. It is especially optimized for voltage rails that can climb as high as 25 V. Typical end systems include laptop computers, tablets and mobile phone. Applications include battery protection, input power line protection and charge path protection, including USB and other charge paths. The FDMA6676PZ has an enhanced V_{GS} rating of 25 V specifically designed to simplify installation. When used as reverse polarity protection, with gate tied to ground and drain tied to V input, it is designed to support operating input voltages that can raise as high as 25 V without the need for external Zener protection on the gate. Its small 2 x 2 x 0.8 form factor make it an ideal part for mobile and space constrained applications.

Features

- Max $r_{DS(on)}$ = 13.5 mΩ @ V_{GS} = −10 V
- 25 V V_{GS} Extended Operating Rating
- 30 V V_{DS} Blocking
- 2 x 2 mm Form Factor
- Low Profile − 0.8 mm Maximum
- Integrated Protection Diode
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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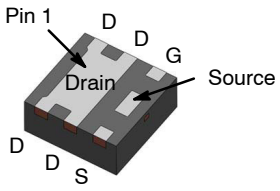

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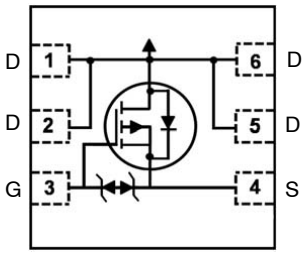
CASE 483AV

MARKING DIAGRAM

&2	= 2−Digit Date Code
&K	= Lot Code
&Z	= Assembly Plant Code
676	= Specific Device Code
&.	= Pin 1 Dot

PIN CONNECTION



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		−30	V
V_{GS}	Gate to Source Voltage		±25	V
I_D	Drain Current − Continuous,	T_A = 25°C (Note 1a)	−11	A
	− Pulsed	(Note 3)	−165	
P_D	Power Dissipation	T_A = 25°C (Note 1a)	2.4	W
	Power Dissipation	T_A = 25°C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic		Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

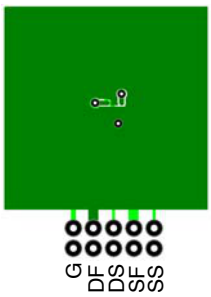
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−30			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C		−19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −24 V, V_{GS} = 0 V			−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−1.2	−2	−2.6	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C		5.9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −10 V, I_D = −11 A		11	13.5	mΩ
		V_{GS} = −4.5 V, I_D = −8 A		19	27	
		V_{GS} = −10 V, I_D = −11 A, T_J = 125°C		14.5	21	
g_{FS}	Forward Transconductance	V_{DD} = −5 V, I_D = −11 A		38		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz		1440	2160	pF
C_{oss}	Output Capacitance			477	720	pF
C_{rss}	Reverse Transfer Capacitance			458	690	pF
R_g	Gate Resistance			12		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −15 V, I_D = −11 A, V_{GS} = −10 V, R_{GEN} = 6 Ω		8.8	18	ns
t_r	Rise Time			19	34	ns
$t_{d(off)}$	Turn−Off Delay Time			87	139	ns
t_f	Fall Time			72	115	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to −10 V, V_{DD} = −15 V, I_D = −11 A		33	46	nC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

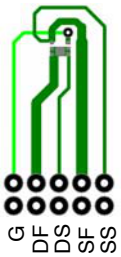
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SWITCHING CHARACTERISTICS						
Q_g	Total Gate Charge	V_{GS} = 0 V to −4.5 V, V_{DD} = −15 V, I_D = −11 A		20	28	nC
Q_{gs}	Gate to Source Charge	V_{DD} = −15 V, I_D = −11 A		4.5		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = −15 V, I_D = −11 A		13		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −2 A (Note 2)		−0.7	−1.2	V
		V_{GS} = 0 V, I_S = −11 A (Note 2)		−0.9	−1.4	V
t_{rr}	Reverse Recovery Time	I_F = -11 A, di/dt = 100 A/μs		31	50	ns
Q_{rr}	Reverse Recovery Charge			9	18	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user’s board design.



a. 52°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Pulse Id refers to Forward Bias Safe Operation Area.

ORDERING INFORMATION

Device Marking	Device	Package	Package Method†
676	FDMA6676PZ	WDFN−6	3000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

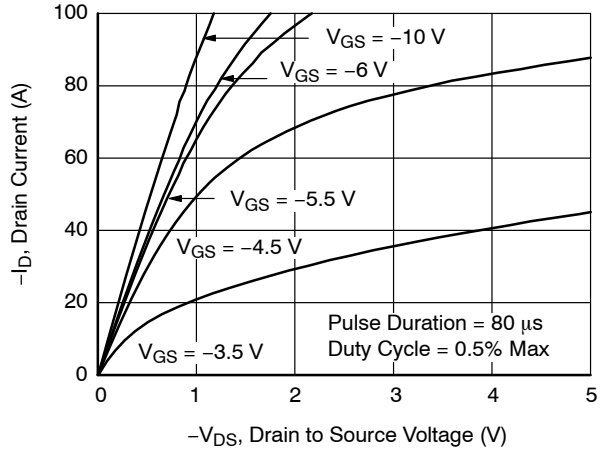


Figure 1. On−Region Characteristics

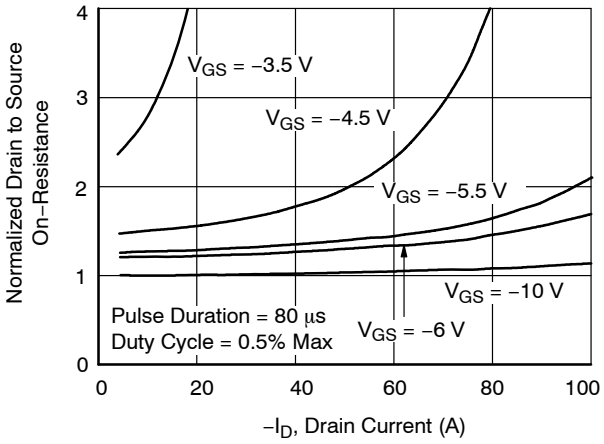


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

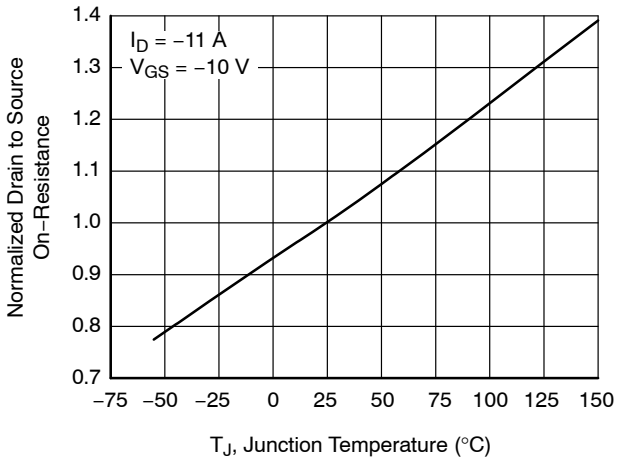


Figure 3. Normalized On−Resistance vs. Junction Temperature

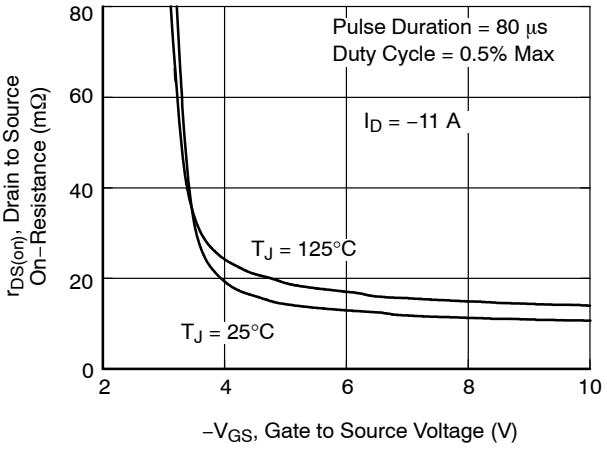


Figure 4. On−Resistance vs. Gate to Source Voltage

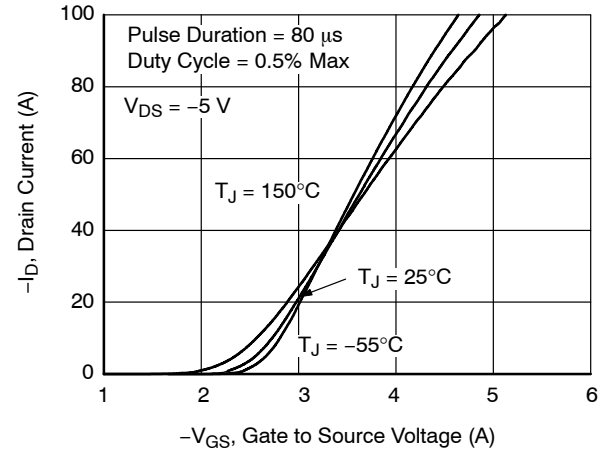


Figure 5. Transfer Characteristics

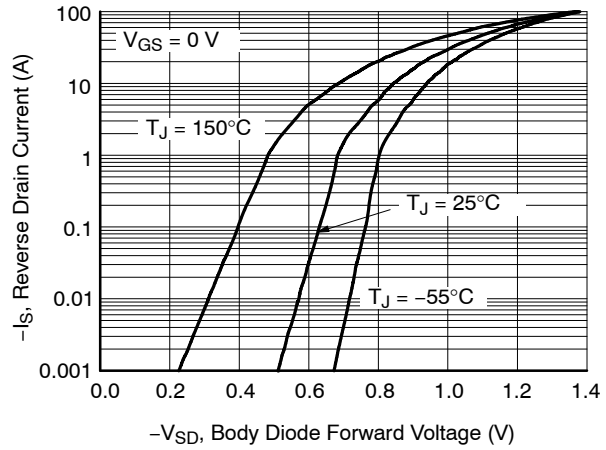


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

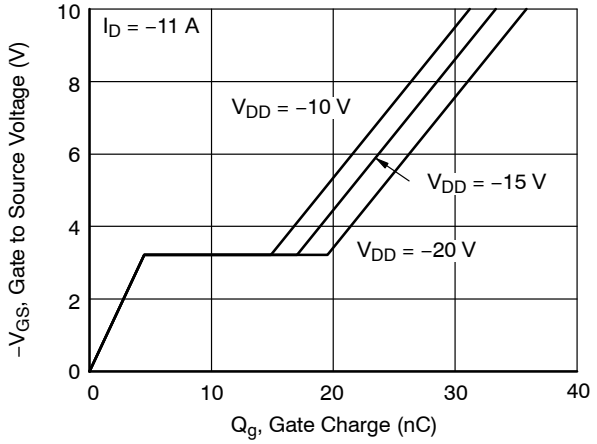


Figure 7. Gate Charge Characteristics

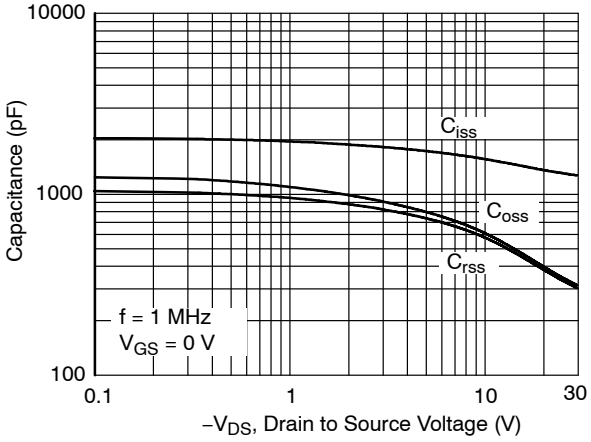


Figure 8. Capacitance vs. Drain to Source Voltage

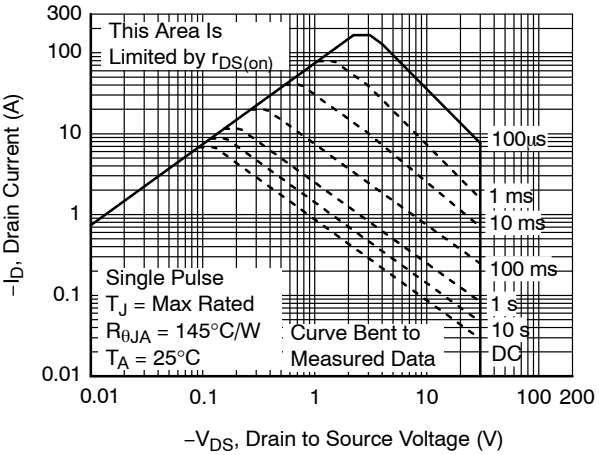


Figure 9. Forward Bias Safe Operating Area

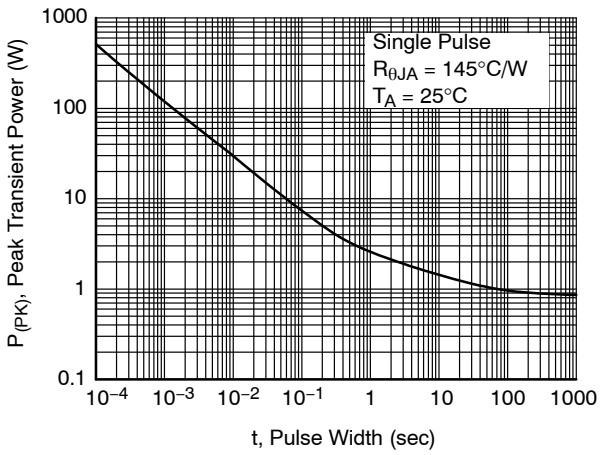


Figure 10. Single Pulse Maximum Power Dissipation

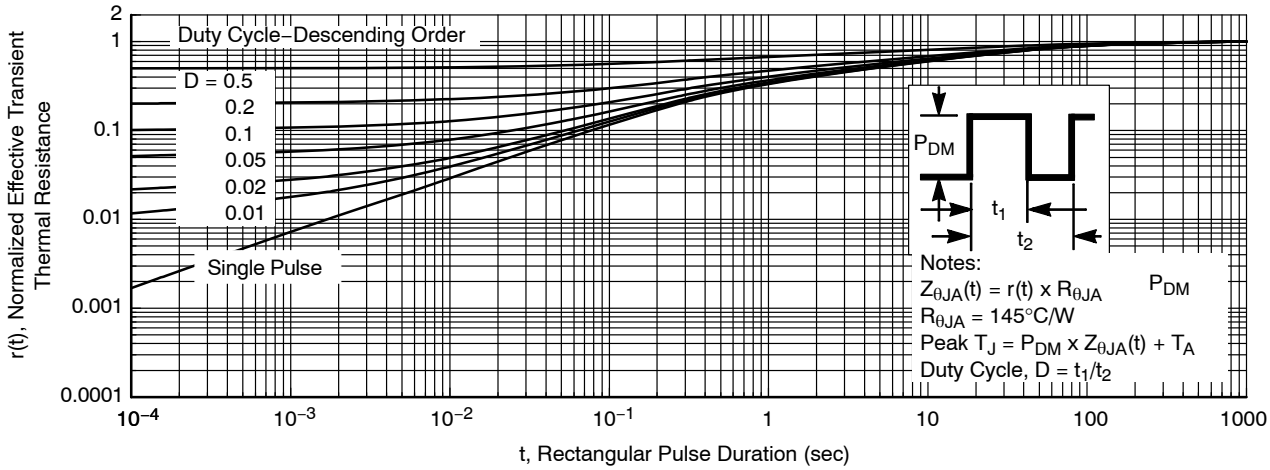


Figure 11. Junction−to−Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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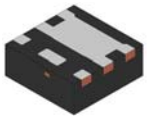

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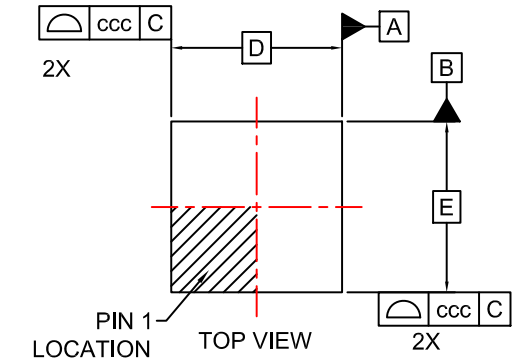
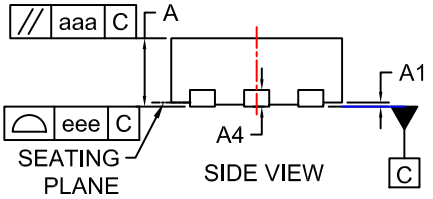
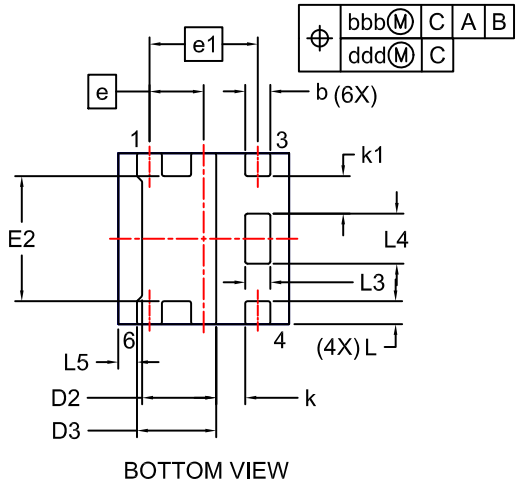
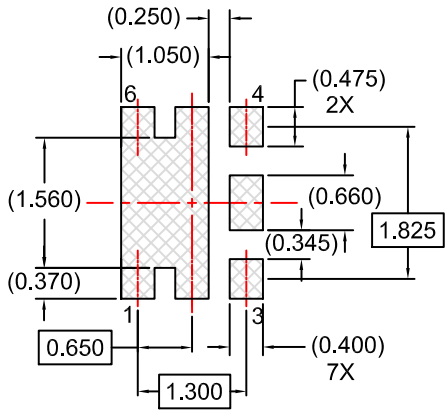






LAND PATTERN
RECOMMENDATION



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4		(0.20)	
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3		(0.95)	
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e		0.65 BSC	
e1		1.30 BSC	
k		(0.35)	
k1		(0.45)	
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5		(0.23)	
aaa		0.10	
bbb		0.10	
ccc		0.05	
ddd		0.05	
eee		0.05	

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