

MOSFET – Single, N-Channel, POWERTRENCH®

100 V, 3.3 A, 88 mΩ

FDMA86151L

General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $R_{DS(on)}$ and gate charge provide excellent switching performance.

Features

- Max $R_{DS(on)}$ = 88 mΩ @ $V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}$
- Max $R_{DS(on)}$ = 132 mΩ @ $V_{GS} = 4.5\text{ V}$, $I_D = 2.7\text{ A}$
- Low Profile – 0.8 mm Maximum in the New Package
MicroFET 2x2 mm
- Free from Halogenated Compounds and Antimony Oxides
- RoHS Compliant

Applications

- DC–DC Buck Converters

ABSOLUTE MAXIMUM RATINGS

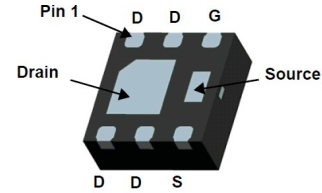
$T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 3)	3.3 20	A
P_D	Power Dissipation, $T_A = 25^\circ\text{C}$ (Note 1a) (Note 1b)	2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

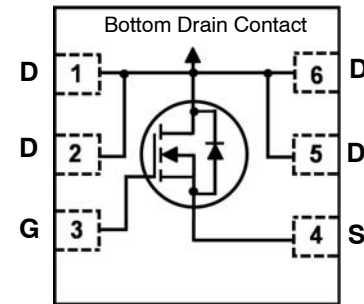
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a) (Note 1b)	52 145	°C/W

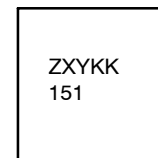


MicroFET 2x2 (Bottom View)

WDFN6 2x2, 0.65P
CASE 511DB



MARKING DIAGRAM



- Z = Assembly Plant Code
- XY = Date Code (Year & Week)
- KK = Lot Traceability Code
- 151 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMA86151L	WDFN6	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	69	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$	-	-	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	-6	-	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 3.3\ \text{A}$,	-	60	88	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 2.7\ \text{A}$	-	83	132	
		$V_{GS} = 10\ \text{V}, I_D = 3.3\ \text{A}$, $T_J = 125^\circ\text{C}$	-	102	150	
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 3.3\ \text{A}$	-	8.6	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	-	322	450	pF
C_{oss}	Output Capacitance		-	55	80	
C_{rss}	Reverse Transfer Capacitance		-	3	5	
R_G	Gate Resistance		0.1	1.9	3.8	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 3.3\ \text{A}$, $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$	-	5.6	12	ns
t_r	Rise Time		-	1.4	10	
$t_{d(off)}$	Turn-Off Delay Time		-	11	20	
t_f	Fall Time		-	1.6	10	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 10\ \text{V}, V_{DD} = 50\ \text{V}$, $I_D = 3.3\ \text{A}$	-	5.2	7.3	nC
		$V_{GS} = 0\ \text{V to } 4.5\ \text{V}, V_{DD} = 50\ \text{V}$, $I_D = 3.3\ \text{A}$	-	2.6	3.7	
Q_{gs}	Gate to Source Charge	$V_{DD} = 50\ \text{V}, I_D = 3.3\ \text{A}$	-	1.1	-	
Q_{gd}	Gate to Drain "Miller" Charge		-	1.0	-	

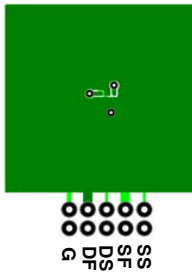
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 3.3\ \text{A}$ (Note 2)	-	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 3.3\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$	-	33	53	ns
Q_{rr}	Reverse Recovery Charge		-	25	40	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a $1\ \text{in}^2$ pad 2 oz copper pad on a $1.5 \times 1.5\ \text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $52^\circ\text{C}/\text{W}$ when mounted on a $1\ \text{in}^2$ pad of 2 oz. copper.



b) $145^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty Cycle $< 2.0\%$
- Pulsed I_D limited by junction temperature, $t_d < = 10\ \mu\text{s}$, please refer to SOA curve for more details.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

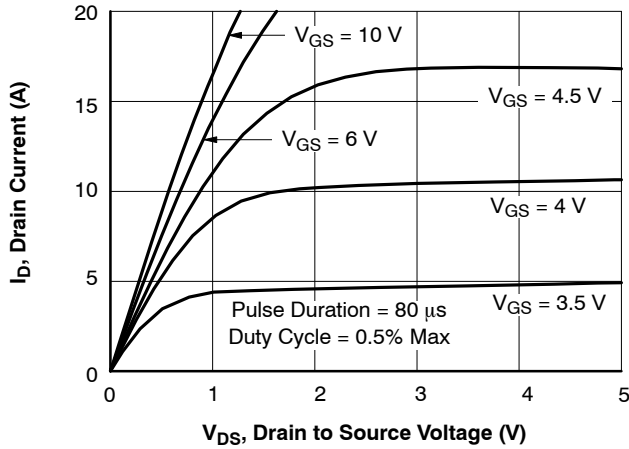


Figure 1. On-Region Characteristics

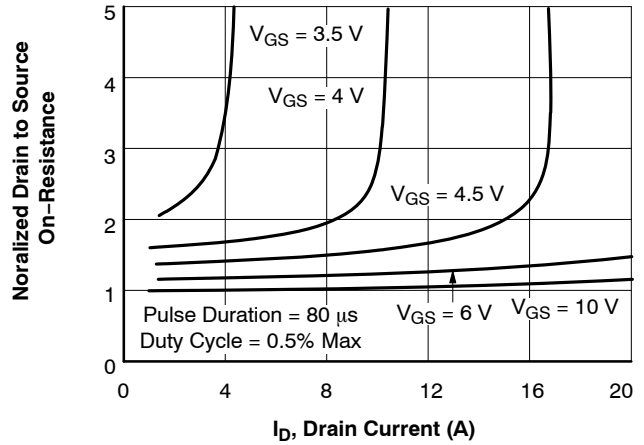


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

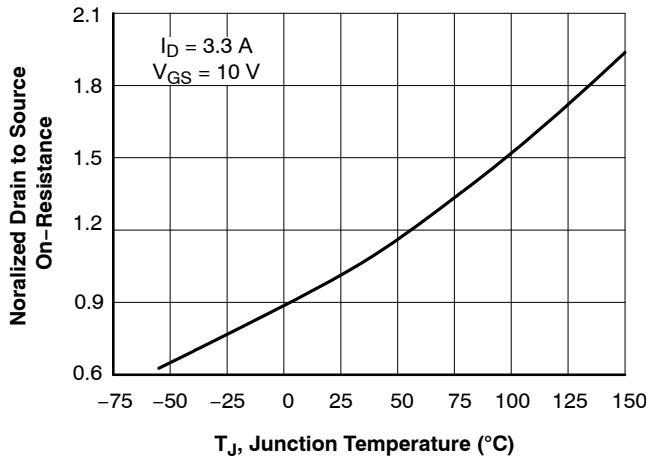


Figure 3. Normalized On-Resistance vs. Junction Temperature

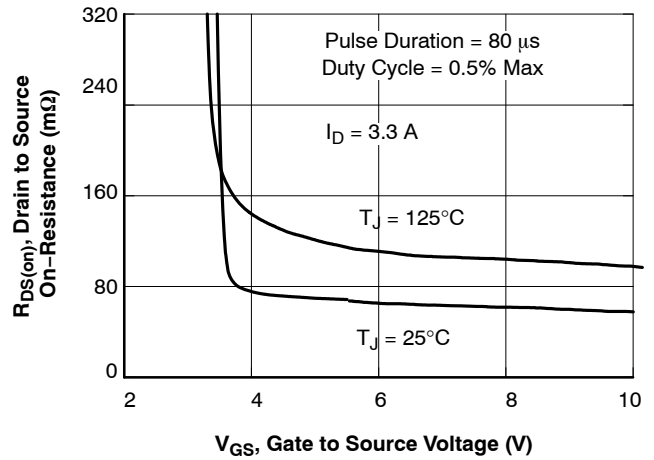


Figure 4. On-Resistance vs. Gate-to-Source Voltage

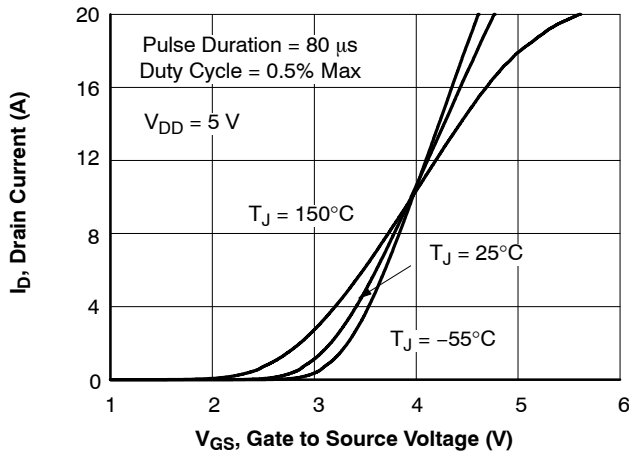


Figure 5. Transfer Characteristics

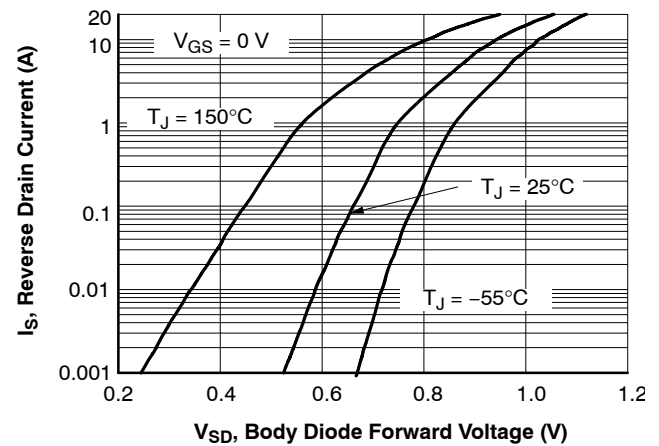


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

FDMA86151L

TYPICAL CHARACTERISTICS (Continued)

($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

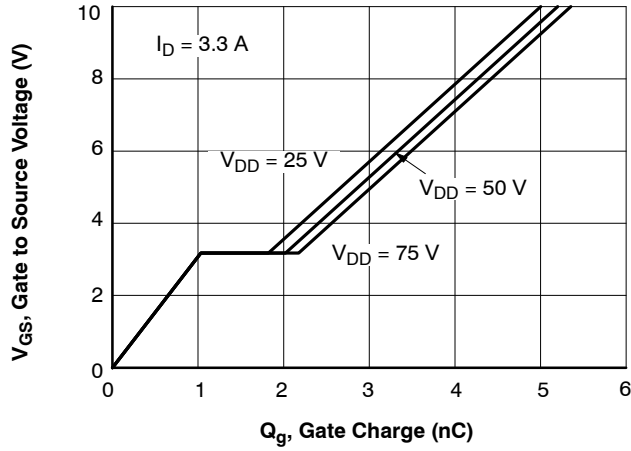


Figure 7. Gate Charge Characteristics

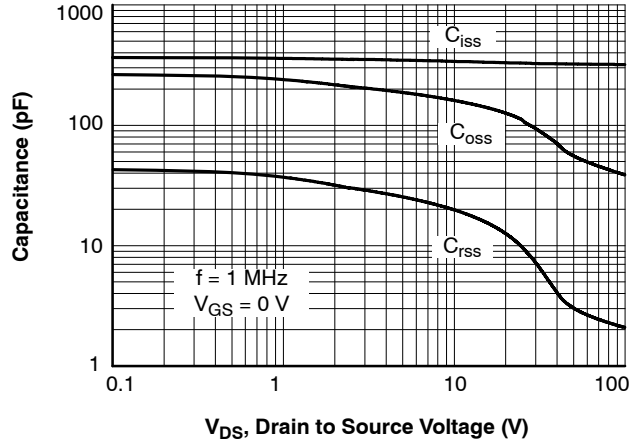


Figure 8. Capacitance vs Drain to Source Voltage

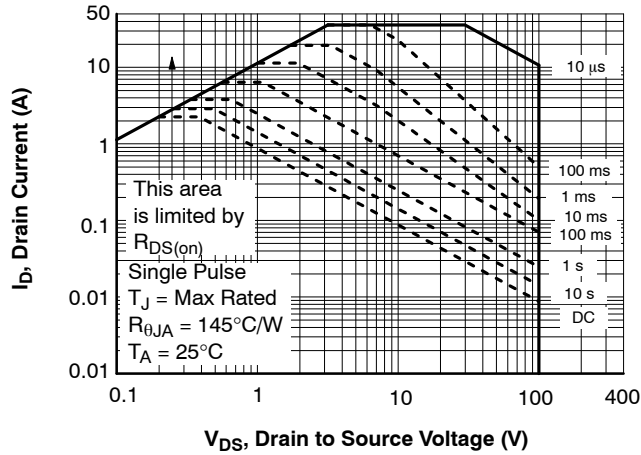


Figure 9. Forward Bias Safe Operating Area

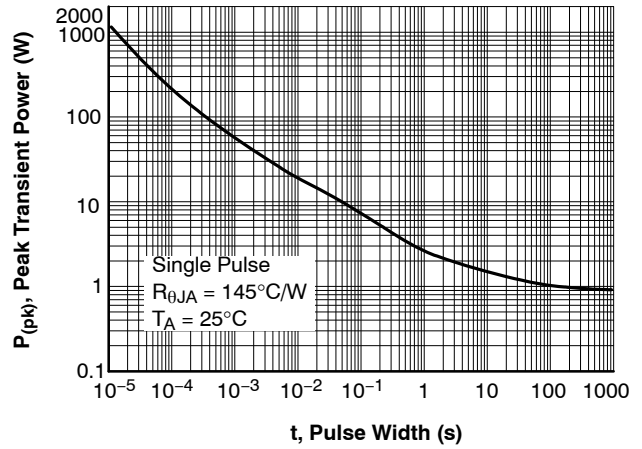


Figure 10. Single Pulse Maximum Power Dissipation

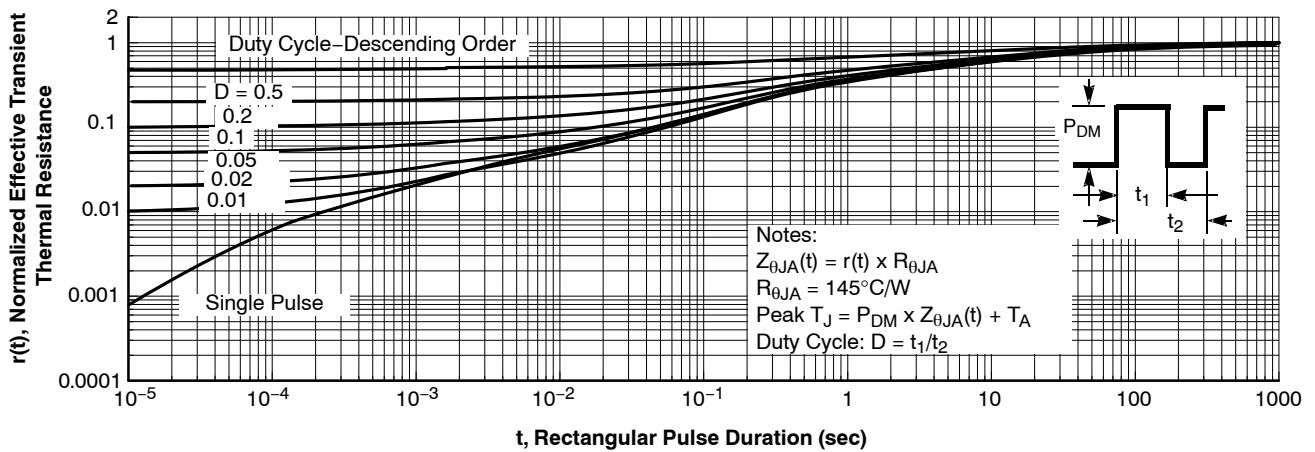


Figure 11. Single Junction-to-Ambient Transient Thermal Response Curve

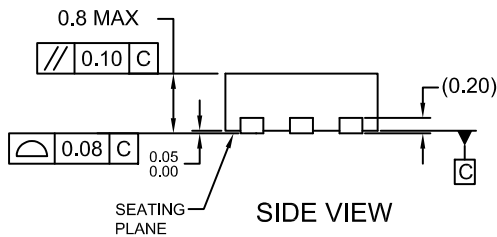
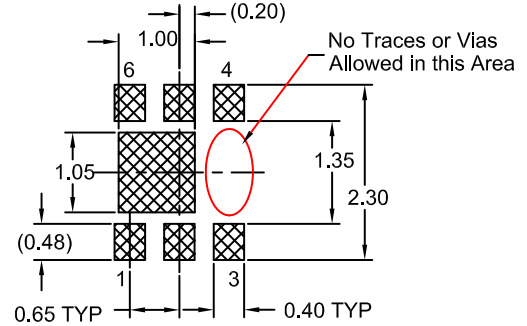
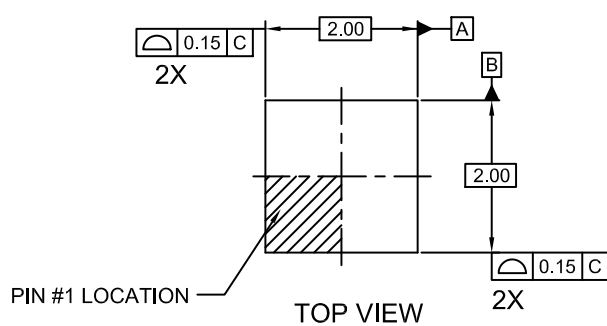
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

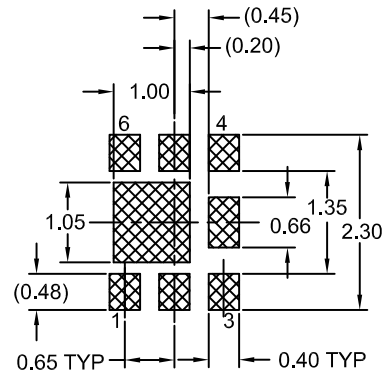
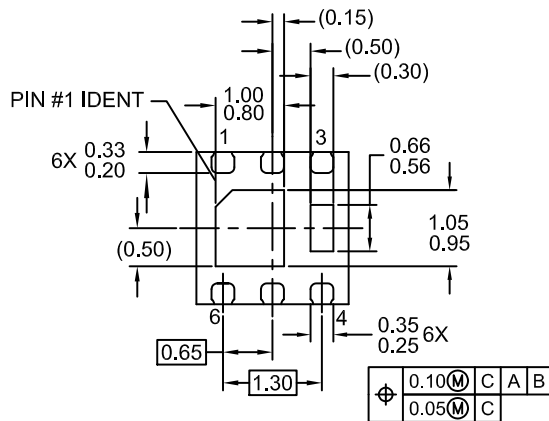


WDFN6 2x2, 0.65P
CASE 511DB
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN OPT 1



BOTTOM VIEW

RECOMMENDED LAND PATTERN OPT 2

NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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