June 2014

FDMA910PZ

Single P-Channel PowerTrench® MOSFET

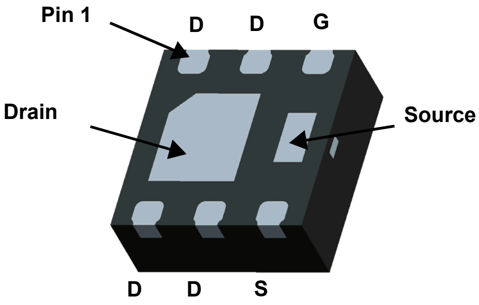
-20 V, -9.4 A, 20 mΩ

Features

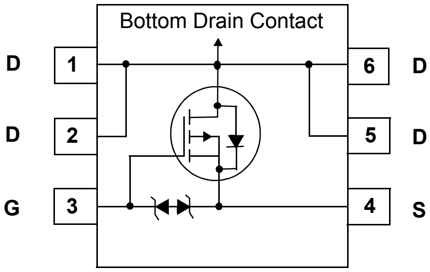
- Max $r_{DS(on)}$ = 20 mΩ at V_{GS} = -4.5 V, I_D = -9.4 A
- Max $r_{DS(on)}$ = 24 mΩ at V_{GS} = -2.5 V, I_D = -8.6 A
- Max $r_{DS(on)}$ = 34 mΩ at V_{GS} = -1.8 V, I_D = -7.2 A
- Low Profile - 0.8 mm maximum in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2.8k V typical (Note 3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications.It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	-Continuous T_A = 25°C (Note 1a)	-9.4	A
	-Pulsed	-45	
P_D	Power Dissipation T_A = 25°C (Note 1a)	2.4	W
	Power Dissipation T_A = 25°C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

Package Marking and Ordering Information

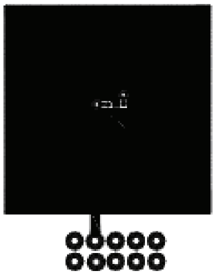
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
910	FDMA910PZ	MicroFET 2X2	7”	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

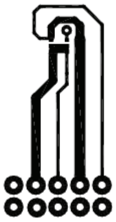
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±1	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -9.4 A		16	20	mΩ
		V_{GS} = -2.5 V, I_D = -8.6 A		19	24	
		V_{GS} = -1.8 V, I_D = -7.2 A		24	34	
		V_{GS} = -4.5 V, I_D = -9.4 A, T_J = 125 °C		20	25	
g_{FS}	Forward Transconductance	V_{DD} = -5 V, I_D = -9.4 A		52		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz		2110	2805	pF
C_{oss}	Output Capacitance			414	620	pF
C_{rss}	Reverse Transfer Capacitance			388	580	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -9.4 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		9.4	19	ns
t_r	Rise Time			19	34	ns
$t_{d(off)}$	Turn-Off Delay Time			135	216	ns
t_f	Fall Time			103	165	ns
Q_g	Total Gate Charge	V_{GS} = -4.5 V, V_{DD} = -10 V, I_D = -9.4 A		21	29	nC
Q_{gs}	Gate to Source Charge			2.5		nC
Q_{gd}	Gate to Drain “Miller” Charge			6		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.6	-1.2	V
		V_{GS} = 0 V, I_S = -9.4 A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -9.4 A, di/dt = 100 A/μs		23	37	ns
Q_{rr}	Reverse Recovery Charge			6.3	13	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

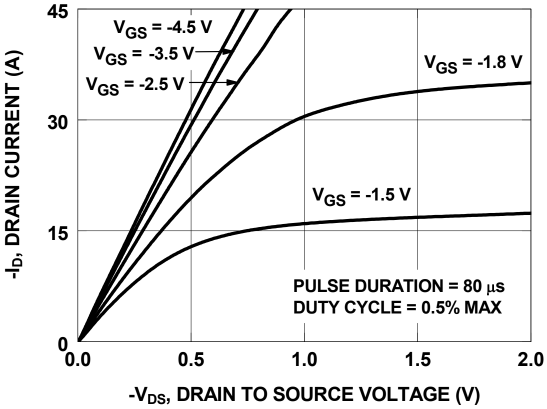


Figure 1. On-Region Characteristics

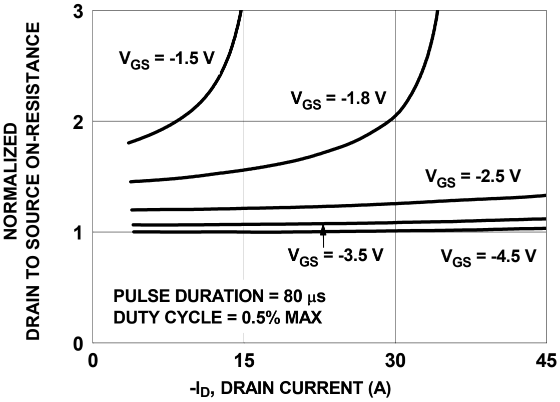


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

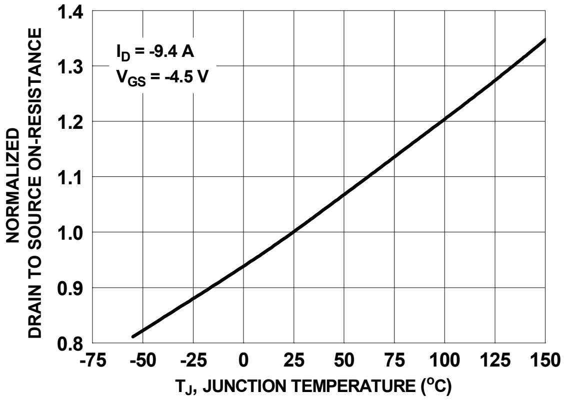


Figure 3. Normalized On-Resistance vs Junction Temperature

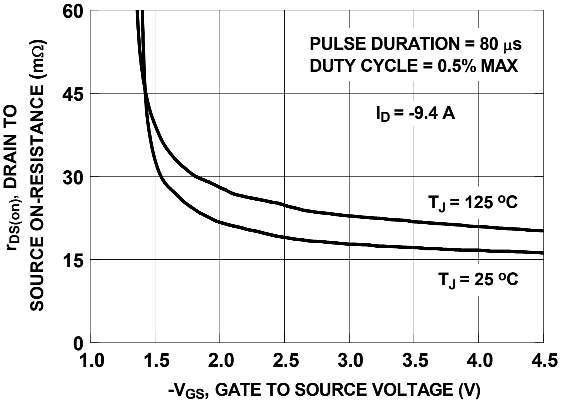


Figure 4. On-Resistance vs Gate to Source Voltage

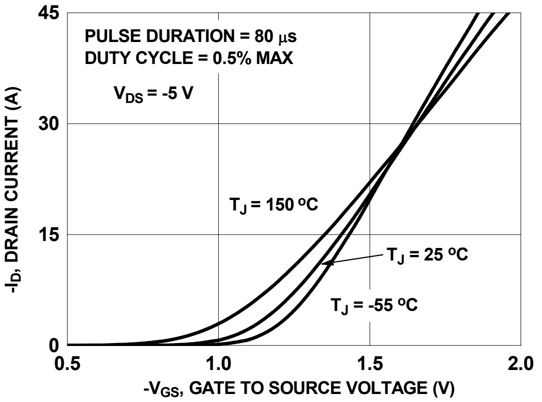


Figure 5. Transfer Characteristics

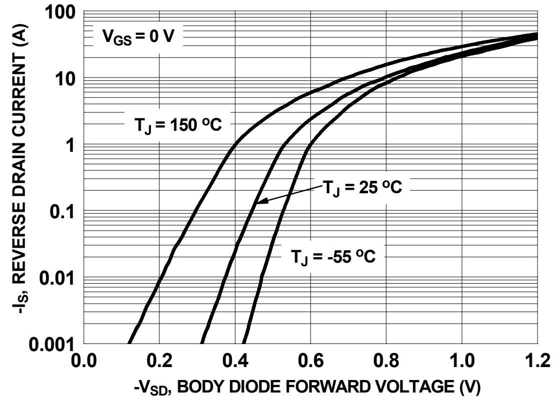


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

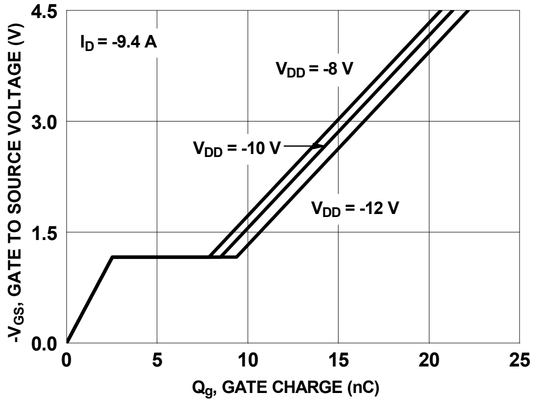


Figure 7. Gate Charge Characteristics

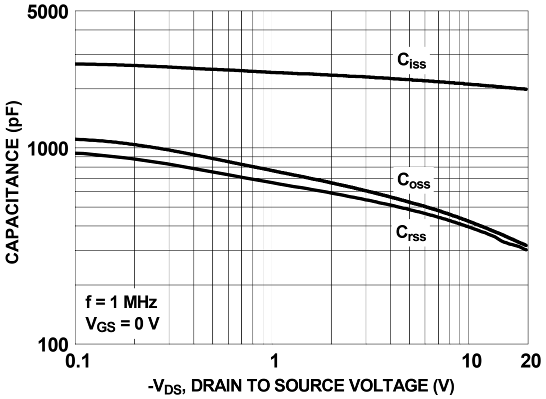


Figure 8. Capacitance vs Drain to Source Voltage

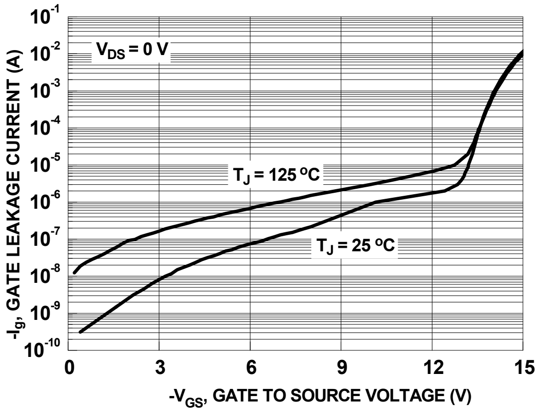


Figure 9. Gate Leakage Current vs Gate to Source Voltage

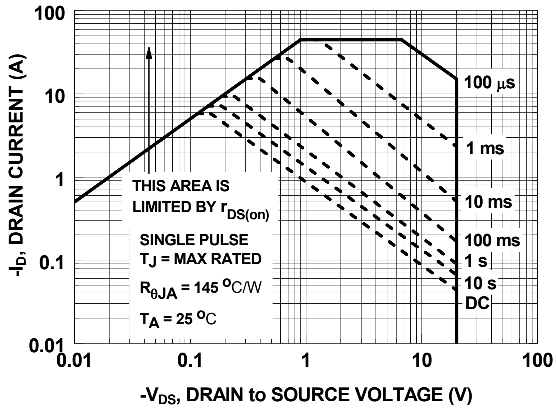


Figure 10. Forward Bias Safe Operating Area

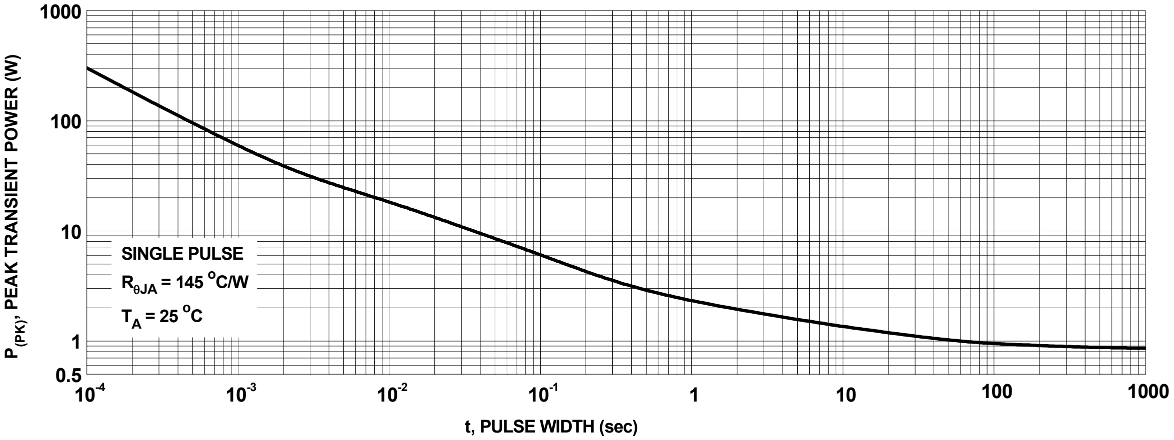


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

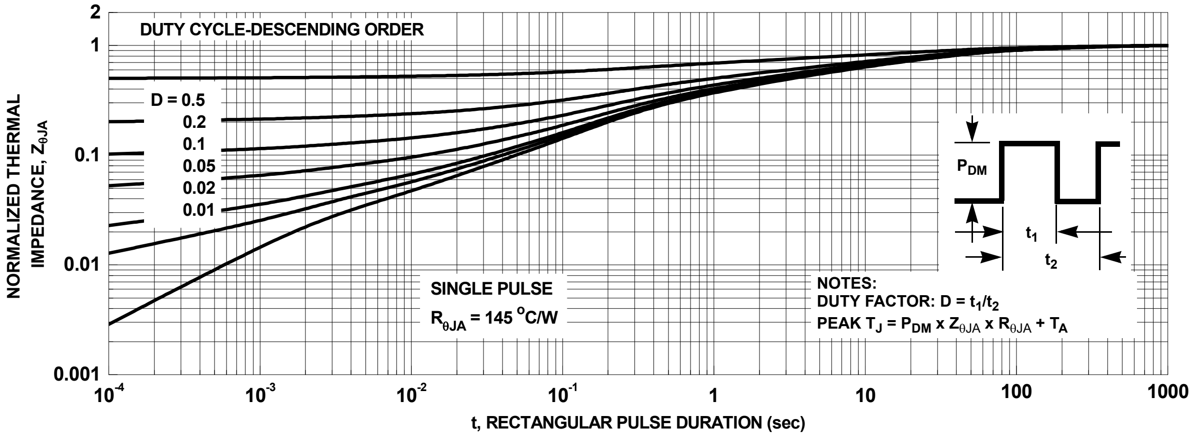
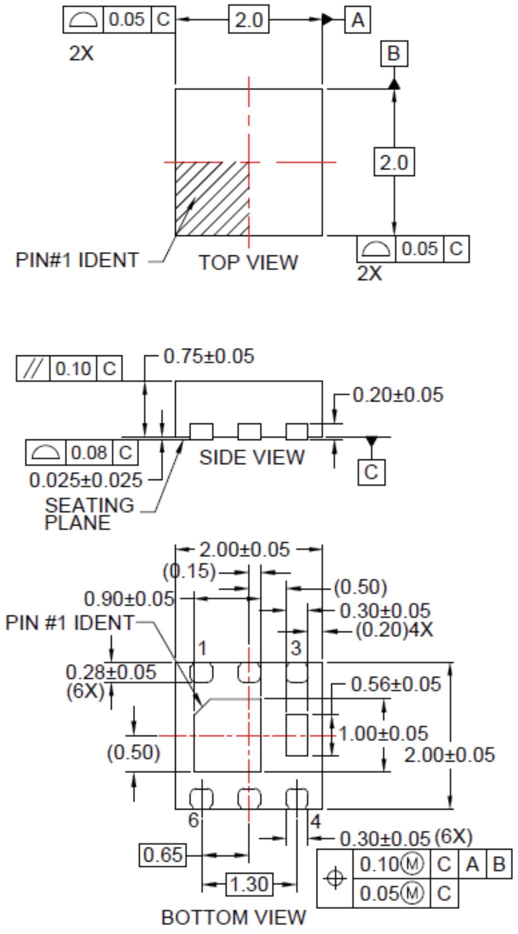
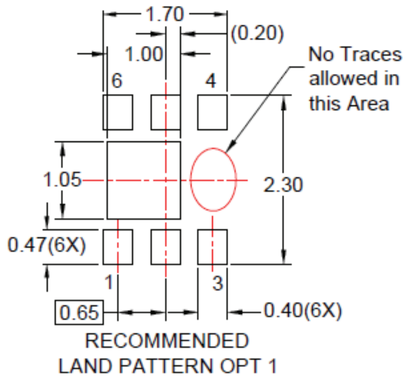
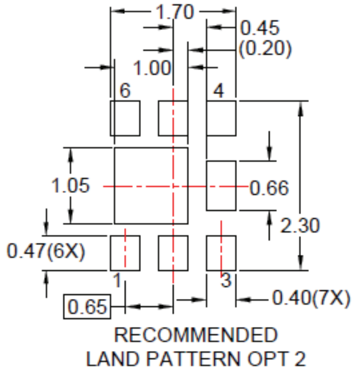


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout







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