



# FDMB2308PZ

## Dual Common Drain P-Channel PowerTrench<sup>®</sup> MOSFET -20 V, -7 A, 36 mΩ

### Features

- Max  $r_{S1S2(on)}$  = 36 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -5.7$  A
- Max  $r_{S1S2(on)}$  = 50 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -4.6$  A
- Low Profile - 0.8 mm maximum - in the new package MicroFET 2x3 mm
- HBM ESD protection level 2.8 kV (Note 3)
- RoHS Compliant

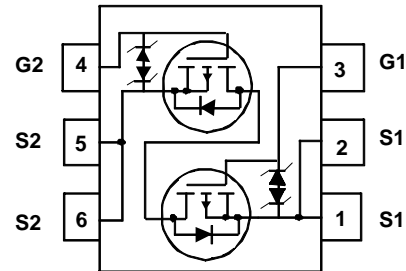
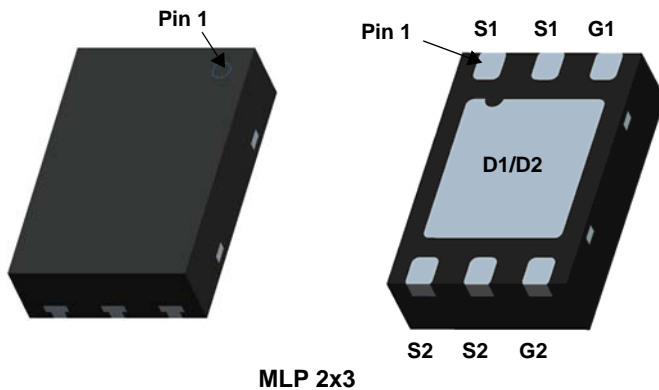


### General Description

This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain P-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench<sup>®</sup> process with state of the art MircoFET Leadframe, the FDMB2308PZ minimizes both PCB space and  $r_{S1S2(on)}$ .

### Application

- Li-Ion Battery Pack



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{S1S2}$	Source1 to Source2 Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_{S1S2}$	Source1 to Source2 Current -Continuous $T_A = 25$ °C (Note 1a)	-7	A
	-Pulsed	-30	
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	2.2	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	161	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
308	FDMB2308PZ	MLP 2x3	7"	8 mm	3000 units

### Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Off Characteristics

$I_{S1S2}$	Zero Gate Voltage Source1 to Source2 Current	$V_{S1S2} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{S1S2} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} = -250\text{ }\mu\text{A}$	-0.6	-0.9	-1.5	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	$V_{GS} = -4.5\text{ V}, I_{S1S2} = -5.7\text{ A}$		27	36	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_{S1S2} = -4.6\text{ A}$		36	50	
		$V_{GS} = -4.5\text{ V}, I_{S1S2} = -5.7\text{ A}, T_J = 125\text{ }^\circ\text{C}$		35	49	
$g_{FS}$	Forward Transconductance	$V_{S1S2} = -5\text{ V}, I_{S1S2} = -5.7\text{ A}$		29		S

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{S1S2} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2280	3030	pF
$C_{oss}$	Output Capacitance			361	540	pF
$C_{rss}$	Reverse Transfer Capacitance			339	510	pF

#### Switching Characteristics

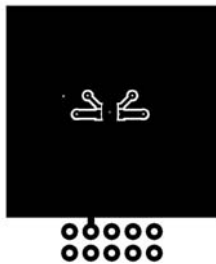
$t_{d(on)}$	Turn-On Delay Time	$V_{S1S2} = -10\text{ V}, I_{S1S2} = -5.7\text{ A}, V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		14	25	ns
$t_r$	Rise Time			33	52	ns
$t_{d(off)}$	Turn-Off Delay Time			74	118	ns
$t_f$	Fall Time			58	93	ns
$Q_g$	Total Gate Charge		$V_{S1S2} = -10\text{ V}, I_{S1S2} = -5.7\text{ A}, V_{G1S1} = -4.5\text{ V}, V_{G2S2} = 0\text{ V}$		22	30
$Q_{gs}$	Gate1 to Source1 Charge			3.6		nC
$Q_{gd}$	Gate1 to Source2 "Miller" Charge			7.7		nC

#### Source1- Source2 Diode Characteristics

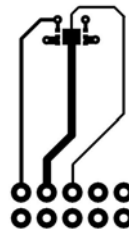
$I_{fss}$	Maximum Continuous Source1-Source2 Diode Forward Current				-5.7	A
$V_{fss}$	Source1 to Source2 Diode Forward Voltage	$V_{G1S1} = 0\text{ V}, V_{G2S2} = -4.5\text{ V}, I_{fss} = -5.7\text{ A}$ (Note 2)		-1	-1.6	V

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 57  $^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

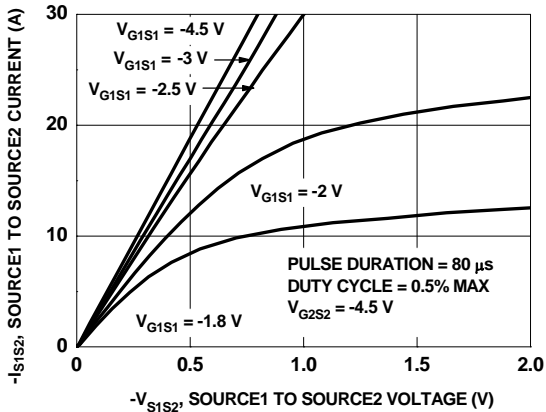


b. 161  $^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

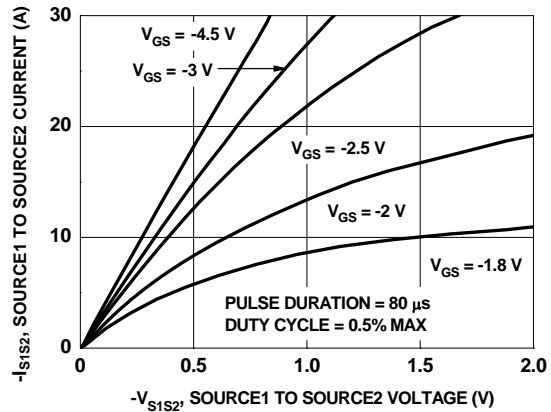
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

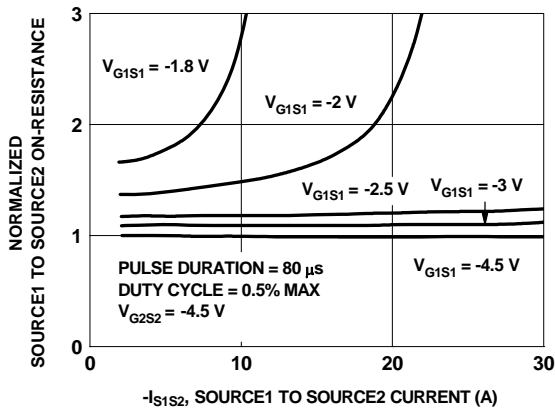
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



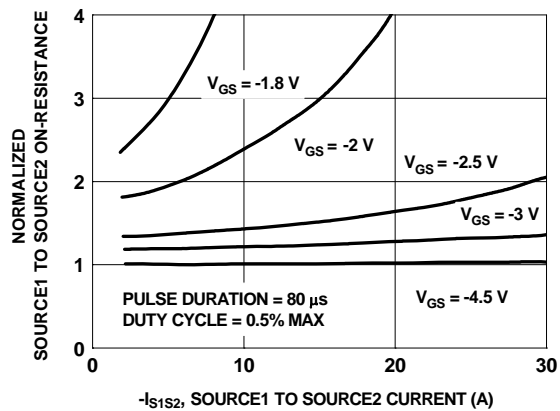
**Figure 1. On-Region Characteristics**



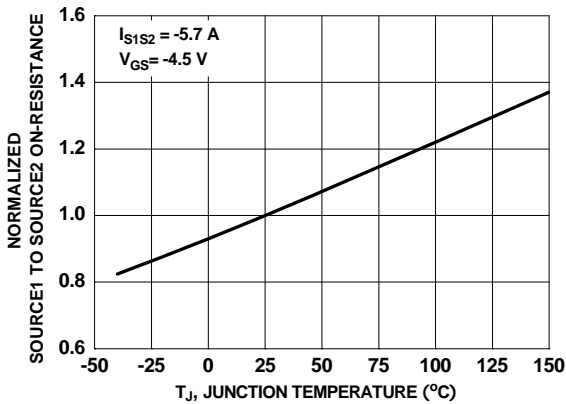
**Figure 2. On-Region Characteristics**



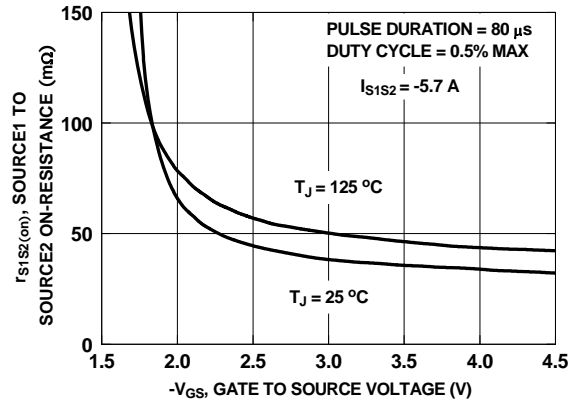
**Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage**



**Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage**

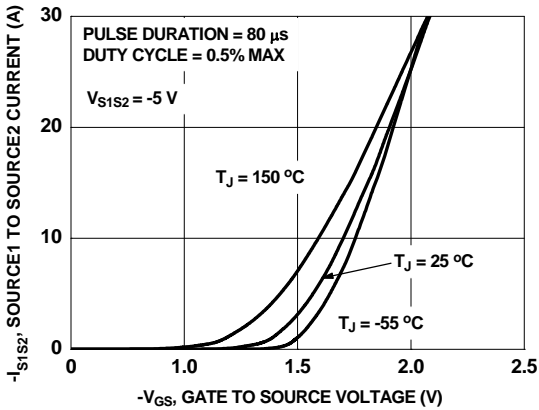


**Figure 5. Normalized On Resistance vs Junction Temperature**

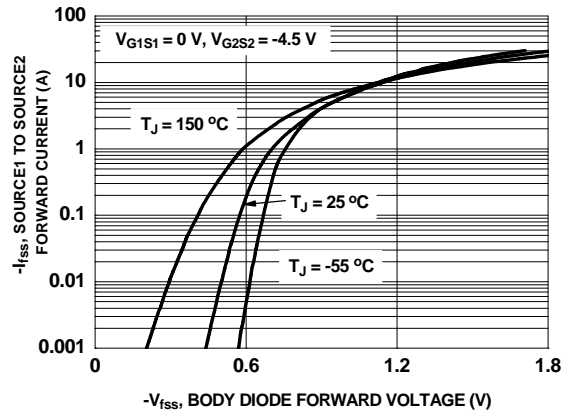


**Figure 6. On Resistance vs Gate to Source Voltage**

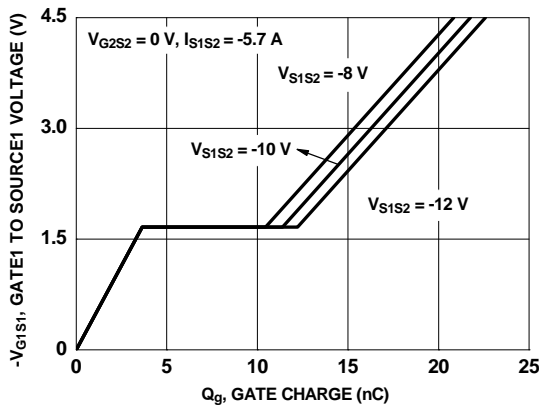
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



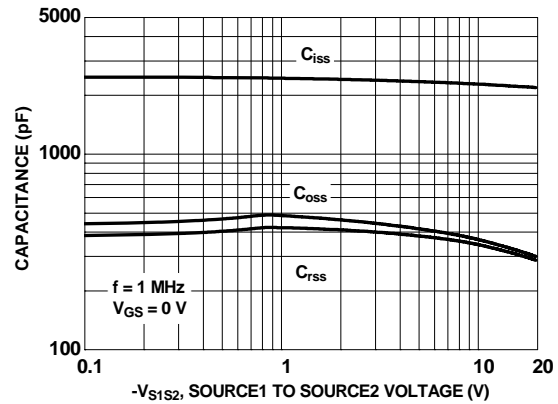
**Figure 7. Transfer Characteristics**



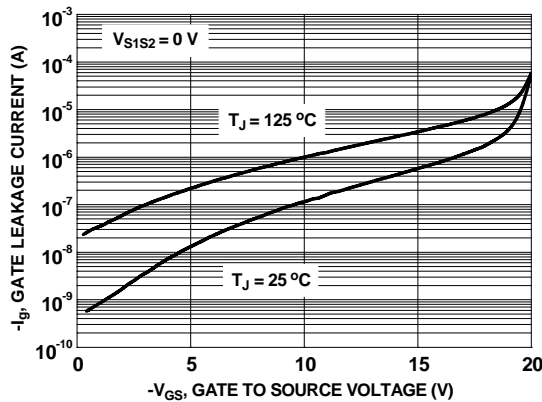
**Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current**



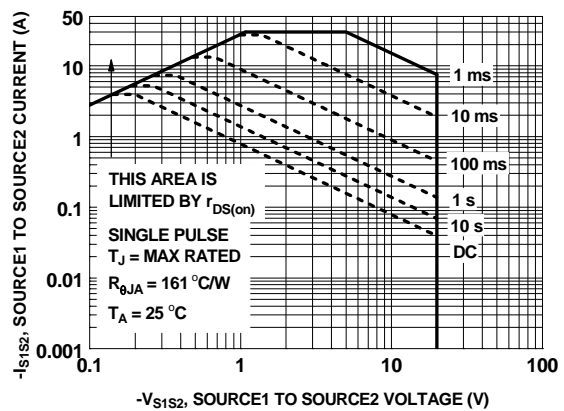
**Figure 9. Gate Charge Characteristics**



**Figure 10. Capacitance vs Source1 to Source2 Voltage**

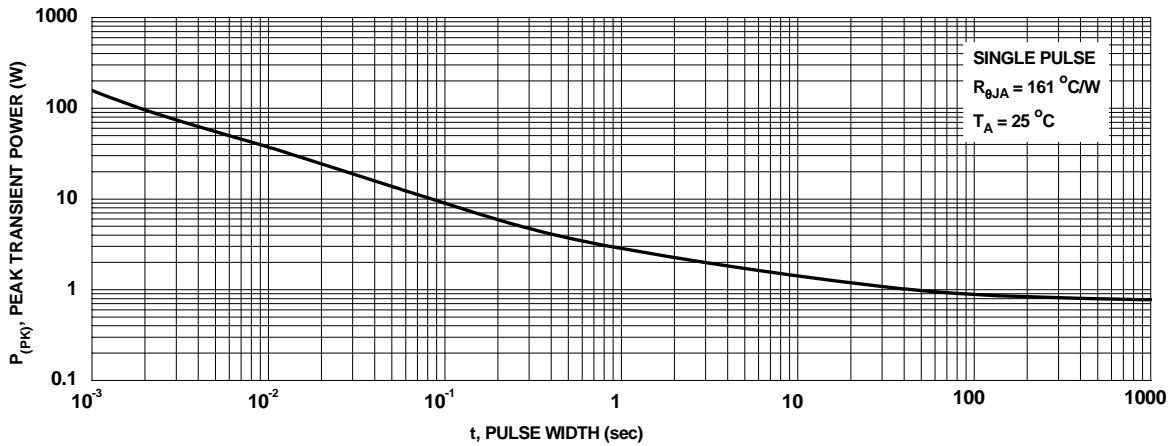


**Figure 11. Gate Leakage Current vs Gate to Source Voltage**

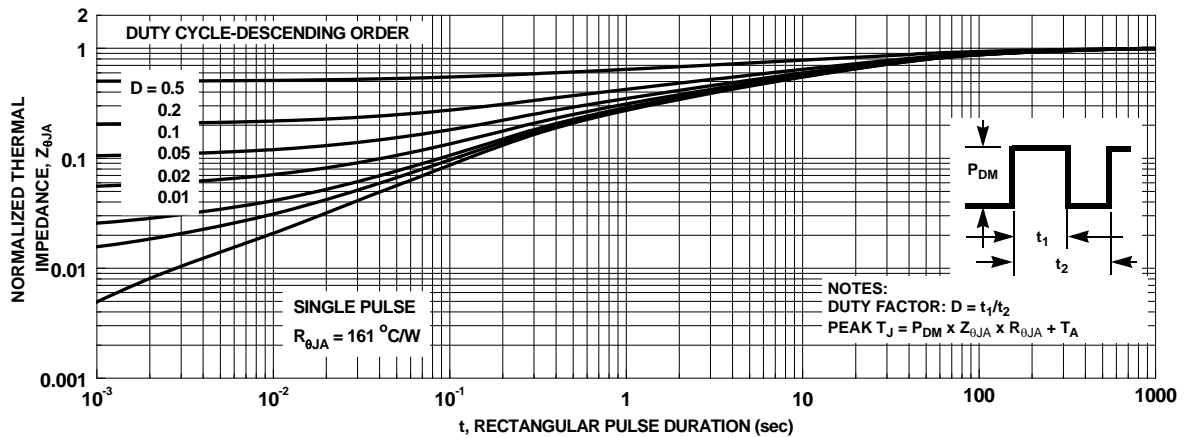


**Figure 12. Forward Bias Safe Operating Area**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

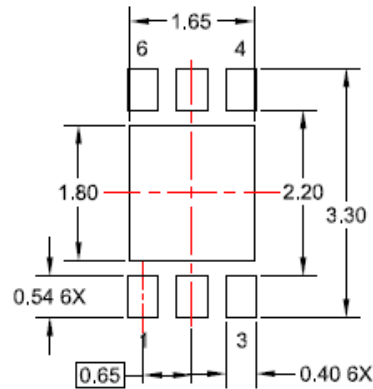
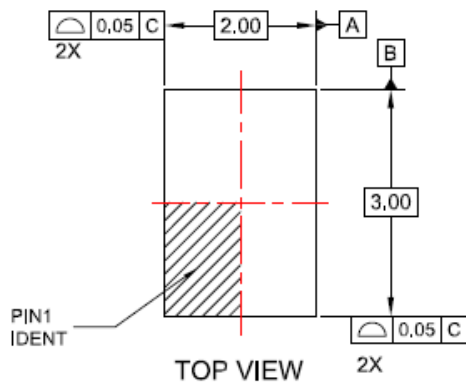


**Figure 13. Single Pulse Maximum Power Dissipation**

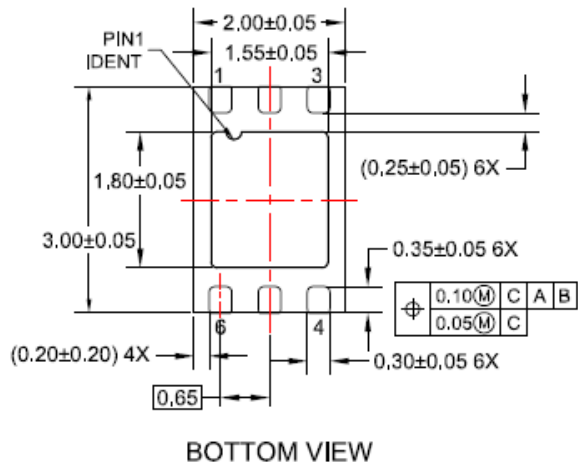
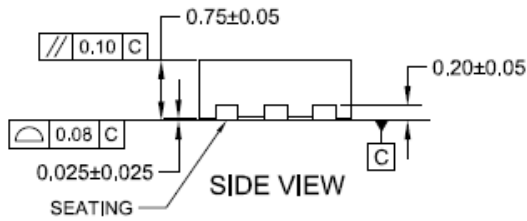


**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN



### NOTES:

- PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.
- DRAWING FILENAME: MKT-MLP06Qrev3.
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