

# MOSFET – Power, N-Channel, UltraFET

55 V, 15 A, 90 mΩ

## FDMC15N06

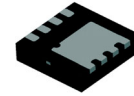
### Description

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance.

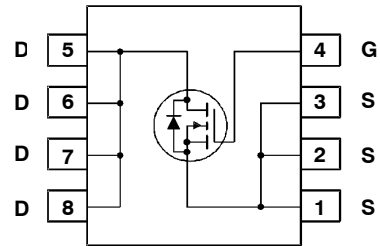
This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low voltage bus switches, and power management in portable and battery-operated products.

### Features

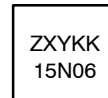
- $R_{DS(on)} = 75 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 15 \text{ A}$
- 100% Avalanche Tested
- These Device is Pb-Free and RoHS Compliant



WDFN8 3.3X3.3, 0.65P  
CASE 511DQ



### MARKING DIAGRAM



- Z = Assembly Plant Code
- XY = Date Code (Year & Week)
- KK = Lot Traceability Code
- 15N06 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDMC15N06	WDFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# FDMC15N06

## MOSFET MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain to Source Voltage	55	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current –Continuous ( $T_C = 25^\circ\text{C}$ ) –Continuous ( $T_C = 100^\circ\text{C}$ ) –Continuous ( $T_A = 25^\circ\text{C}$ ) (Note 3)	15 9 2.4	A
$I_{DM}$	Drain Current –Pulsed (Note 4)	60	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 5)	36	mJ
$I_{AR}$	Avalanche Energy	15	A
$E_{AR}$	Repetitive Avalanche Energy	3.5	mJ
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) ( $T_A = 25^\circ\text{C}$ )	35 2.3	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+150$	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max (Note 3)	53	

## ELECTRICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_C = 25^\circ\text{C}$	55	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	70	–	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 45 \text{ V}, T_C = 150^\circ\text{C}$	–	–	1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$	–	0.075	0.090	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 15 \text{ A}$	–	5	–	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	–	265	350	pF
$C_{oss}$	Output Capacitance		–	97	130	pF
$C_{rss}$	Reverse Transfer Capacitance		–	28	42	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 30 \text{ V}, I_D = 15 \text{ A},$ $V_{GS} = 10 \text{ V}$ (Note 4)	–	8.8	11.5	nC
$Q_{gs}$	Gate to Source Gate Charge		–	1.7	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	3.6	–	nC

# FDMC15N06

## ELECTRICAL CHARACTERISTICS $T_c = 25\text{ }^\circ\text{C}$ unless otherwise noted. (continued)

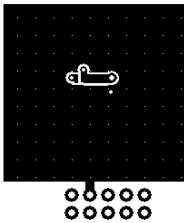
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}$ , $I_D = 15\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_G = 25\text{ }\Omega$ (Note 6)	–	9.5	29	ns
$t_r$	Turn-On Rise Time		–	36.5	83	ns
$t_{d(off)}$	Turn-Off Delay Time		–	22.5	55	ns
$t_f$	Turn-Off Fall Time		–	22	54	ns

### Drain-Source Diode Characteristics

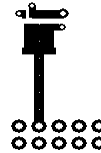
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		–	–	15	A
			–	–	60	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		–	–	1.25	V
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 15\text{ A}$				
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}$ , $I_{SD} = 15\text{ A}$ , $di_F/dt = 100\text{ A}/\mu\text{s}$ (Note 7)	–	30	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	35	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

4. Repetitive rating: pulse-width limited by maximum junction temperature.
5.  $L = 1\text{ mH}$ ,  $I_{AS} = 8.5\text{ A}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25\text{ }^\circ\text{C}$ .
6. Essentially independent of operating temperature typical characteristics.
7.  $I_{SD} \leq 15\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 40\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ .

TYPICAL CHARACTERISTICS

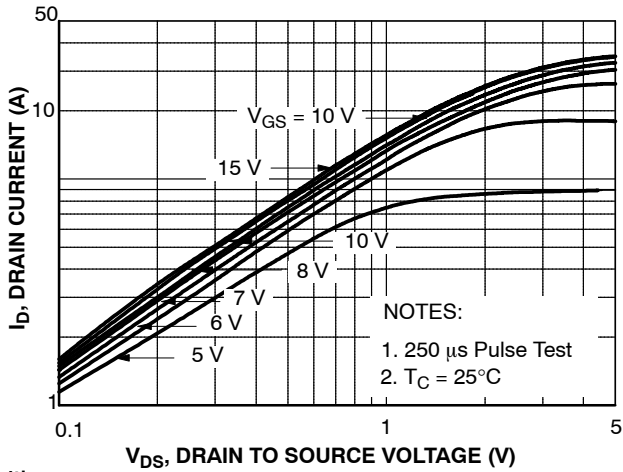


Figure 12. On-Region Characteristics

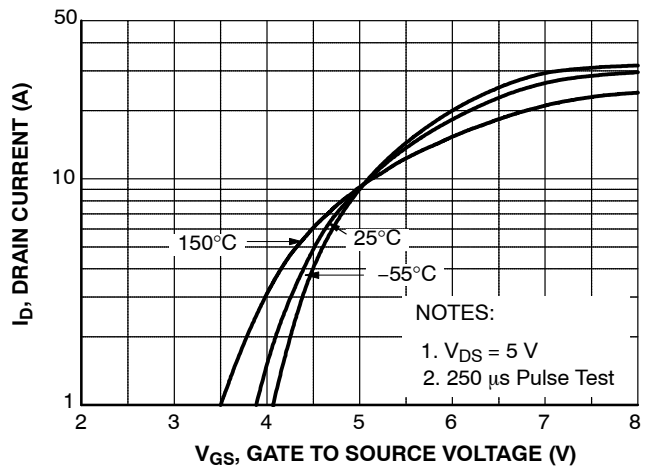


Figure 13. Transfer Characteristics

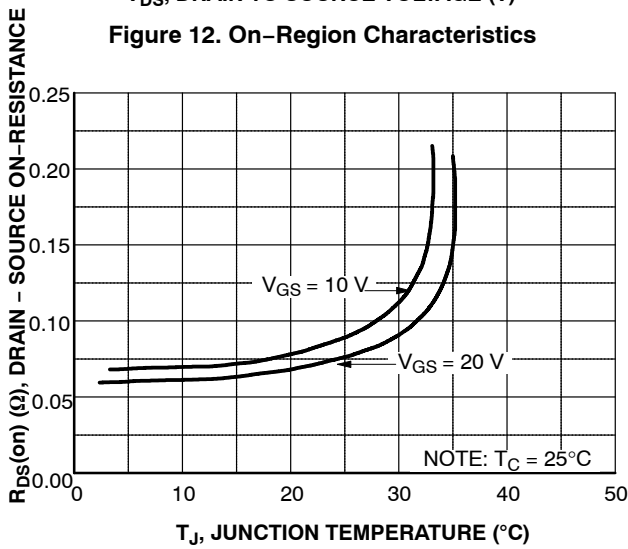


Figure 14. On-Resistance Variation vs. Drain Current and Gate Voltage

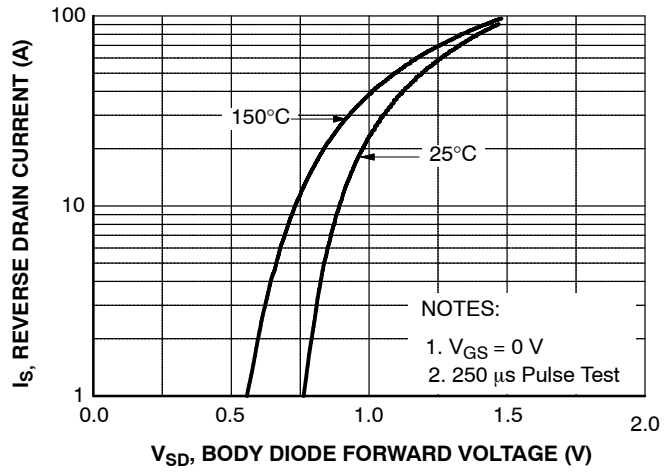


Figure 15. Body Diode Forward Voltage Variation vs. Source Current and Temperature

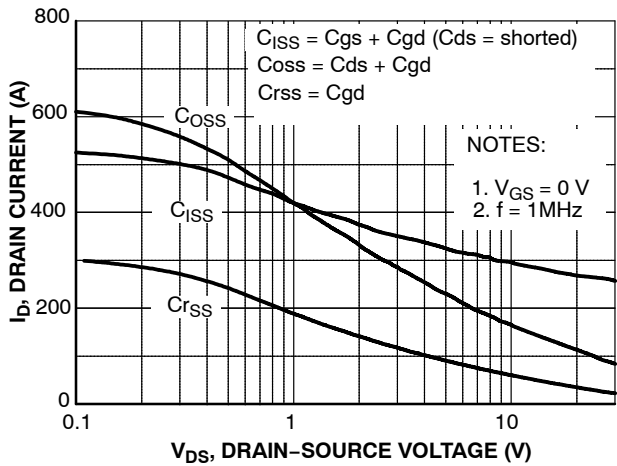


Figure 16. Capacitance Characteristics

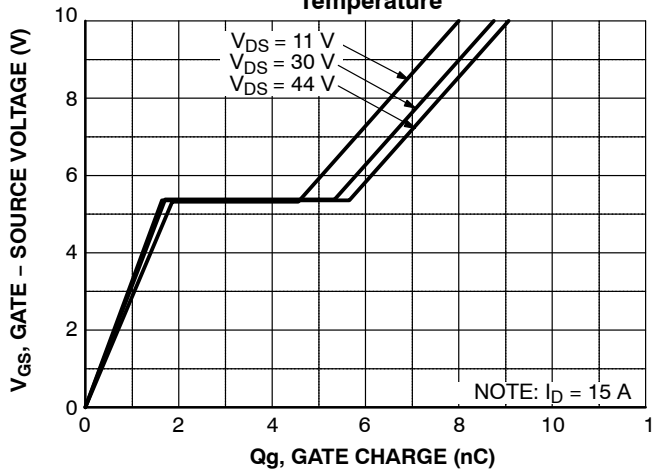


Figure 17. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

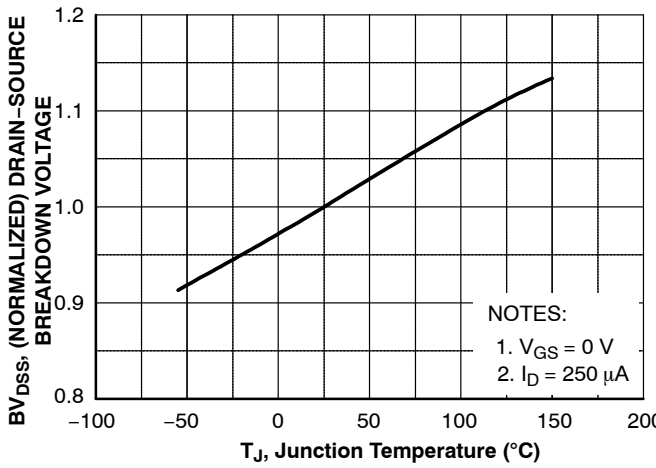


Figure 18. Breakdown Voltage Variation vs. Temperature

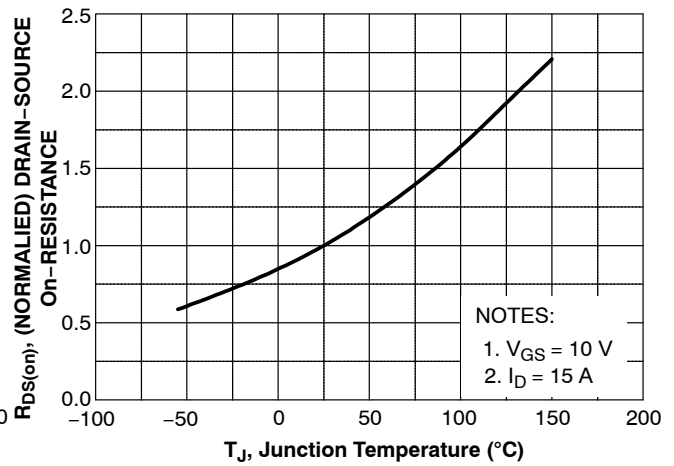


Figure 19. On-Resistance Variation vs. Temperature

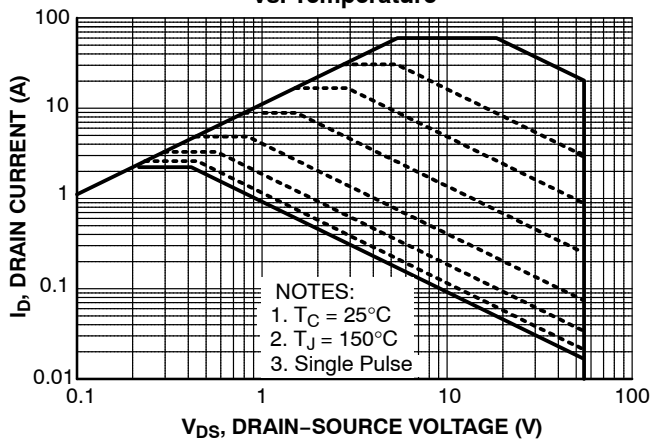


Figure 20. Unclamped Inductive Switching Capability

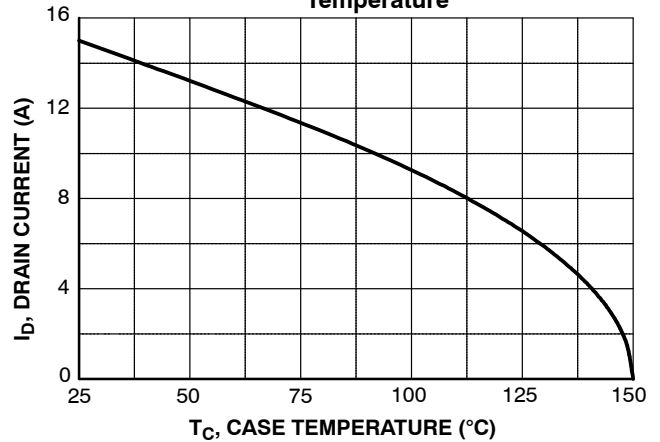


Figure 21. Maximum Drain Current vs. Case Temperature

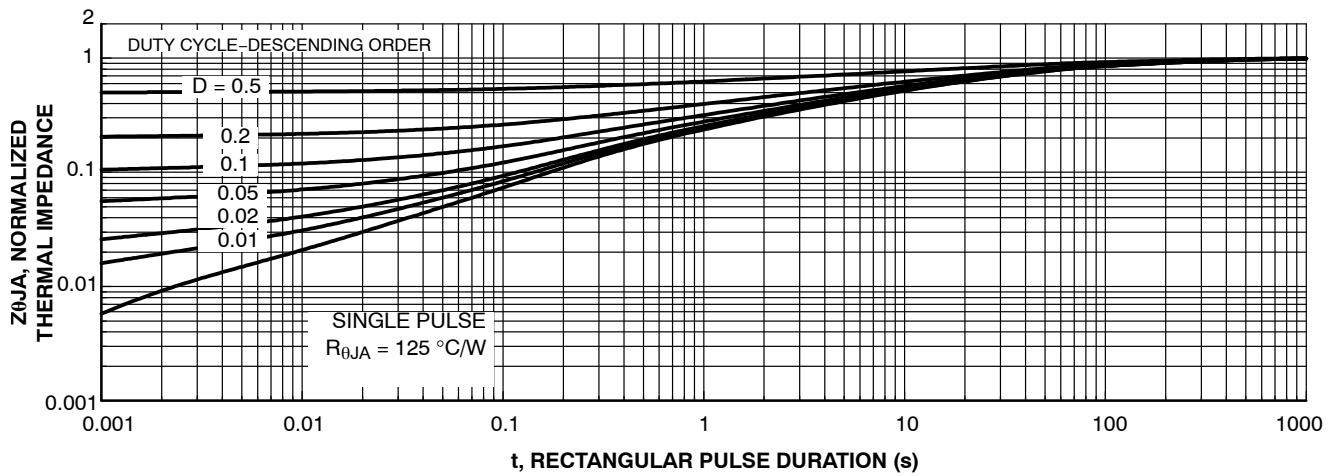


Figure 22. Thermal Response Curve

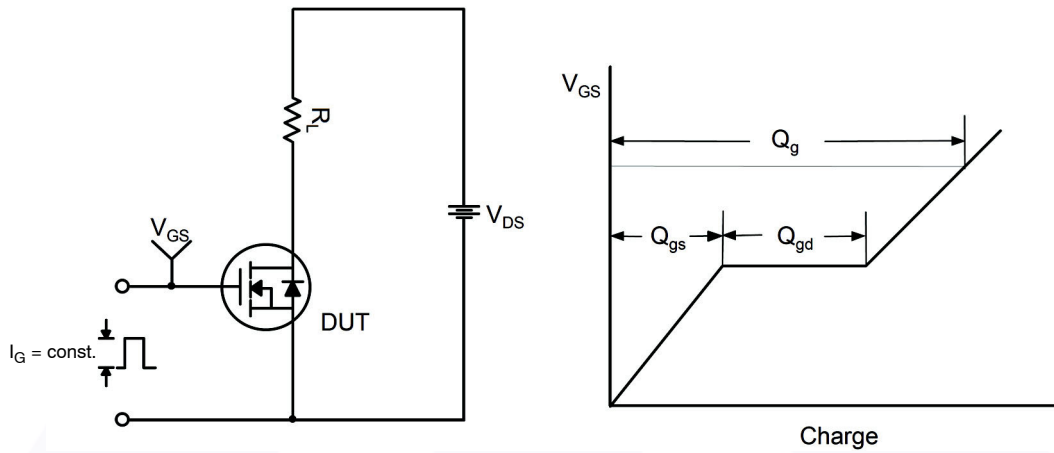


Figure 12. Gate Charge Test Circuit & Waveform

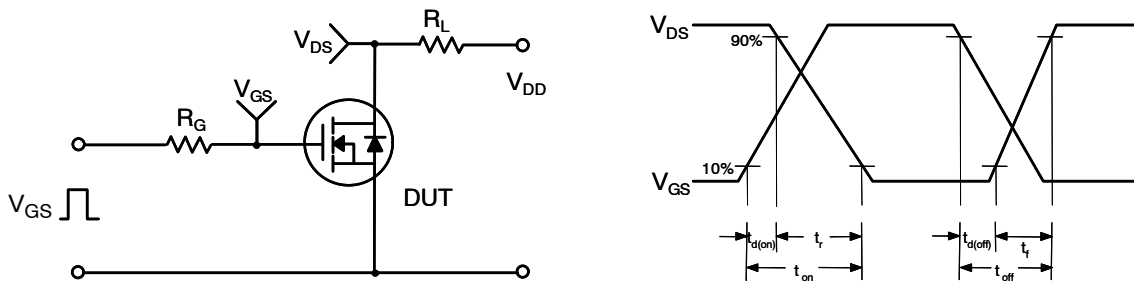


Figure 13. Resistive Switching Test Circuit & Waveforms

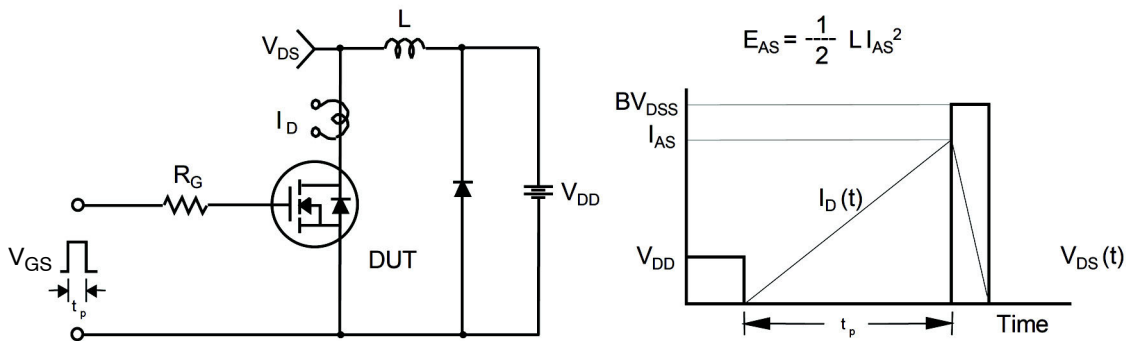
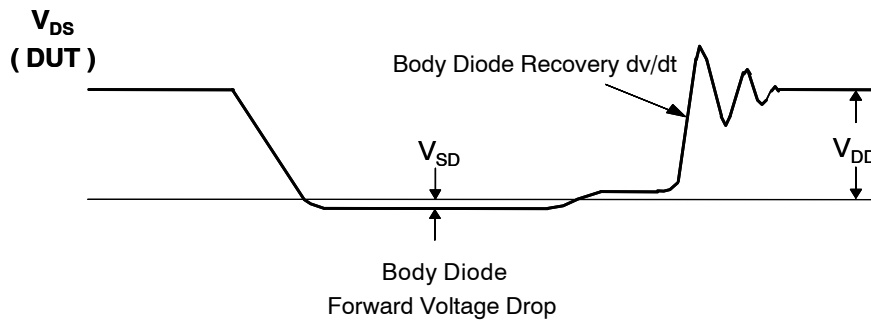
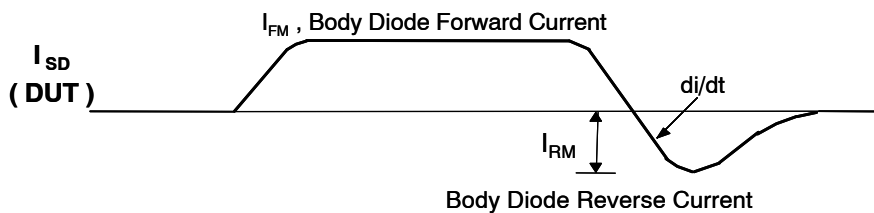
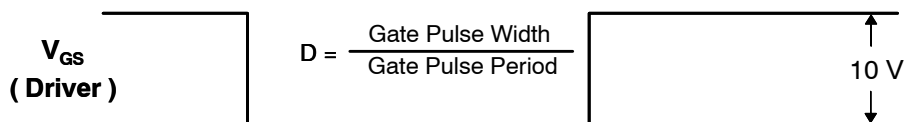
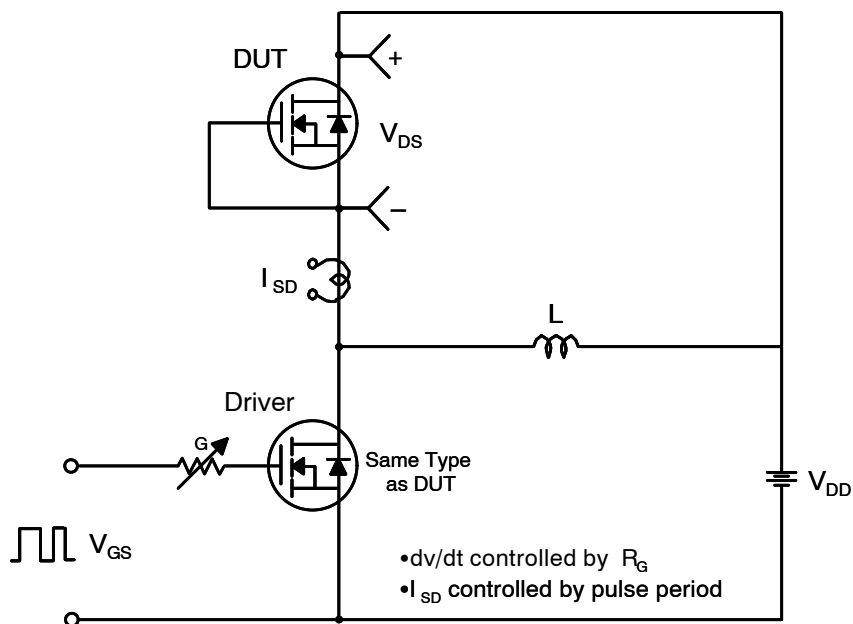


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

# FDMC15N06



**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

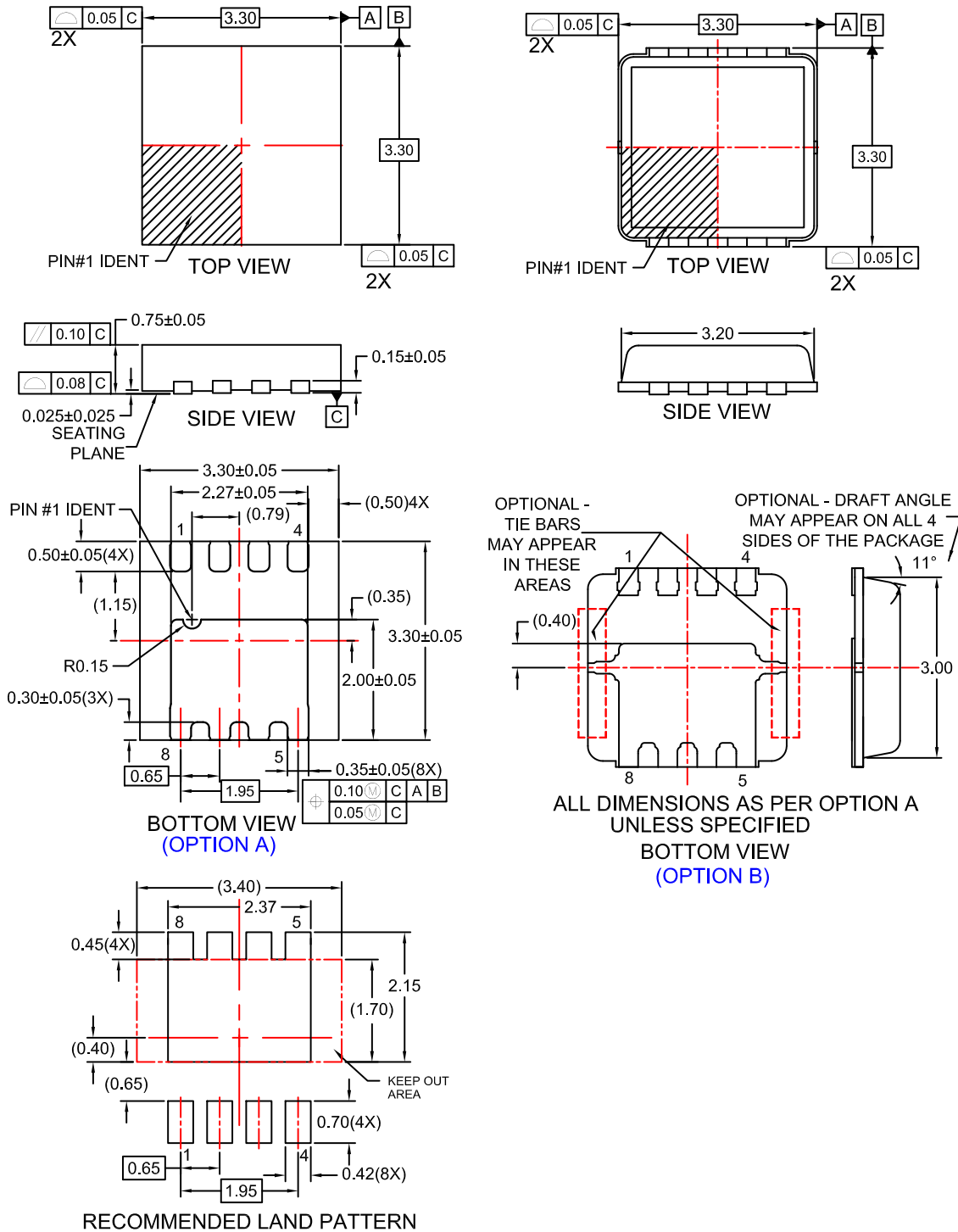
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## WDFN8 3.3x3.3, 0.65P CASE 511DQ ISSUE O

DATE 31 OCT 2016



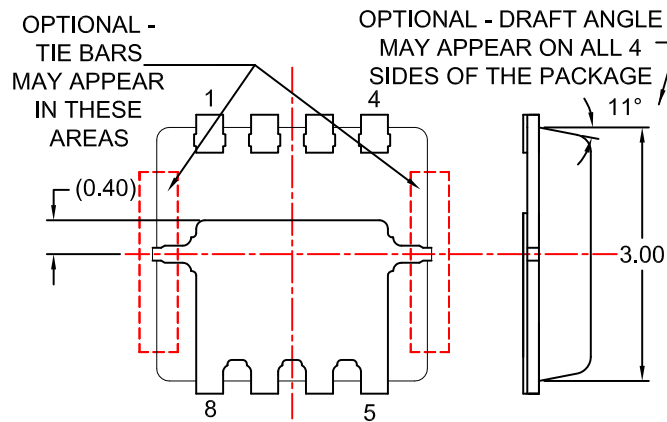
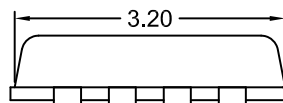
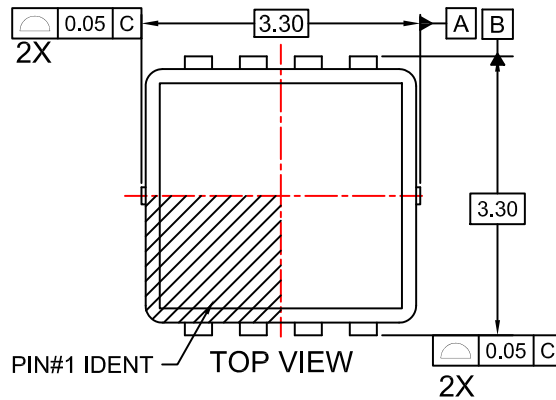
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**WDFN8 3.3x3.3, 0.65P**  
CASE 511DQ  
ISSUE O

DATE 31 OCT 2016



ALL DIMENSIONS AS PER OPTION A  
UNLESS SPECIFIED  
**BOTTOM VIEW**  
(OPTION C)

**NOTES:**

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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