

MOSFET – P-Channel, POWERTRENCH[®]

-20 V, -56 A, 4 mΩ

FDMC6686P

General Description

This P-Channel MOSFET is produced using **onsemi's** advanced POWERTRENCH process that has been optimized for $R_{DS(ON)}$, switching performance and ruggedness.

Features

- Max $R_{DS(on)}$ = 4 mΩ at $V_{GS} = -4.5$ V, $I_D = -18$ A
- Max $R_{DS(on)}$ = 5.7 mΩ at $V_{GS} = -2.5$ V, $I_D = -16$ A
- Max $R_{DS(on)}$ = 11.5 mΩ at $V_{GS} = -1.8$ V, $I_D = -11$ A
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

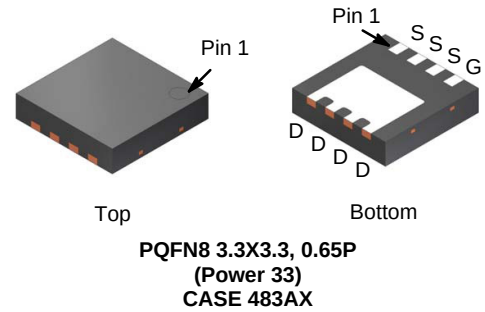
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current – Continuous $T_C = 25^\circ\text{C}$ – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed (Note 3)	-56 -18 -377	A
P_D	Power Dissipation $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	40 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

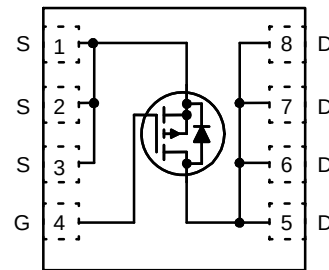
THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

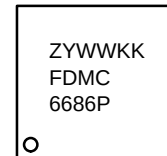
V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
-20 V	4 mΩ @ -4.5 V	-56 A
	5.7 mΩ @ -2.5 V	
	11.5 mΩ @ -1.8 V	



PIN ASSIGNMENT



MARKING DIAGRAM



Z = Assembly Plant Code
 YWW = Date Code (Year & Week)
 KK = Lot Traceability Code
 FDMC6686P = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMC6686P	PQFN8 (Power 33) (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDMC6686P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-15	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.75	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	3	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -4.5 V, I _D = -18 A	-	3.3	4	mΩ
		V _{GS} = -2.5 V, I _D = -16 A	-	4.1	5.7	
		V _{GS} = -1.8 V, I _D = -11 A	-	6	11.5	
		V _{GS} = -4.5 V, I _D = -18 A, T _J = 125°C	-	4.3	6.5	
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -18 A	-	116	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	8800	13200	pF
C _{oss}	Output Capacitance		-	1520	2280	pF
C _{rss}	Reverse Transfer Capacitance		-	1340	2010	pF
R _g	Gate Resistance		-	6.2	-	Ω

SWITCHING CHARACTERISTICS

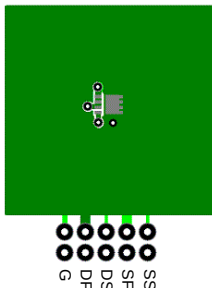
t _{d(on)}	Turn-On Delay Time	V _{DD} = -10 V, I _D = -18 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω	-	25	40	ns
t _r	Rise Time		-	77	122	ns
t _{d(off)}	Turn-Off Delay Time		-	317	506	ns
t _f	Fall Time		-	178	285	ns
Q _g	Total Gate Charge	V _{DD} = -10 V, I _D = -18 A, V _{GS} = -4.5 V	-	87	122	nC
Q _{gs}	Gate to Source Charge		-	14	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	24	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

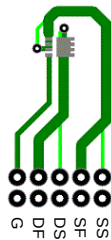
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -18 A (Note 2)	-	-0.7	-1.2	V
		V _{GS} = 0 V, I _S = -2 A (Note 2)	-	-0.6	-1.2	
t _{rr}	Reverse Recovery Time	I _F = -18 A, di/dt = 100 A/μs	-	38	61	ns
Q _{rr}	Reverse Recovery Charge		-	24	39	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Pulse Id refers to Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

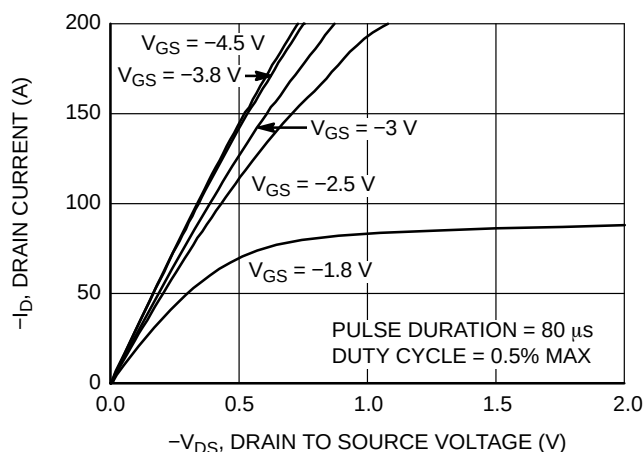


Figure 1. On-Region Characteristics

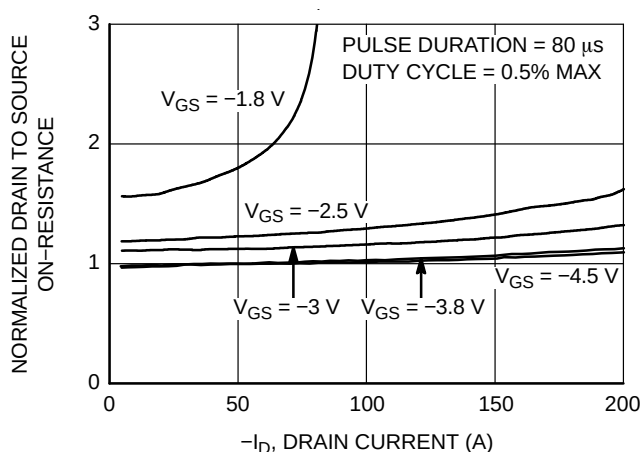


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

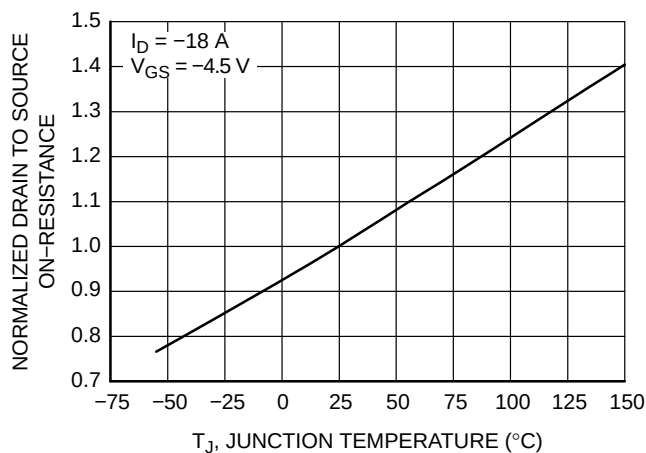


Figure 3. Normalized On-Resistance vs. Junction Temperature

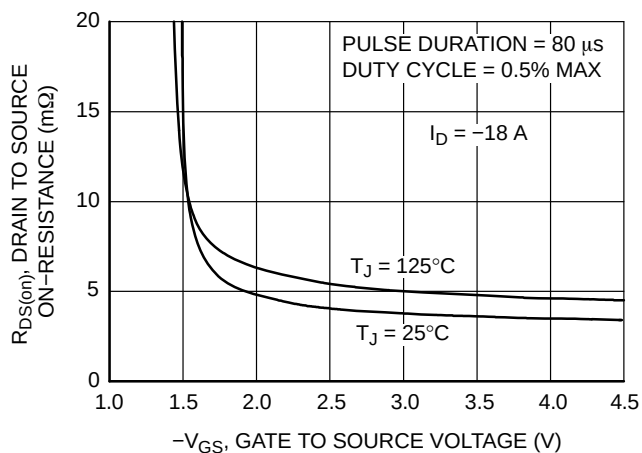


Figure 4. On-Resistance vs. Gate to Source Voltage

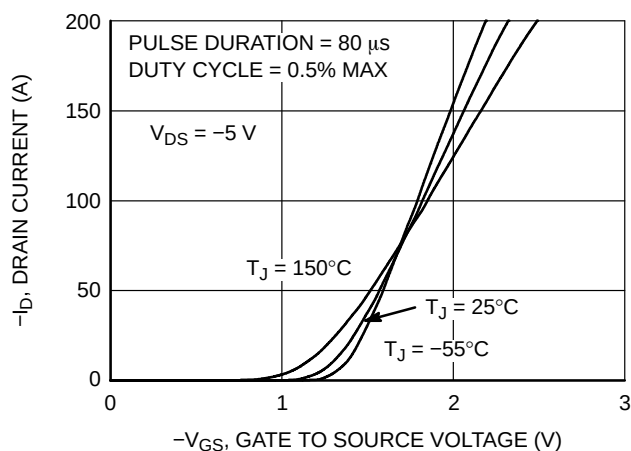


Figure 5. Transfer Characteristics

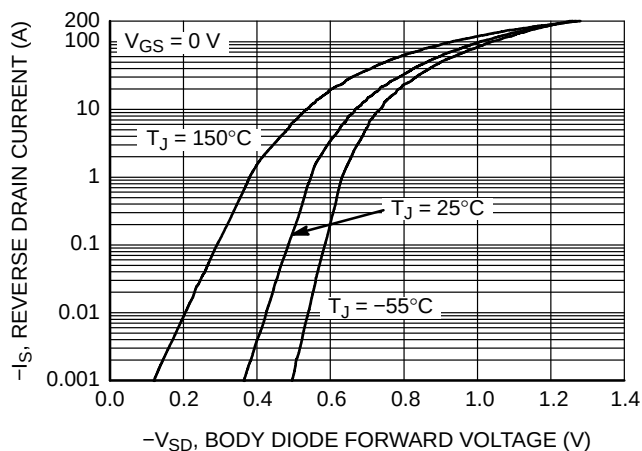


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

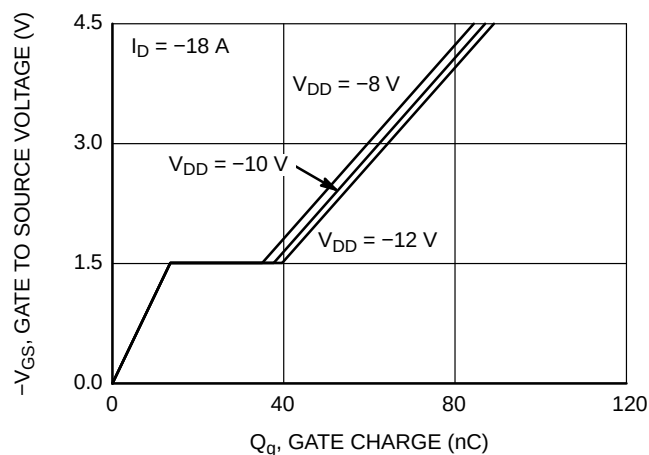


Figure 7. Gate Charge Characteristics

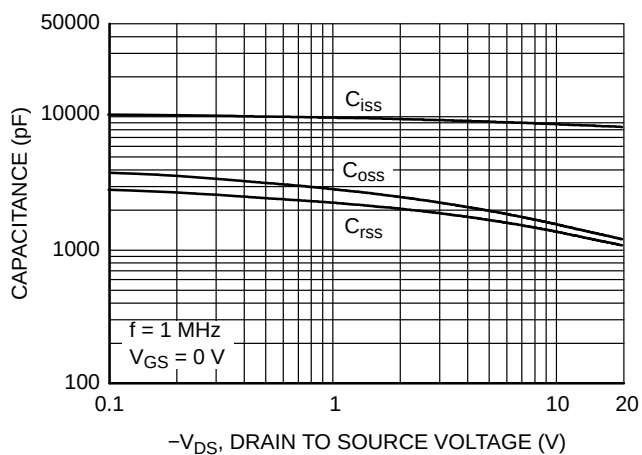


Figure 8. Capacitance vs. Drain to Source Voltage

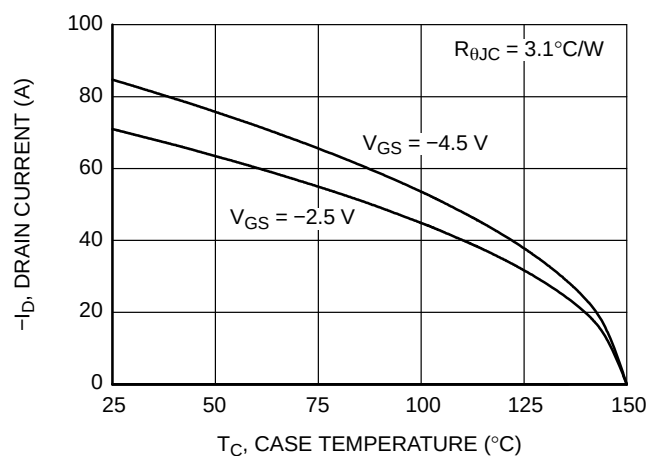


Figure 9. Maximum Continuous Drain Current vs. Case Temperature

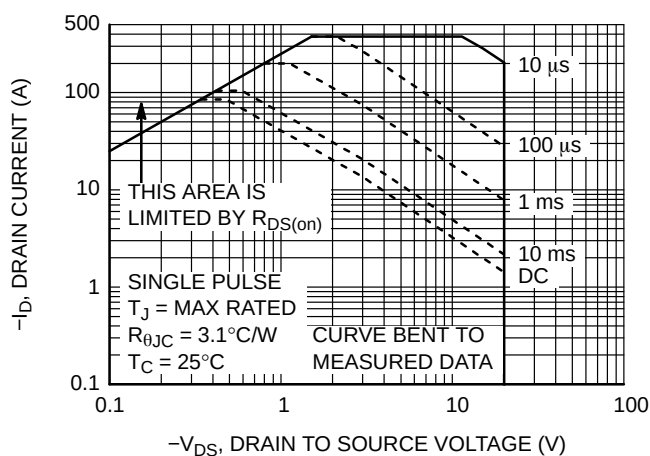


Figure 10. Forward Bias Safe Operating Area

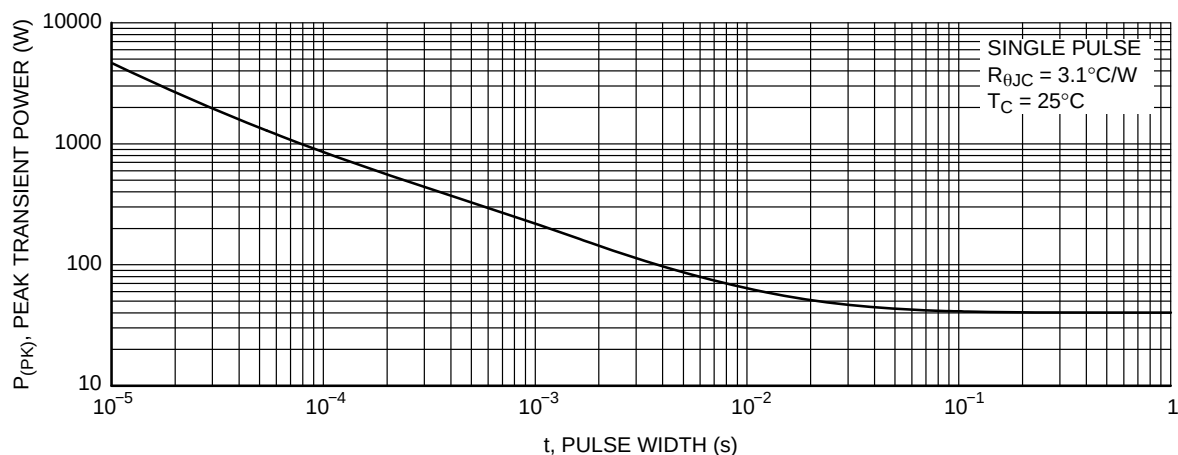
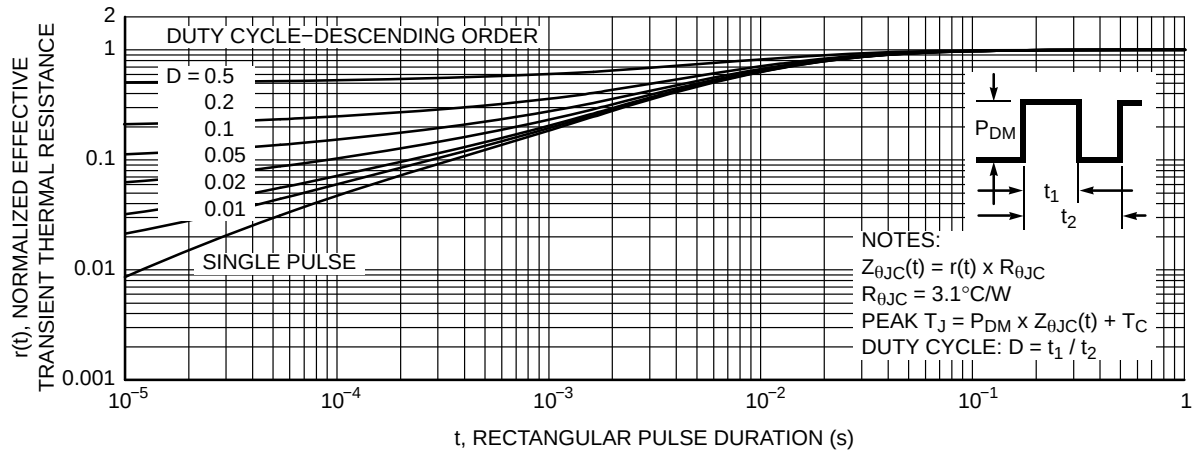


Figure 11. Single Pulse Maximum Power Dissipation

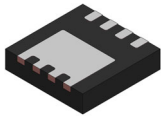
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)



MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

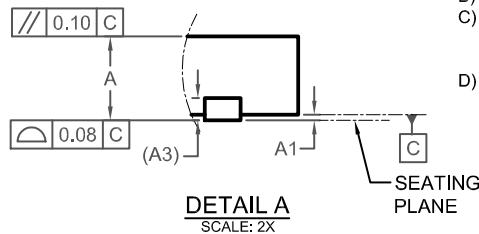
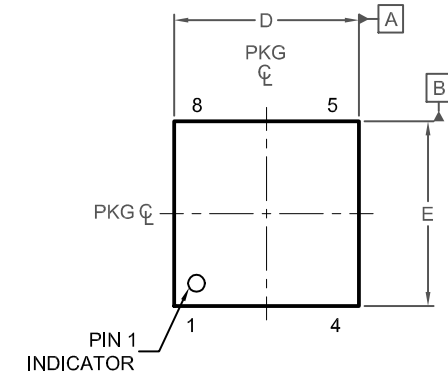


PQFN8 3.3X3.3, 0.65P

CASE 483AX

ISSUE B

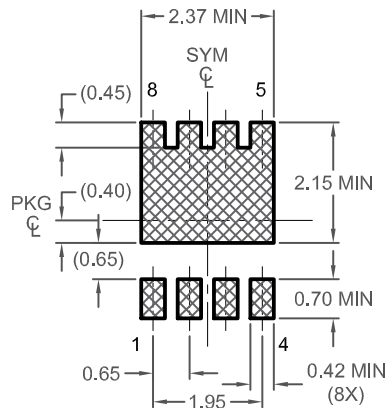
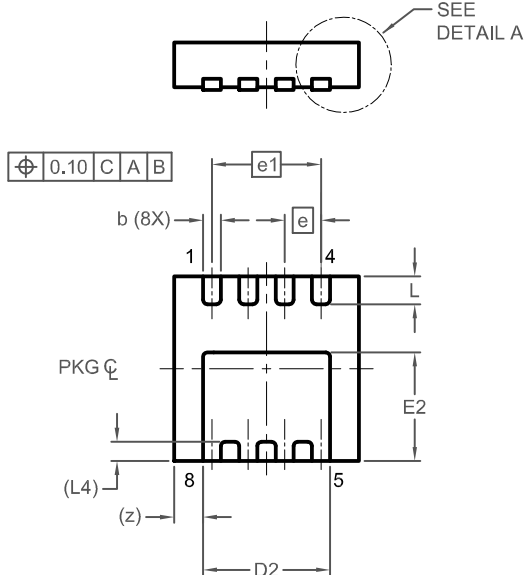
DATE 24 JUN 2022



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
E	3.20	3.30	3.40
E2	1.84	1.94	2.04
e	0.65 BSC		
e1	1.95 BSC		
L	0.40	0.50	0.60
L4	0.34 REF		
z	0.52 REF		



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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