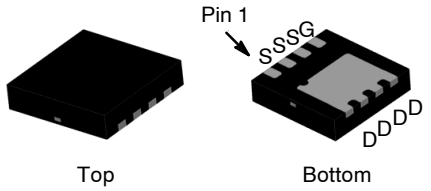
# MOSFET – N-Channel, POWERTRENCH®

## 20 V, 16.5 A, 5 mΩ

# FDMC8554

| $V_{DS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 20 V | 5 mΩ @ 10 V | 16.5 A |
| | 6.4 mΩ @ 4.5 V | |




**WDFN8 3.3x3.3, 0.65P**
**CASE 511DH**

### General Description

This N−Channel MOSFET is a rugged gate version of **onsemi**'s advanced Power Trench process. It has been optimized for power management applications.

### Features

- Max $R_{DS(on)}$ = 5 mΩ at $V_{GS}$ = 10 V, $I_D$ = 16.5 A
- Max $R_{DS(on)}$ = 6.4 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 14 A
- Low Profile – 1 mm Max in Power 33
- This Device is Pb−Free, Halide Free and is RoHS Compliant

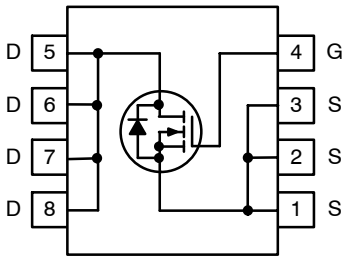
### Applications

- DC−DC Conversion

### MARKING DIAGRAM


FDMC8554 = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

### PIN ASSIGNMENT




**N−Channel MOSFET**

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted.)

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 20 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current<br>– Continuous<br>– Continuous (Note 1a)<br>– Pulsed | <br>$T_C$ = 25°C<br>$T_A$ = 25°C<br> | <br>16.5<br>16.5<br>36 | A |
| $P_D$ | Power Dissipation | $T_C$ = 25°C | 41 | W |
| | Power Dissipation (Note 1a) | $T_A$ = 25°C | 2.0 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted.)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 60 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDMC8554 | WDFN8 (Pb−Free, Halide Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

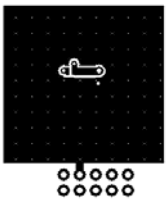
**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 20 | – | – | V |
| $\Delta BV_{DSS}$ /$\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 15.7 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| | | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V, $T_J$ = 125°C | – | – | 100 | |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.8 | 3.0 | V |
| $\Delta V_{GS(th)}$ /$\Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | −6.1 | – | mV/°C |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 16.5 A | – | 3.6 | 5.0 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 14 A | – | 4.6 | 6.4 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 16.5 A, $T_J$ = 125°C | – | 5.4 | 7.1 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 16.5 A | – | 62 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 2540 | 3380 | pF |
| $C_{oss}$ | Output Capacitance | | – | 795 | 1060 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 510 | 765 | pF |
| $R_g$ | Gate Resistance | f = 1 MHz | – | 1.2 | – | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 16.5 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 13 | 24 | ns |
| $t_r$ | Rise Time | | – | 10 | 20 | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 32 | 51 | ns |
| $t_f$ | Fall Time | | – | 7 | 14 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at 10V | $V_{DD}$ = 10 V, $I_D$ = 16.5 A | – | 44 | 62 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge at 4.5V | | – | 24 | 34 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | – | 8.5 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | – | 10 | – | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 16.5 A (Note 2) | – | 0.8 | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 16.5 A, di/dt = 100 A/μs | – | 31 | 47 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 22 | 33 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 60°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.

b) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

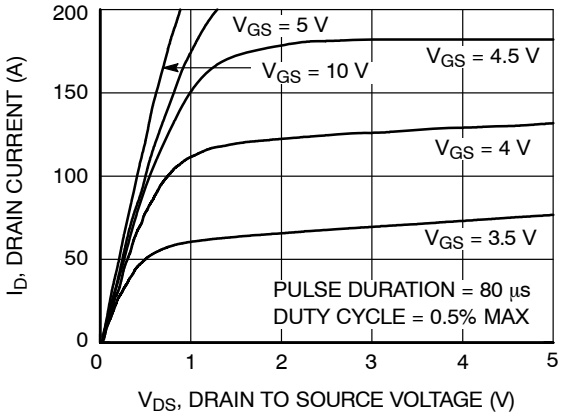



**Figure 1. On Region Characteristics**

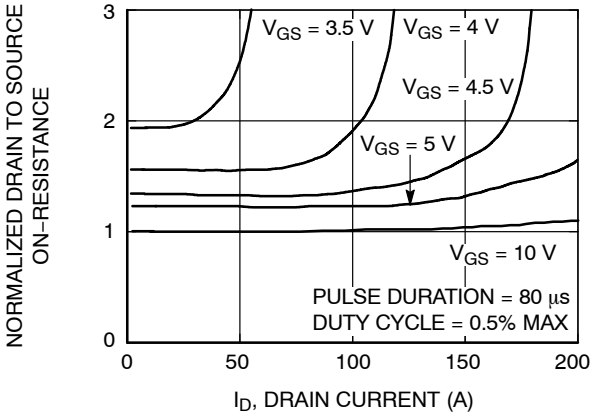



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

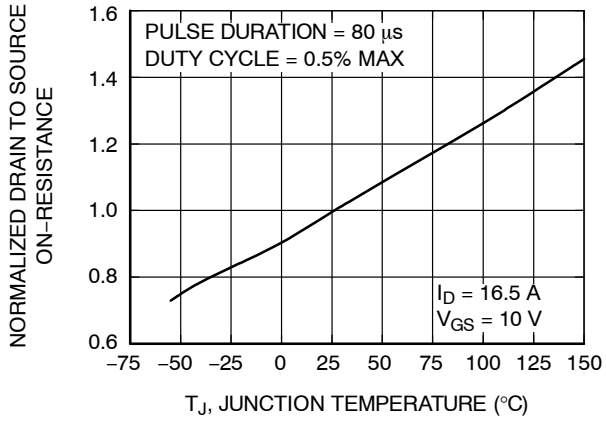



**Figure 3. Normalized On Resistance vs. Junction Temperature**

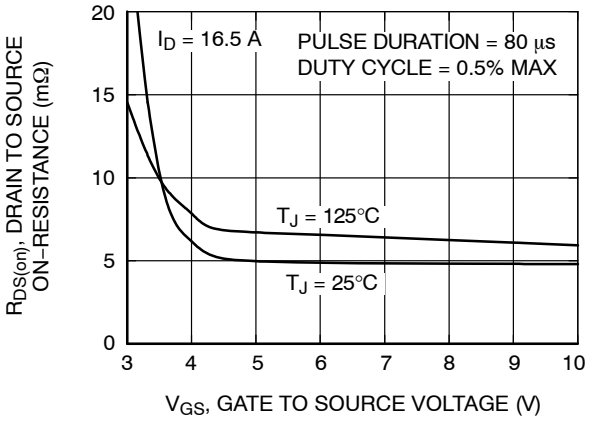



**Figure 4. On−Resistance vs. Gate to Source Voltage**

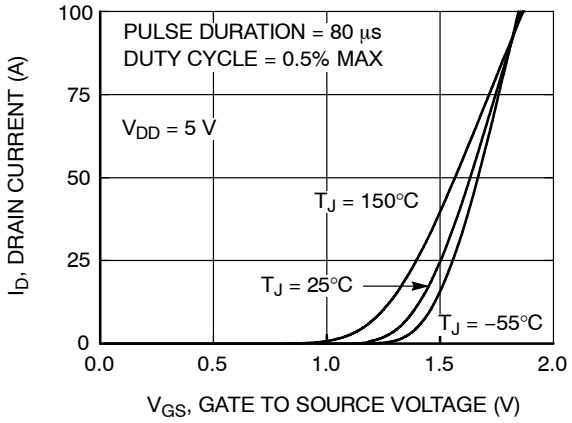



**Figure 5. Transfer Characteristics**

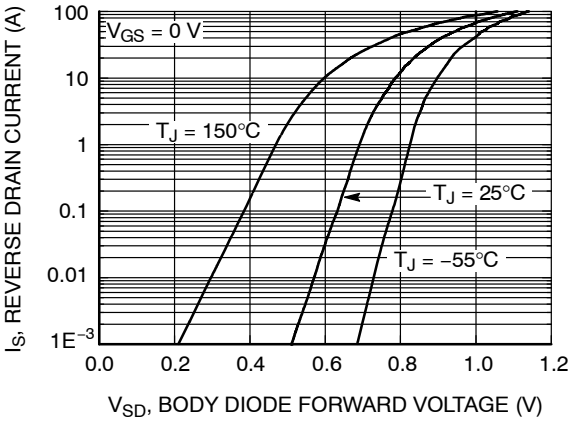



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

**TYPICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued)

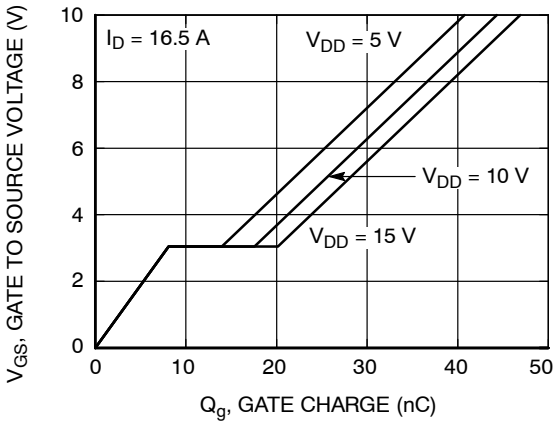



**Figure 7. Gate Charge Characteristics**

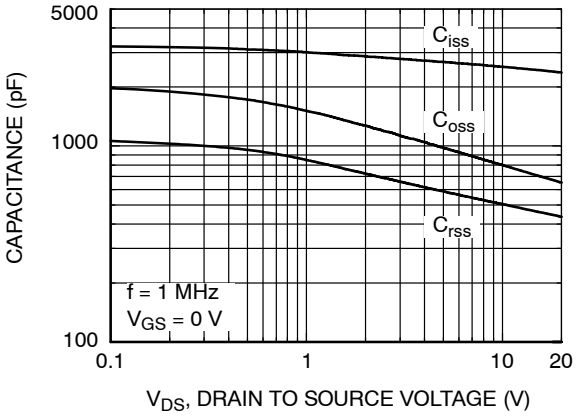



**Figure 8. Capacitance vs. Drain to SourceVoltage**

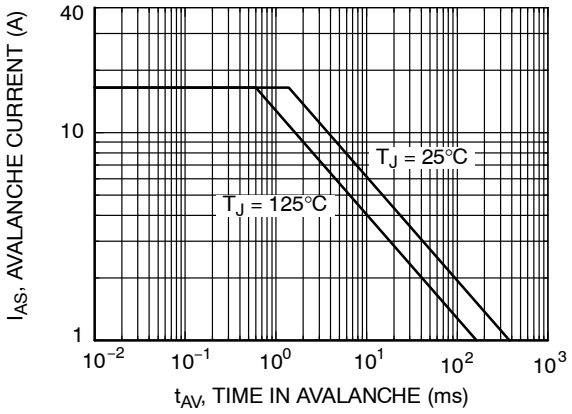



**Figure 9. Unclamped Inductive Switching Capability**

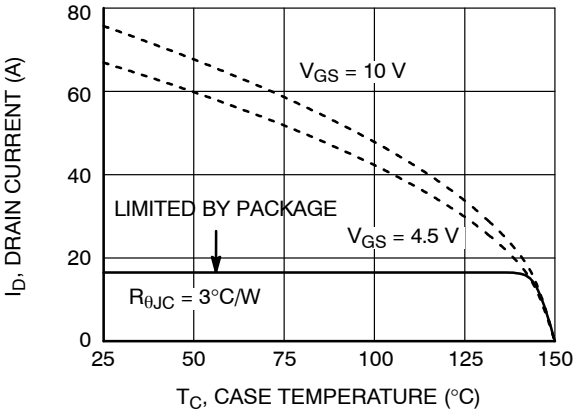



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

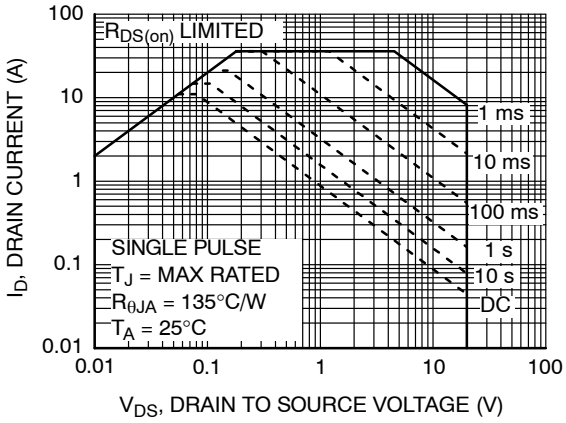



**Figure 11. Forward Bias Safe Operating Area**

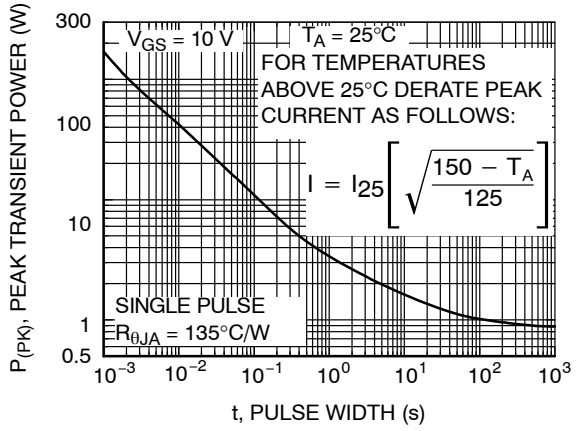



**Figure 12. Single Pulse Maximum Power Dissipation**

**TYPICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued)

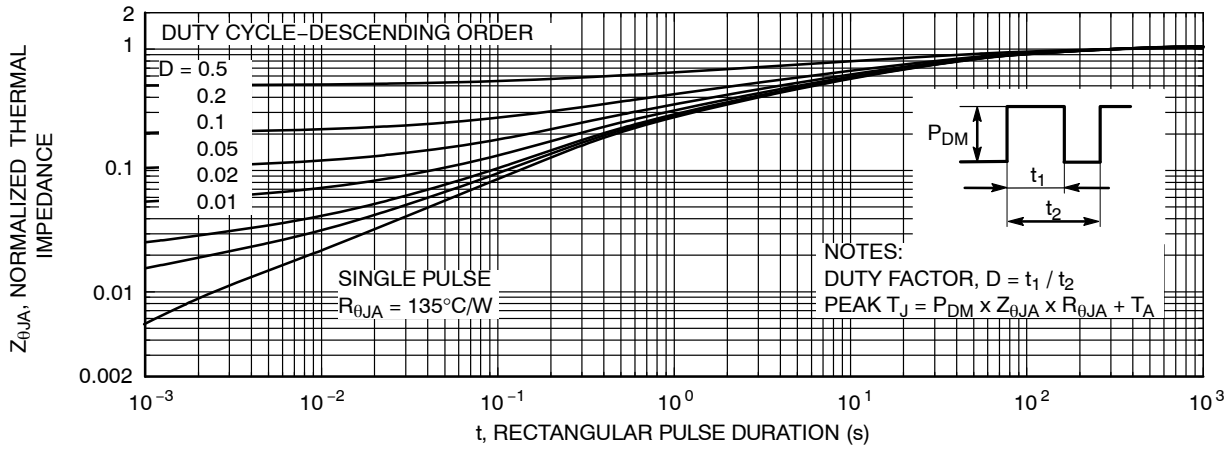
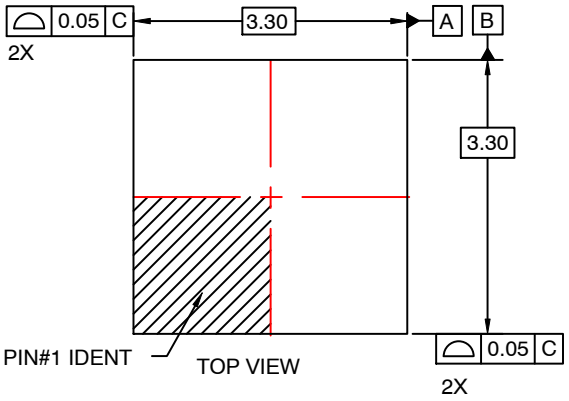
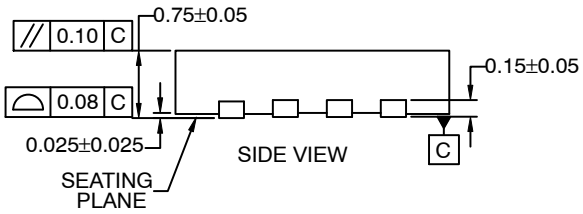


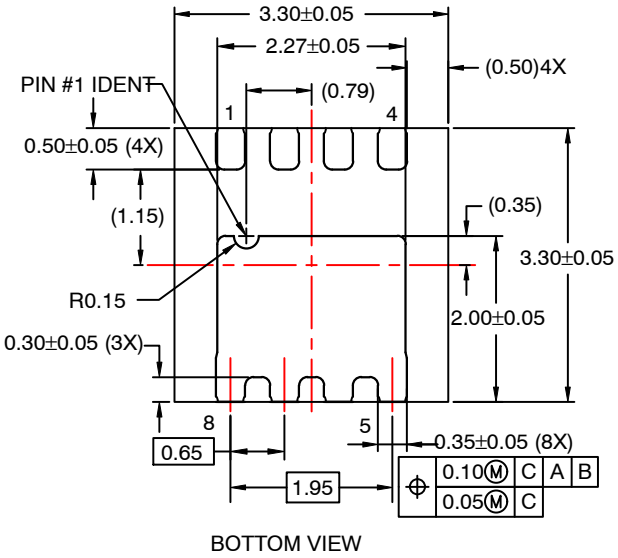

**Figure 13. Transient Thermal Response Curve**

**WDFN8 3.3x3.3, 0.65P**
CASE 511DH
ISSUE O

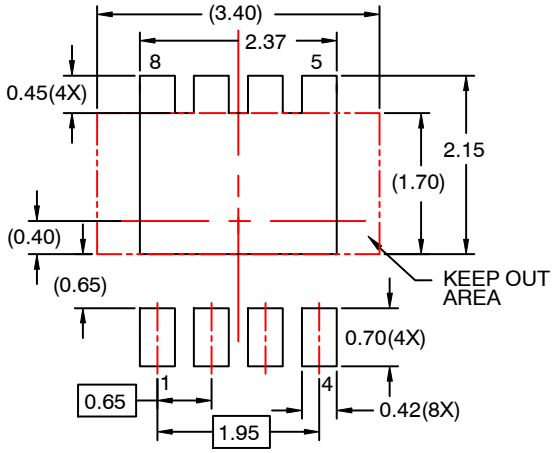
DATE 31 JUL 2016




BOTTOM VIEW




RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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