June 2014

# FDMC86320

## N-Channel Power Trench® MOSFET

### 80 V, 22 A, 11.7 mΩ

### Features

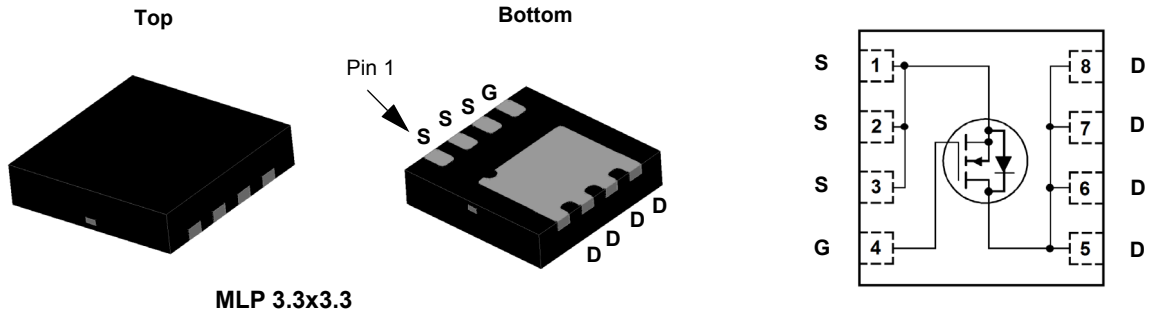
- Max $r_{DS(on)}$ = 11.7 mΩ at $V_{GS}$ = 10 V, $I_D$ = 10.7 A
- Max $r_{DS(on)}$ = 16 mΩ at $V_{GS}$ = 8 V, $I_D$ = 8.5 A
- MSL1 robust package design
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers.It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

### Applications

- Primary DC-DC Switch
- Motor Bridge Switch
- Synchronous Rectifier




MLP 3.3x3.3

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 80 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | | 22 | A |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | 10.7 | |
| | -Pulsed | | | 50 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 60 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 40 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.3 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 3.1 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | |

### Package Marking and Ordering Information

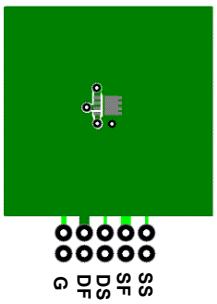
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMC86320 | FDMC86320 | Power 33 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

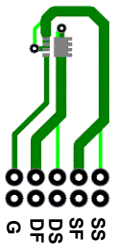
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 80 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 56 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.4 | 3.5 | 4.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -11 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 10.7 A | | 9.7 | 11.7 | mΩ |
| | | $V_{GS}$ = 8 V, $I_D$ = 8.5 A | | 11.4 | 16 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 10.7 A, $T_J$ = 125 °C | | 15 | 18 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 10.7 A | | 20 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, f = 1 MHz | | 1985 | 2640 | pF |
| $C_{oss}$ | Output Capacitance | | | 353 | 469 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 12 | 30 | pF |
| $R_g$ | Gate Resistance | | | 0.5 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 40 V, $I_D$ = 10.7 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 15 | 28 | ns |
| $t_r$ | Rise Time | | | 8 | 16 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 20 | 35 | ns |
| $t_f$ | Fall Time | | | 5 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 40 V, $I_D$ = 10.7 A | | 29 | 41 | nC |
| $Q_{g(TOT)}$ | | $V_{GS}$ = 0 V to 8 V; $V_{DD}$ = 40 V, $I_D$ = 10.7 A | | 24 | 34 | nC |
| $Q_{gs}$ | Total Gate Charge | $V_{DD}$ = 40 V, $I_D$ = 10.7 A | | 10 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 6.9 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 10.7 A (Note 2) | | 0.84 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 2 A (Note 2) | | 0.75 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 10.7 A, di/dt = 100 A/μs | | 38 | 61 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 27 | 43 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a. 53 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper




b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25 °C; N-ch: L = 0.3 mH, $I_{AS}$ = 20 A, $V_{DD}$ = 72 V, $V_{GS}$ = 10 V.

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

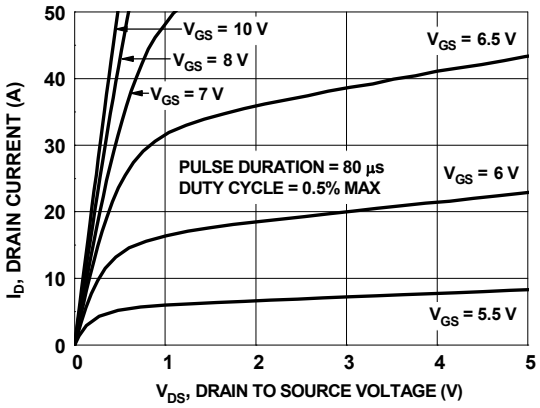



**Figure 1. On Region Characteristics**

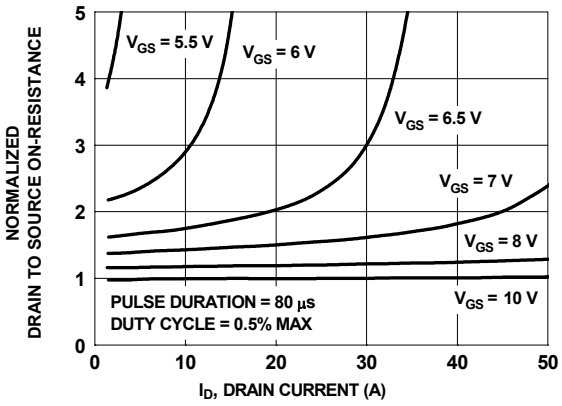



**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**

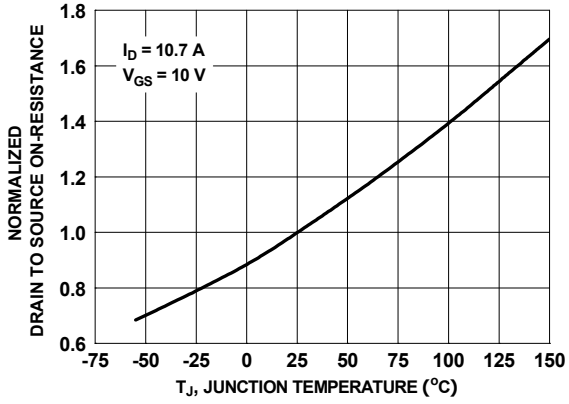



**Figure 3. Normalized On Resistance vs. Junction Temperature**

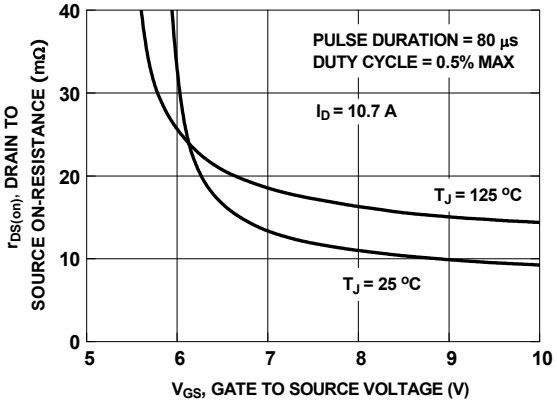



**Figure 4. On-Resistance vs. Gate to Source Voltage**

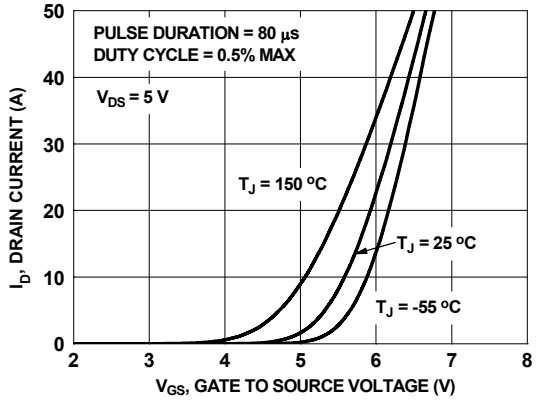



**Figure 5. Transfer Characteristics**

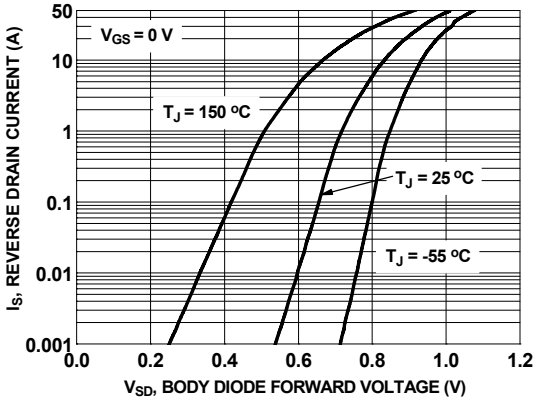



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

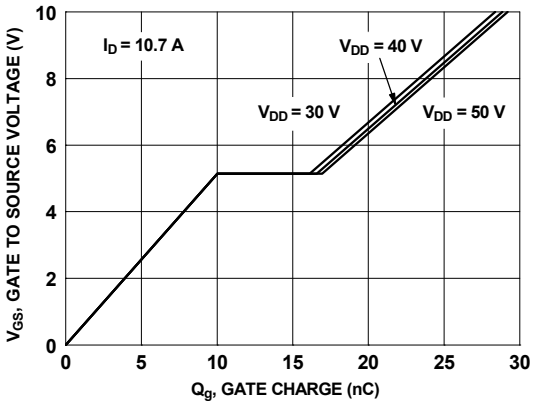



**Figure 7. Gate Charge Characteristics**

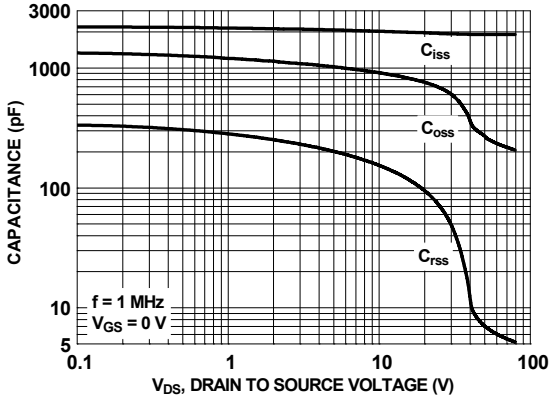



**Figure 8. Capacitance vs. Drain to Source Voltage**

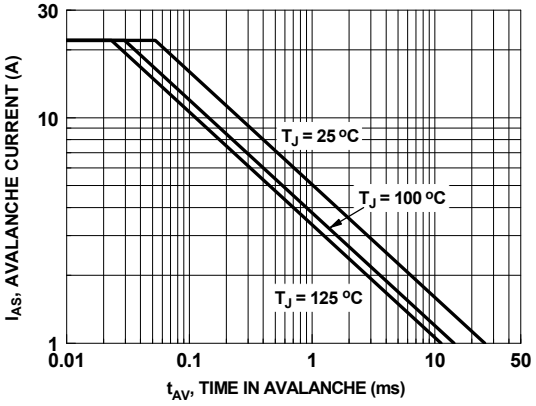



**Figure 9. Unclamped Inductive Switching Capability**

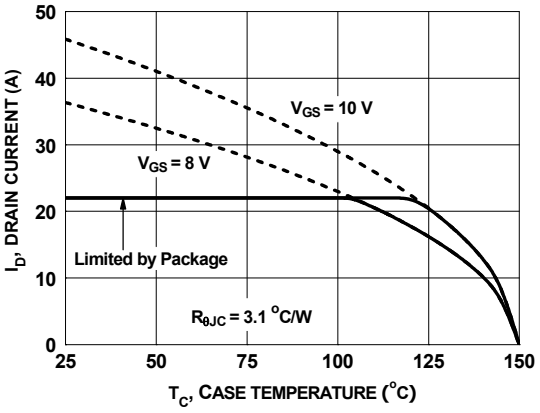



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

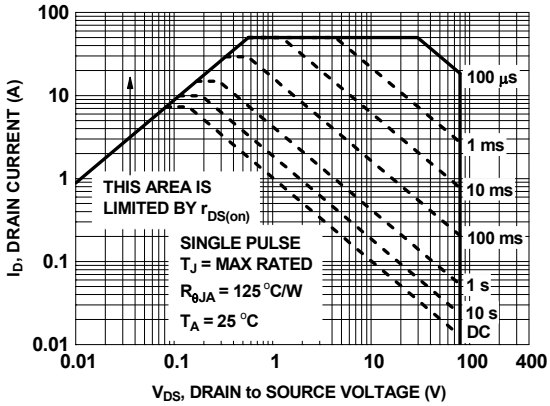



**Figure 11. Forward Bias Safe Operating Area**

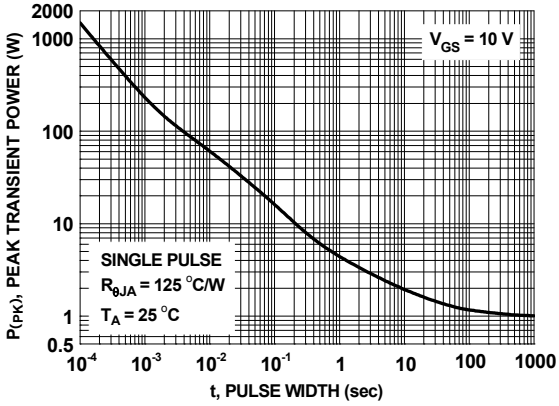



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

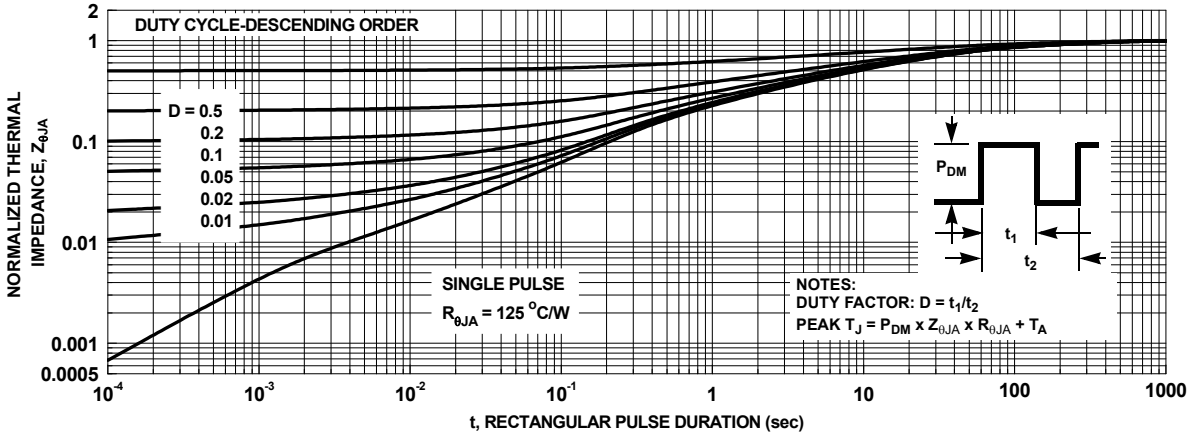
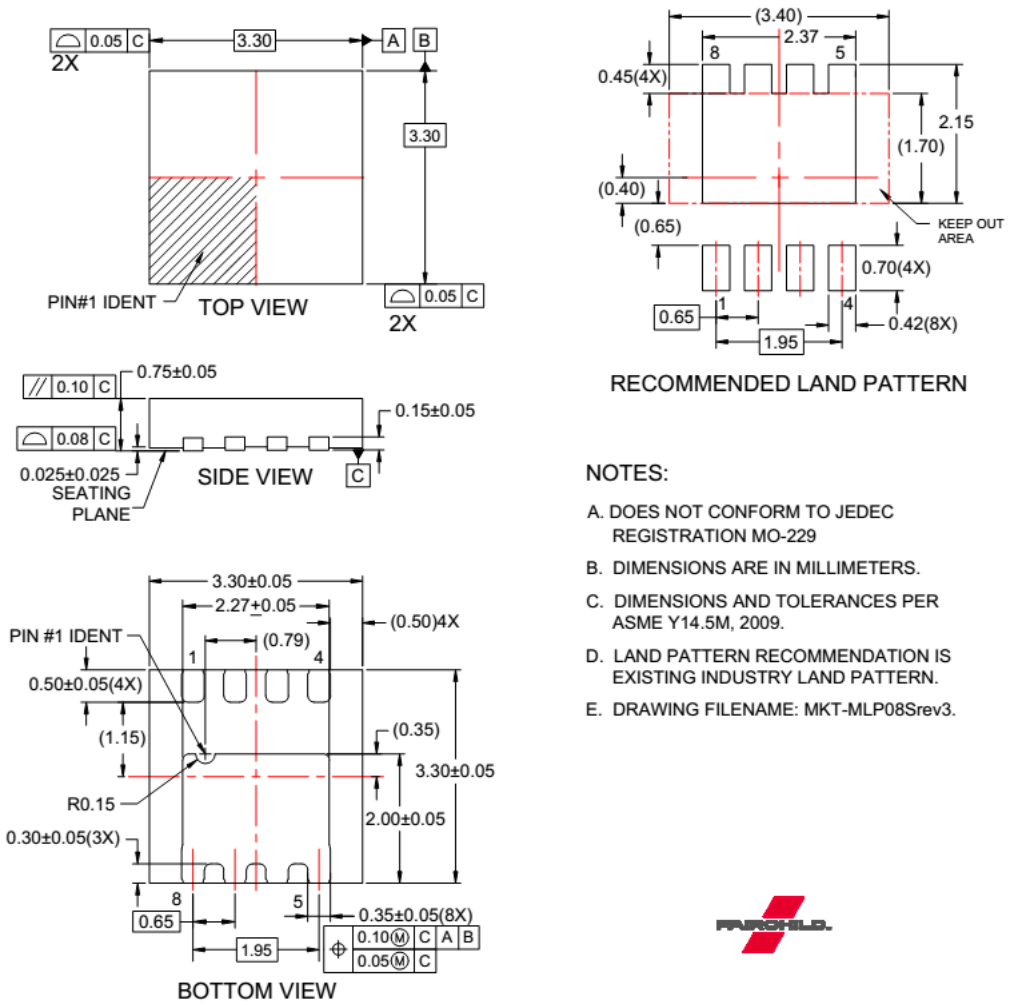



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout

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