

FDMQ8403

GreenBridge™ Series of High-Efficiency Bridge Rectifiers N-Channel PowerTrench® MOSFET 100 V, 6 A, 110 mΩ

Features

- Max $r_{DS(on)}$ = 110 mΩ at $V_{GS} = 10$ V, $I_D = 3$ A
- Max $r_{DS(on)}$ = 175 mΩ at $V_{GS} = 6$ V, $I_D = 2.4$ A
- Substantial efficiency benefit in PD solutions
- RoHS Compliant

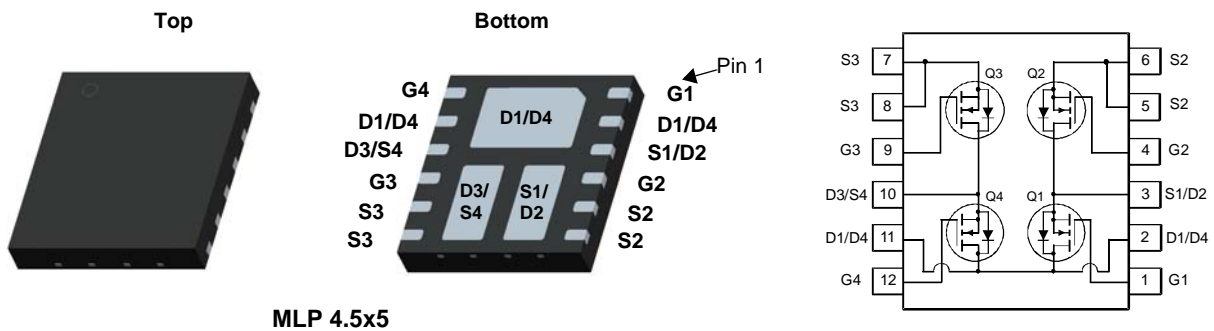


General Description

This quad MOSFET solution provides ten-fold improvement in power dissipation over diode bridge.

Application

- High-Efficiency Bridge Rectifiers



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25$ °C	6	A
	-Continuous (Silicon limited) $T_C = 25$ °C	9	
	-Continuous $T_A = 25$ °C (Note 1a)	3.1	
	-Pulsed	12	
P_D	Power Dissipation $T_C = 25$ °C	17	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	1.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	135	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMQ8403	FDMQ8403	MLP 4.5x5	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		72		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	2	2.8	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$		85	110	m Ω
		$V_{GS} = 6\text{ V}$, $I_D = 2.4\text{ A}$		115	175	
		$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		147	191	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 3\text{ A}$		6		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		162	215	pF
C_{oss}	Output Capacitance			43	60	pF
C_{rss}	Reverse Transfer Capacitance			2.6	5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 3\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		4.1	10	ns	
t_r	Rise Time			1.2	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			7.2	15	ns	
t_f	Fall Time			1.8	10	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		3	5	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } 5\text{ V}$	$V_{DD} = 50\text{ V}$, $I_D = 3\text{ A}$		1.7	3	nC
Q_{gs}	Gate to Source Charge				0.9		nC
Q_{gd}	Gate to Drain "Miller" Charge				0.8		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 3\text{ A}$ (Note 2)		0.86	1.3	V
t_{rr}	Reverse Recovery Time	$I_F = 3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		33	53	ns
Q_{rr}	Reverse Recovery Charge			23	37	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $65\text{ }^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.



b. $135\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

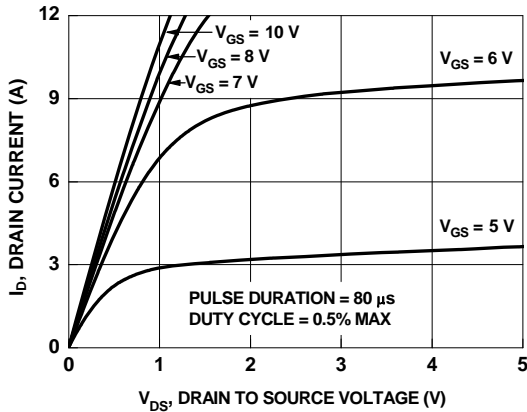


Figure 1. On Region Characteristics

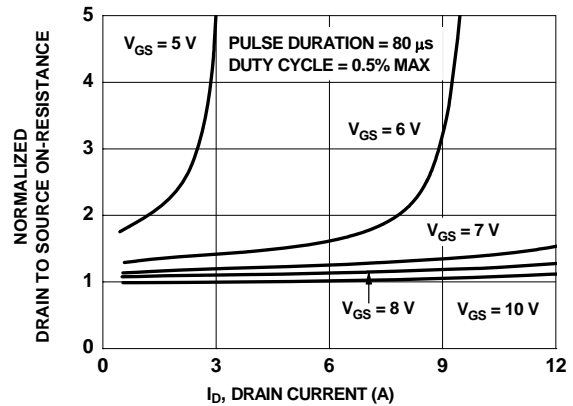


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

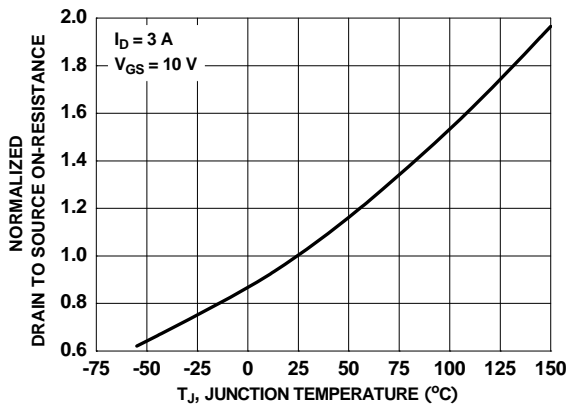


Figure 3. Normalized On Resistance vs Junction Temperature

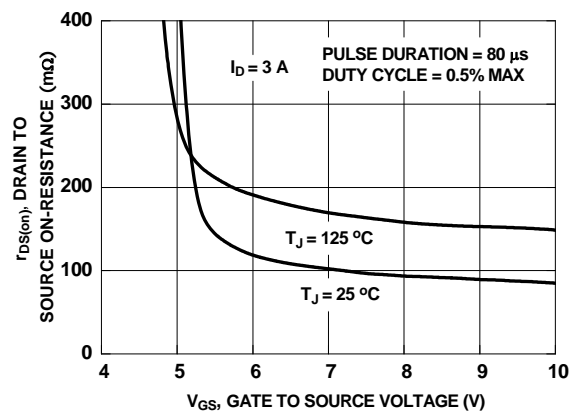


Figure 4. On-Resistance vs Gate to Source Voltage

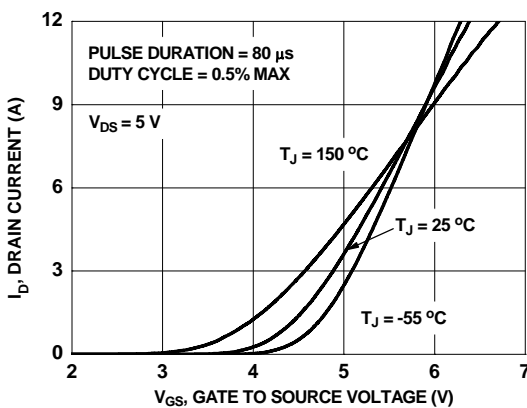


Figure 5. Transfer Characteristics

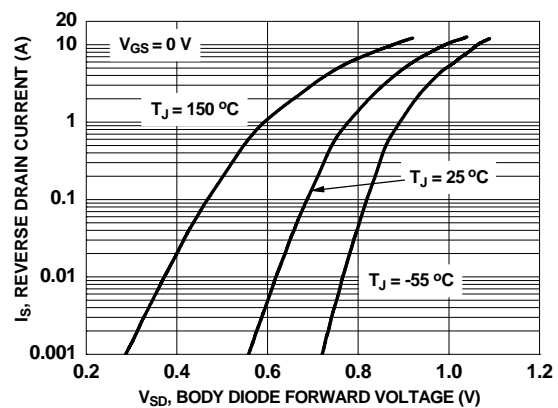


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

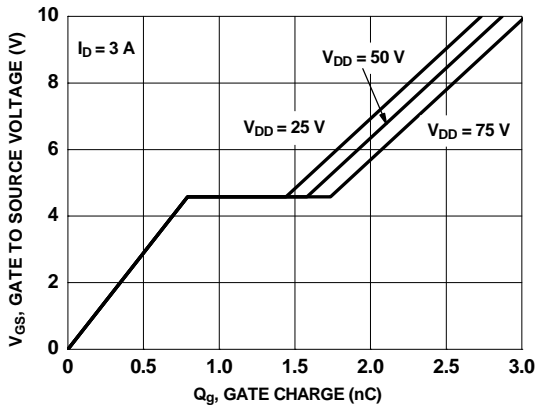


Figure 7. Gate Charge Characteristics

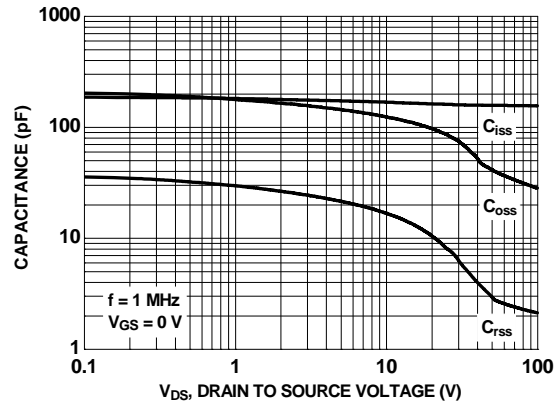


Figure 8. Capacitance vs Drain to Source Voltage

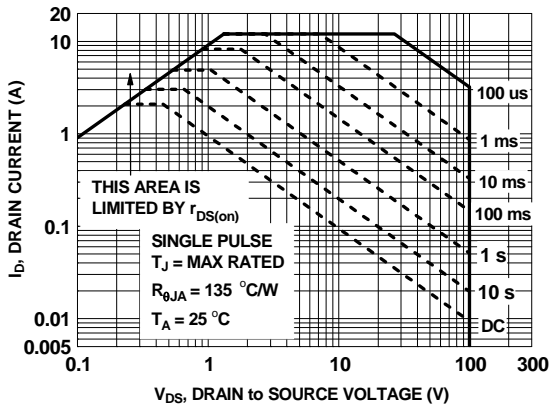


Figure 9. Forward Bias Safe Operating Area

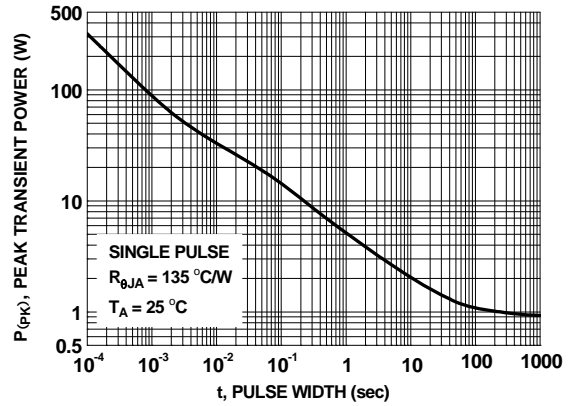


Figure 10. Single Pulse Maximum Power Dissipation

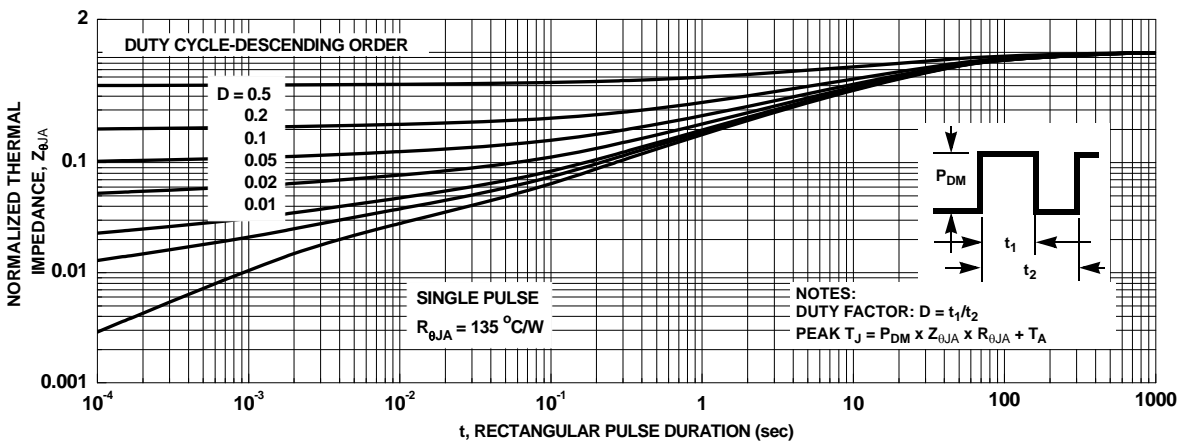
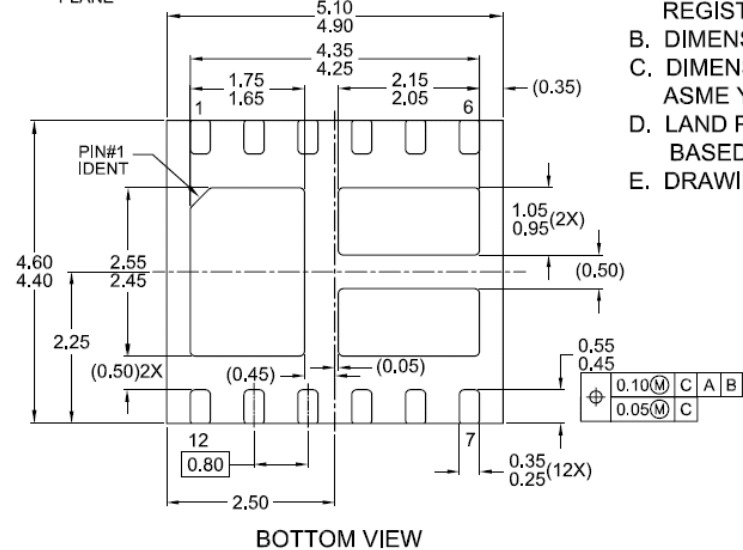
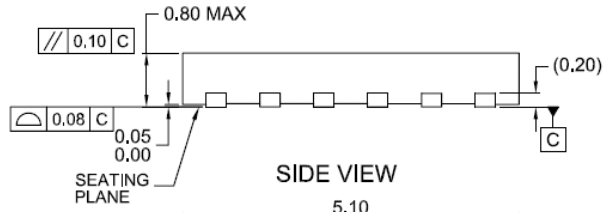
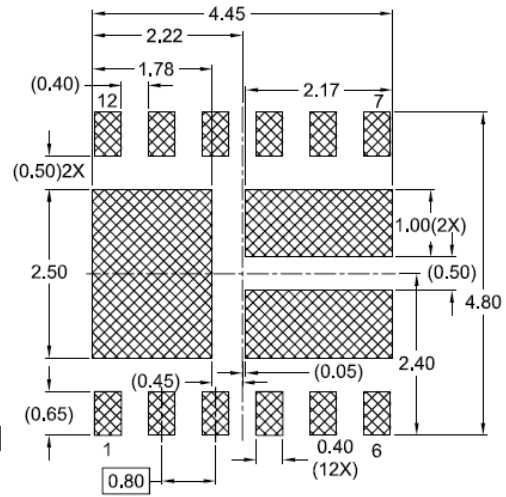
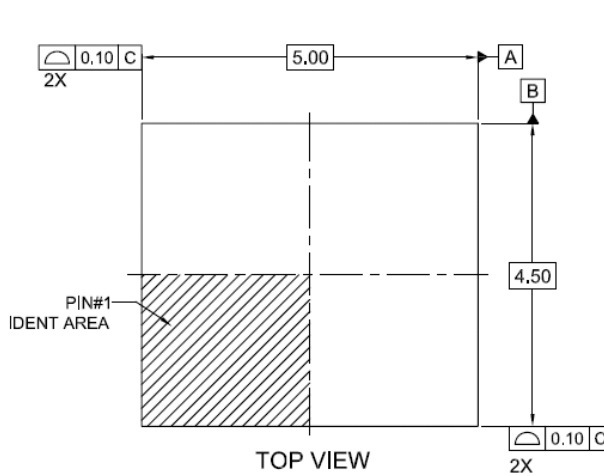


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout






- NOTES:**
- A. THIS MKT. DWG. DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 - D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
 - E. DRAWING FILENAME: MKT-MLP12FRev1.



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