October 2014

FDMS3500

N-Channel Power Trench® MOSFET

75V, 49A, 14.5mΩ

Features

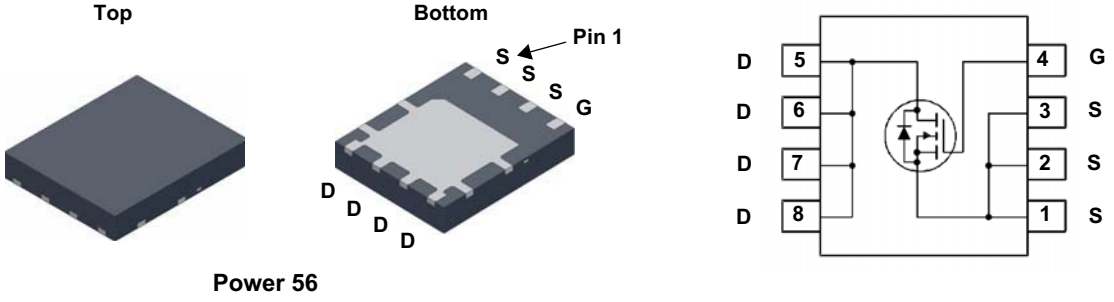
- Max $r_{DS(on)}$ = 14.5mΩ at V_{GS} = 10V, I_D = 11.5A
- Max $r_{DS(on)}$ = 16.3mΩ at V_{GS} = 4.5V, I_D = 10A
- Advanced Package and Silicon combination for low $r_{DS(on)}$
- MSL1 robust package design
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC - DC Conversion



Power 56

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			75	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		49	A
	-Continuous (Silicon limited)	T_C = 25°C		57	
	-Continuous	T_A = 25°C	(Note 1a)	9.2	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	384	mJ
P_D	Power Dissipation	T_C = 25°C		96	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

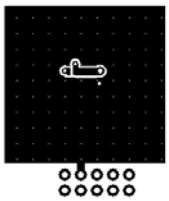
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS3500	FDMS3500	Power 56	13''	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	75			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		71		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 60V,			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-6.8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 11.5A		11.1	14.5	mΩ
		V_{GS} = 4.5V, I_D = 10A		12.8	16.3	
		V_{GS} = 10V, I_D = 11.5A, T_J = 125°C		17.6	23.0	
g_{FS}	Forward Transconductance	V_{DD} = 5V, I_D = 11.5A		56		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		3580	4765	pF
C_{oss}	Output Capacitance			225	300	pF
C_{rss}	Reverse Transfer Capacitance			120	175	pF
R_g	Gate Resistance	f = 1MHz		1.2		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40V, I_D = 11.5A, V_{GS} = 10V, R_{GEN} = 6Ω		16	29	ns
t_r	Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			48	77	ns
t_f	Fall Time			6	11	ns
Q_g	Total Gate Charge	V_{GS} = 0V to 10V; V_{DD} = 40V, I_D = 11.5A		65	91	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 5V; V_{DD} = 40V, I_D = 11.5A		34	48	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40V, I_D = 11.5A		9.9		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 40V, I_D = 11.5A		11.6		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 11.5A (Note 2)		0.8	1.3	V
		V_{GS} = 0V, I_S = 2.1A (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 11.5A, di/dt = 100A/μs		38	60	ns
Q_{rr}	Reverse Recovery Charge			45	72	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting T_J = 25°C, L = 3mH, I_{AS} = 16A, V_{DD} = 75V, V_{GS} = 10V

Typical Characteristics T_J = 25°C unless otherwise noted

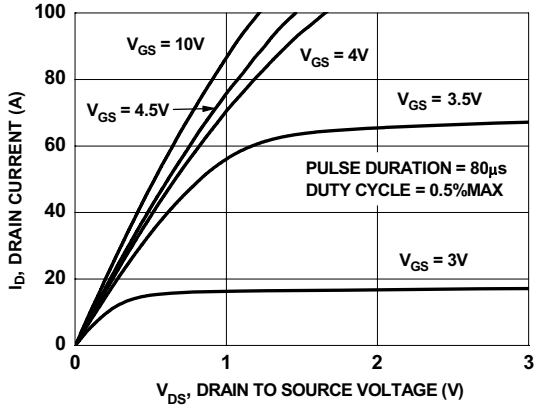


Figure 1. On-Region Characteristics

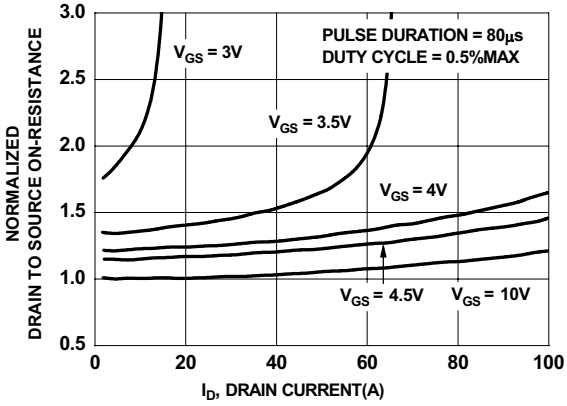


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

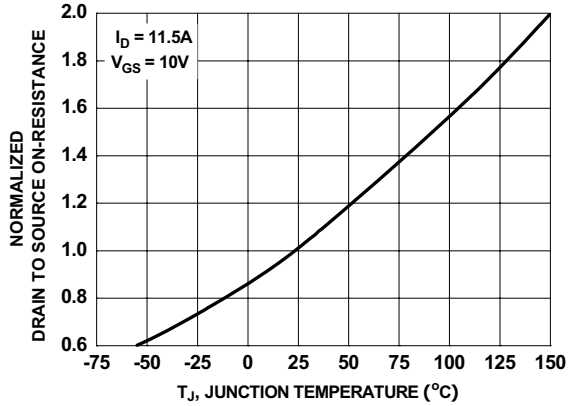


Figure 3. Normalized On-Resistance vs Junction Temperature

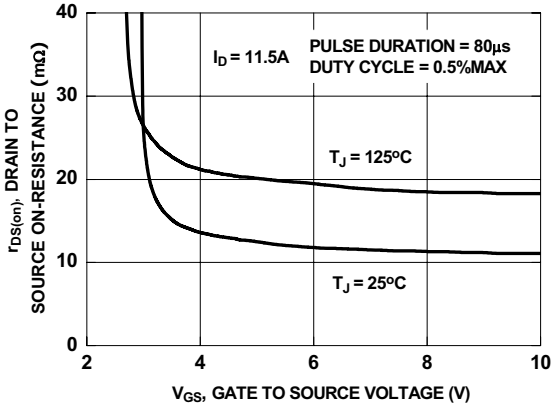


Figure 4. On-Resistance vs Gate to Source Voltage

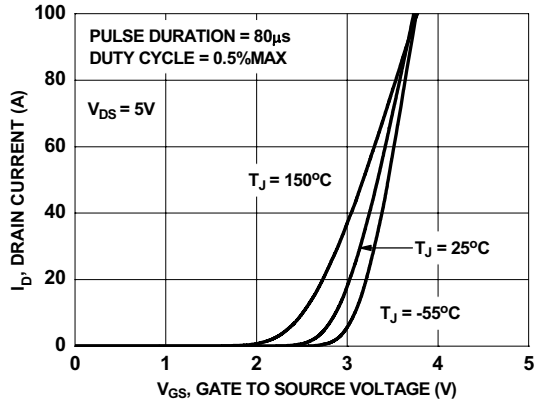


Figure 5. Transfer Characteristics

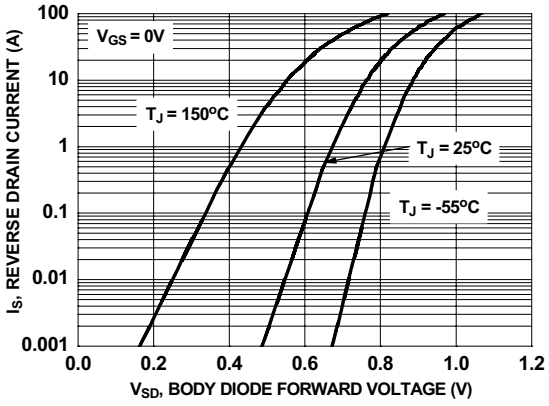


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

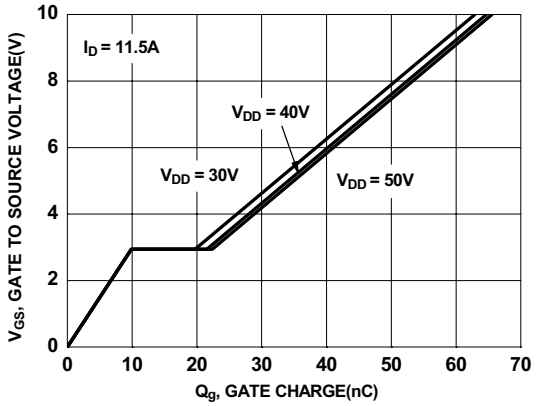


Figure 7. Gate Charge Characteristics

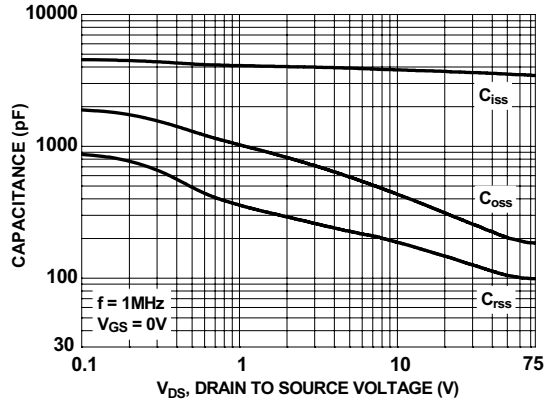


Figure 8. Capacitance vs Drain to Source Voltage

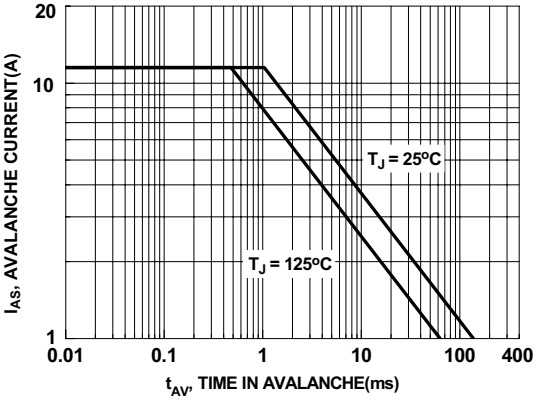


Figure 9. Unclamped Inductive Switching Capability

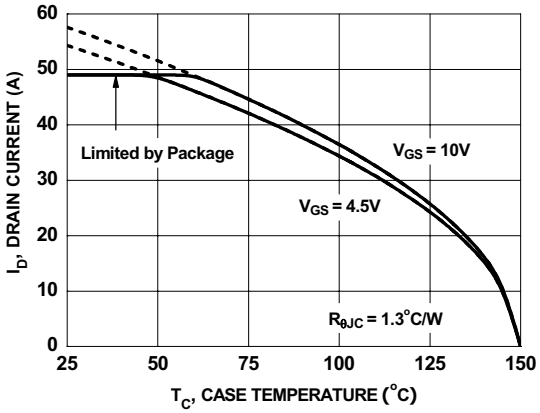


Figure 10. Maximum Continuous Drain Current vs Case Temperature

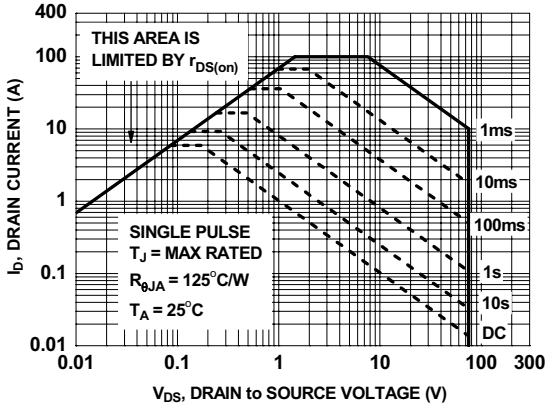


Figure 11. Forward Bias Safe Operating Area

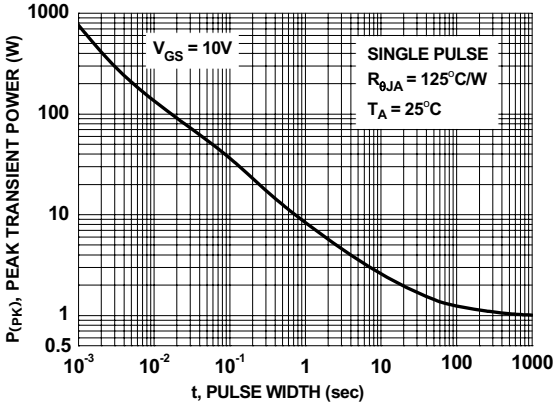


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

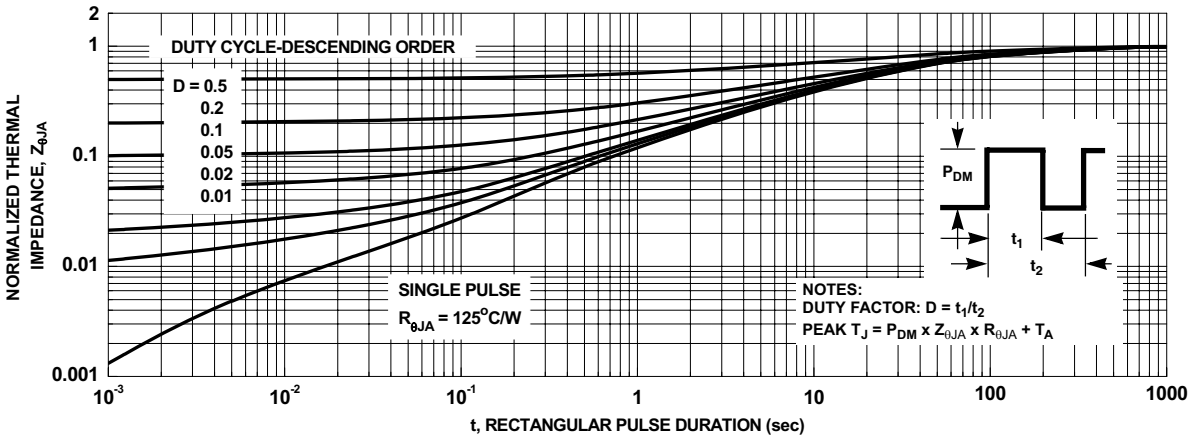
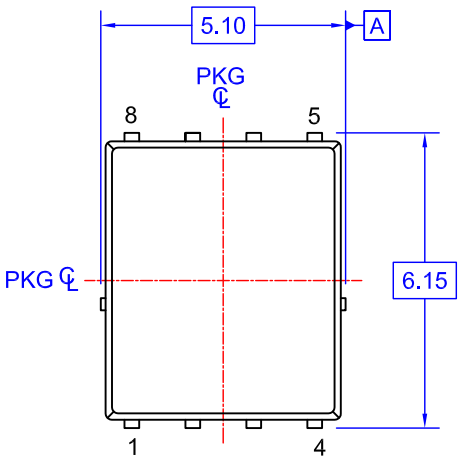
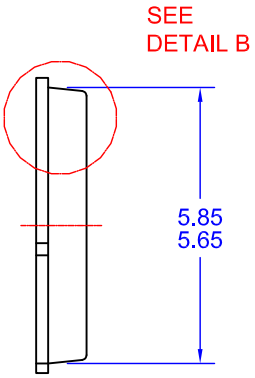
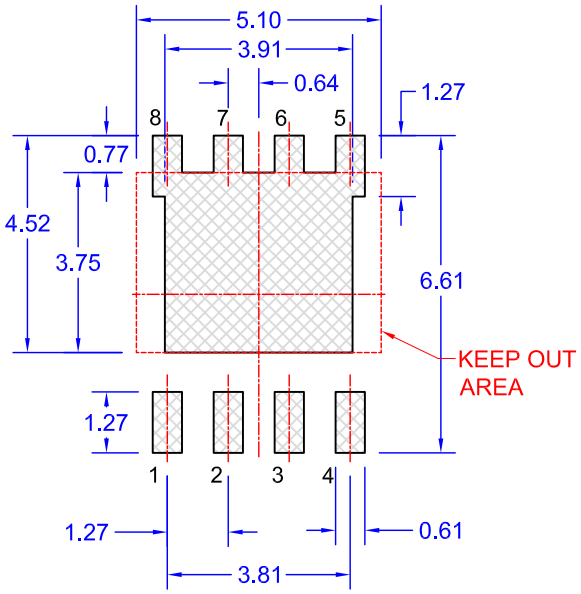


Figure 13. Transient Thermal Response Curve

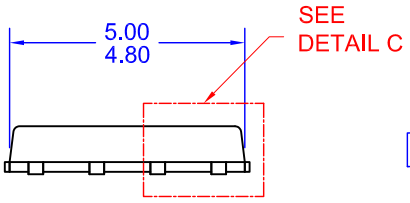


TOP VIEW

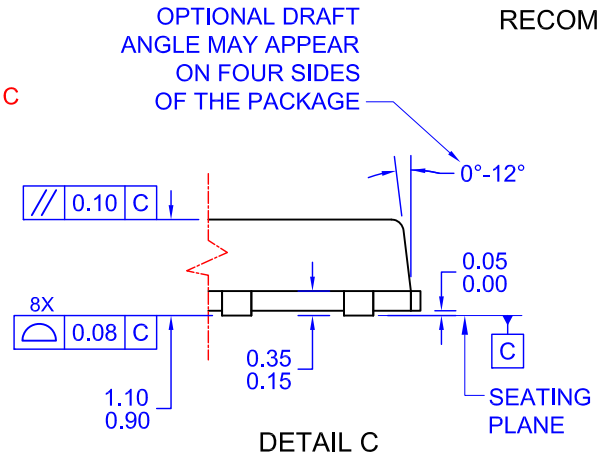




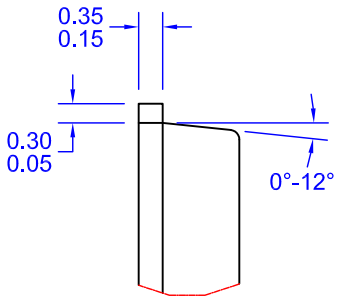
LAND PATTERN
RECOMMENDATION



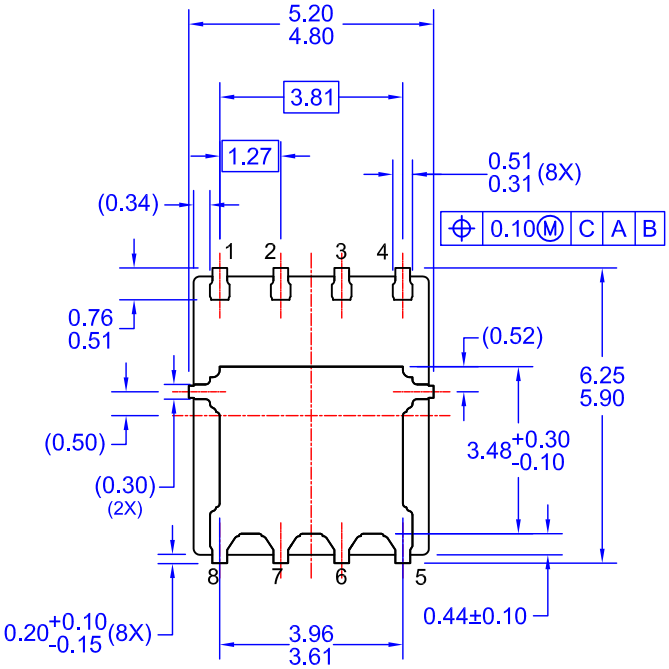
SIDE VIEW



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F. DRAWING FILE NAME: PQFN08AREV10

FAIRCHILD™

PUBLICATION ORDERING INFORMATION

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