



March 2016

# FDMS8320L

## N-Channel PowerTrench<sup>®</sup> MOSFET

40 V, 248 A, 1.1 mΩ

### Features

- Max  $r_{DS(on)}$  = 1.1 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 32\text{ A}$
- Max  $r_{DS(on)}$  = 1.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 27\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

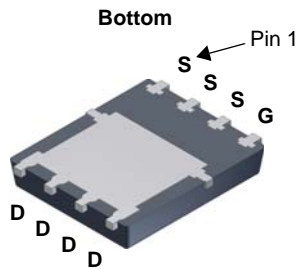
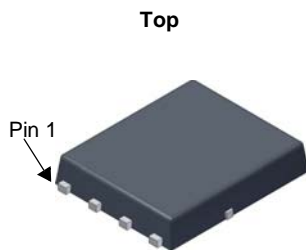


### General Description

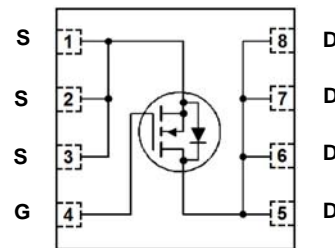
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



Power 56



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	248
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	157
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	36
	-Pulsed	(Note 4)	943
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	264
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	104
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8320L	FDMS8320L	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 32\text{ A}$		0.8	1.1	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 27\text{ A}$		1.0	1.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 32\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		1.2	1.7	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 32\text{ A}$		206		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		8350	11110	pF
$C_{oss}$	Output Capacitance			2840	3780	pF
$C_{rss}$	Reverse Transfer Capacitance			169	295	pF
$R_g$	Gate Resistance		0.1	1.3	2.6	$\Omega$

### Switching Characteristics

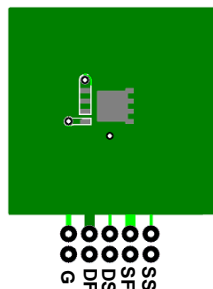
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$ , $I_D = 32\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		17	30	ns
$t_r$	Rise Time			19	35	ns
$t_{d(off)}$	Turn-Off Delay Time			68	110	ns
$t_f$	Fall Time			17	30	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 20\text{ V}$ , $I_D = 32\text{ A}$	121	170	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		58	117	nC
$Q_{gs}$	Gate to Source Charge			19.2		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			16.5		nC

### Drain-Source Diode Characteristics

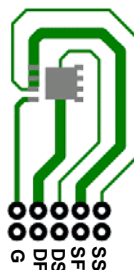
$I_S$	Diode Continuous Forward Current	$T_C = 25\text{ }^\circ\text{C}$			248	A
$I_{S, pulse}$	Diode Pulse Current	$T_C = 25\text{ }^\circ\text{C}$			943	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.65	1.1	V
		$V_{GS} = 0\text{ V}$ , $I_S = 32\text{ A}$ (Note 2)		0.74	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 32\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		68	108	ns
$Q_{rr}$	Reverse Recovery Charge			59	95	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 32\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$		53	85	ns
$Q_{rr}$	Reverse Recovery Charge			104	167	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a)  $50\text{ }^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $125\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 0.3\text{ mH}$ ,  $I_{AS} = 42\text{ A}$ ,  $V_{DD} = 36\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

4. Pulsed  $I_D$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

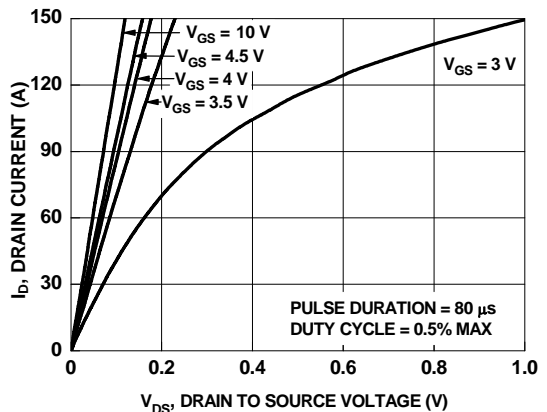


Figure 1. On Region Characteristics

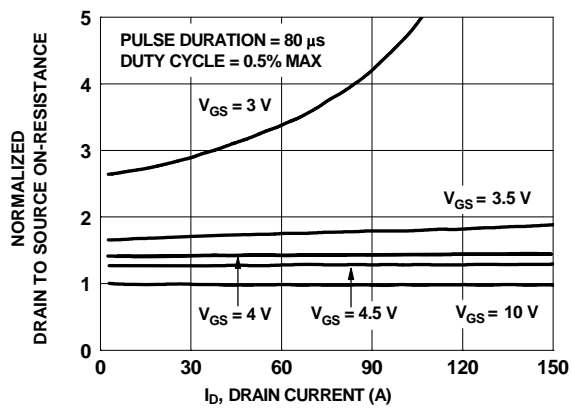


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

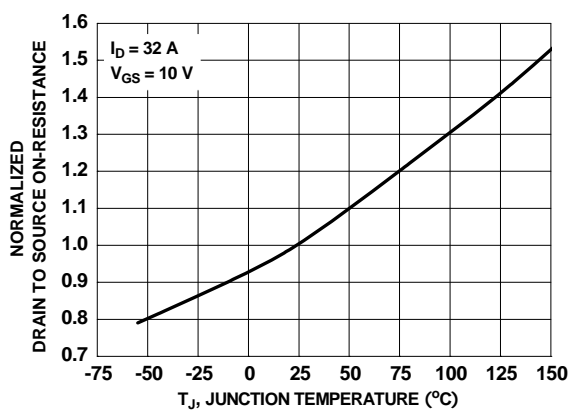


Figure 3. Normalized On Resistance vs. Junction Temperature

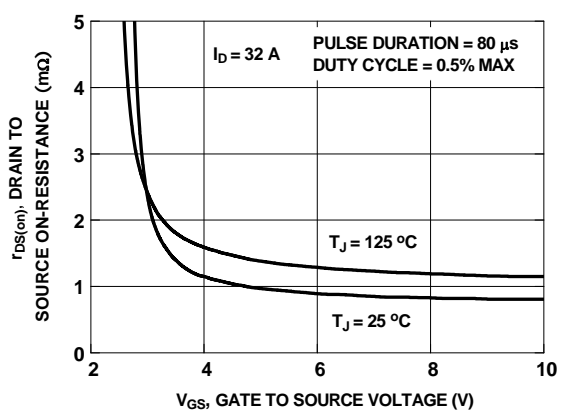


Figure 4. On-Resistance vs. Gate to Source Voltage

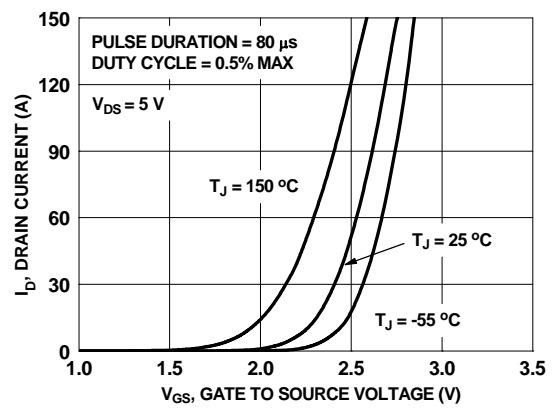


Figure 5. Transfer Characteristics

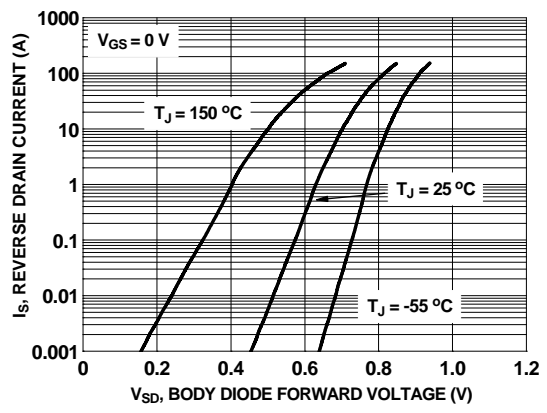
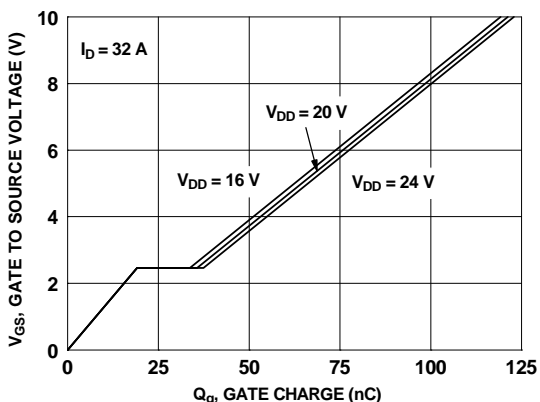
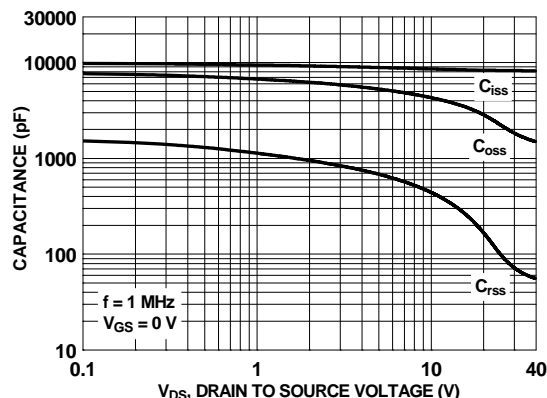


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

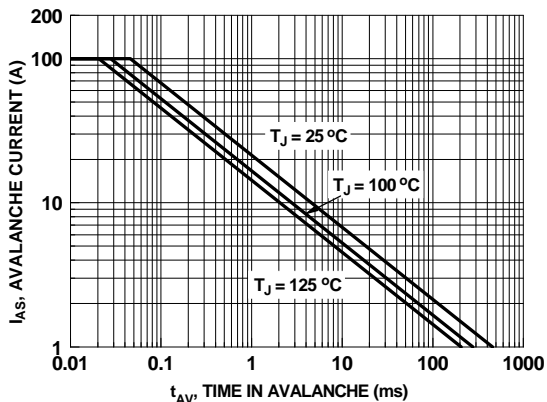
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



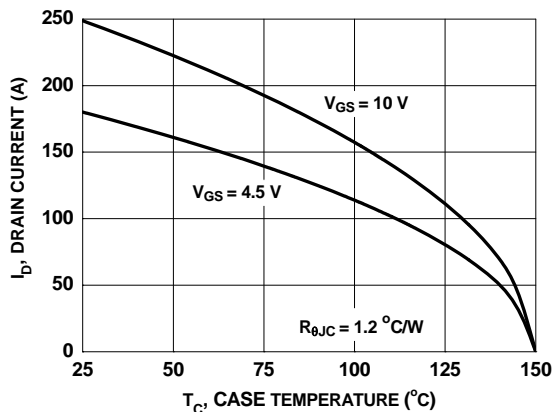
**Figure 7. Gate Charge Characteristics**



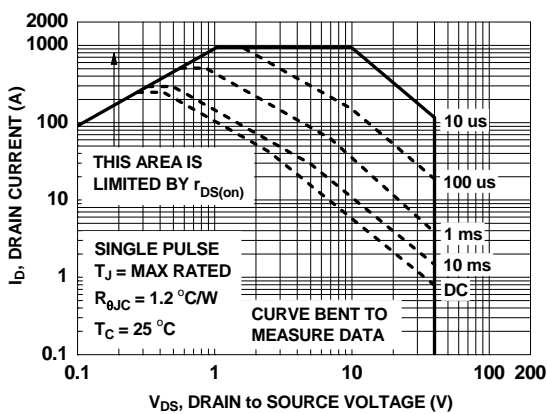
**Figure 8. Capacitance vs. Drain to Source Voltage**



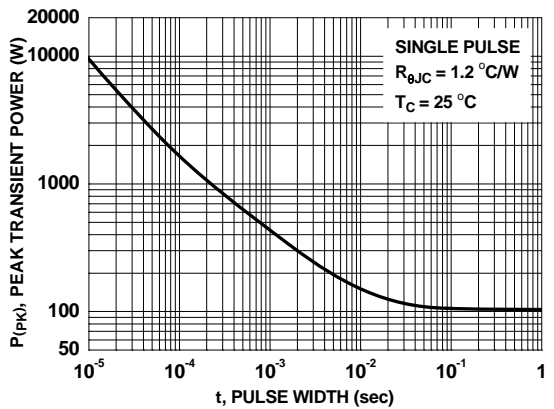
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

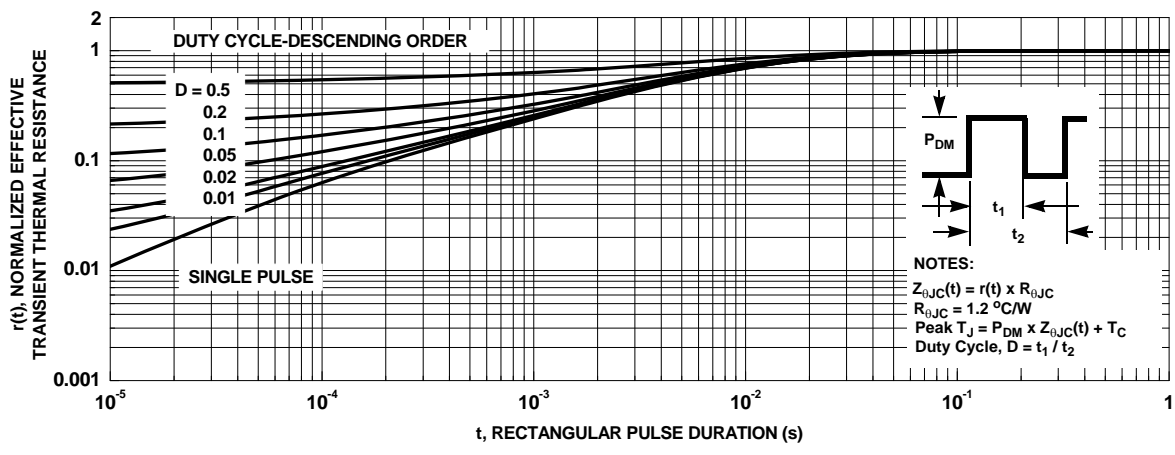


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

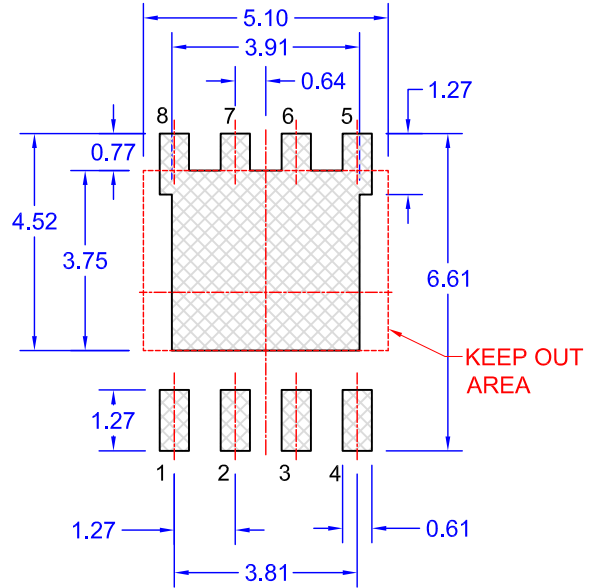
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



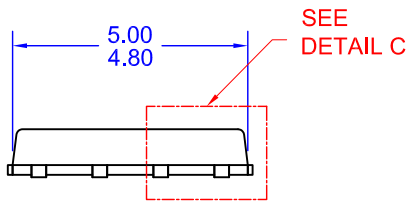
**Figure 13. Transient Thermal Response Curve**



TOP VIEW



LAND PATTERN RECOMMENDATION



SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10



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