



# FDMS8560S

## N-Channel PowerTrench<sup>®</sup> SyncFET<sup>™</sup>

25 V, 70 A, 1.8 mΩ

### Features

- Max  $r_{DS(on)}$  = 1.8 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 30\text{ A}$
- Max  $r_{DS(on)}$  = 2.1 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 28\text{ A}$
- High performance technology for extremely low  $r_{DS(on)}$
- SyncFET<sup>™</sup> Schottky Body Diode
- RoHS Compliant

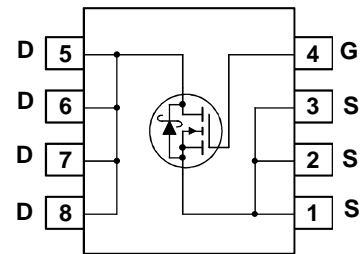
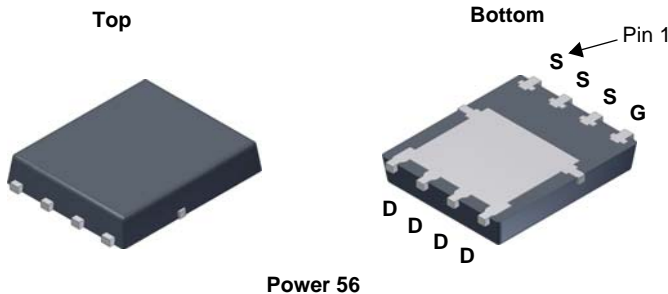


### General Description

This N-Channel SyncFET<sup>™</sup> is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance. This device has the added benefit of an efficient monolithic Schottky body diode.

### Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Rating	Units
$V_{DS}$	Drain to Source Voltage		25	V
$V_{GS}$	Gate to Source Voltage		12	V
$I_D$	Drain Current	-Continuous (Package limited) $T_C = 25^\circ\text{C}$	70	A
		-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	30	
		-Pulsed	150	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	79	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	65	W
		$T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	$T_C = 25^\circ\text{C}$	1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	$T_A = 25^\circ\text{C}$ (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD	FDMS8560S	Power 56	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$		20		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = +12\text{ V}/-8\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.1	1.4	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		1.4	1.8	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 28\text{ A}$		1.6	2.1	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^\circ\text{C}$		2.1	2.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 30\text{ A}$		304		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		4350		pF
$C_{oss}$	Output Capacitance			1270		pF
$C_{rss}$	Reverse Transfer Capacitance			138		pF
$R_g$	Gate Resistance			0.8		$\Omega$

**Switching Characteristics**

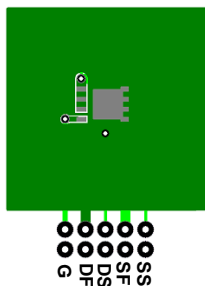
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}, I_D = 30\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		13		ns	
$t_r$	Rise Time			6		ns	
$t_{d(off)}$	Turn-Off Delay Time			45		ns	
$t_f$	Fall Time			5		ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		68		nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$		32		nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 13\text{ V},$ $I_D = 30\text{ A}$		8.2		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			9.6		nC	

**Drain-Source Diode Characteristics**

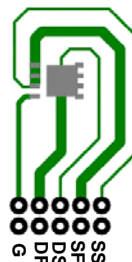
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.6	0.8	V
		$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$ (Note 2)		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 30\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		32		ns
$Q_{rr}$	Reverse Recovery Charge			41		nC

## NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a  $50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

- $E_{AS}$  of 79 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 2.5\text{ mH}$ ,  $I_{AS} = 8\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 33.7\text{ A}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

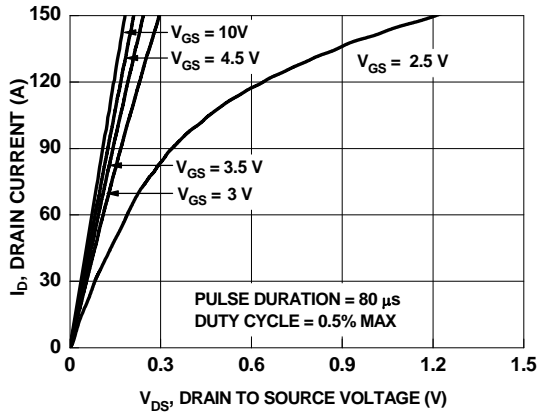


Figure 1. On Region Characteristics

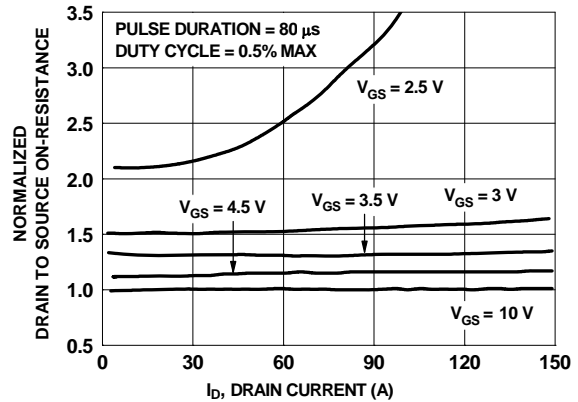


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

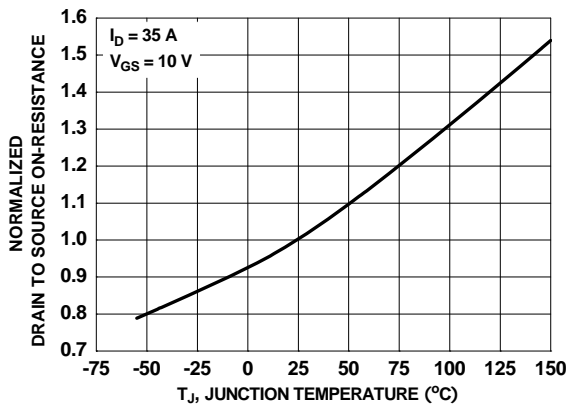


Figure 3. Normalized On Resistance vs Junction Temperature

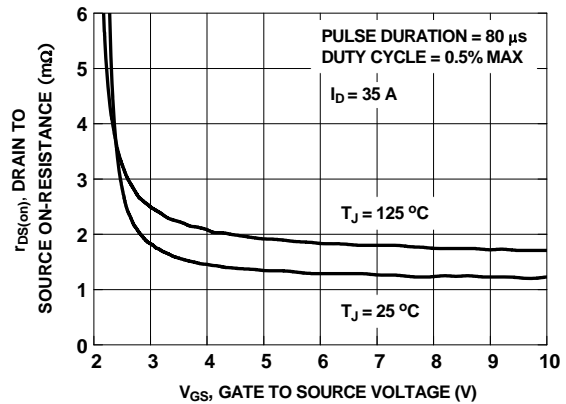


Figure 4. On-Resistance vs Gate to Source Voltage

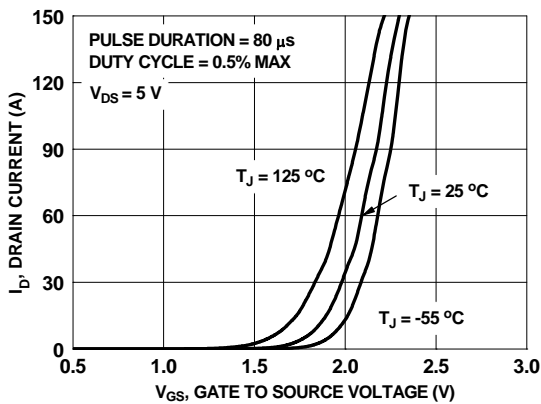


Figure 5. Transfer Characteristics

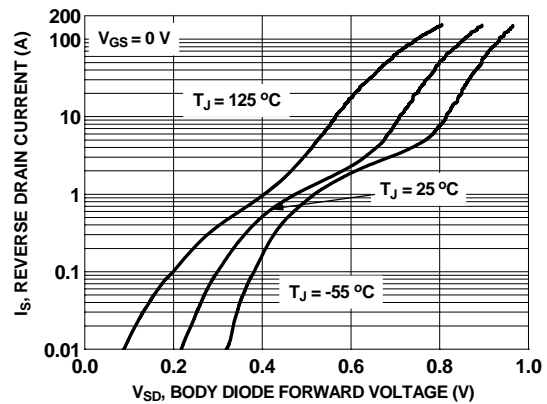
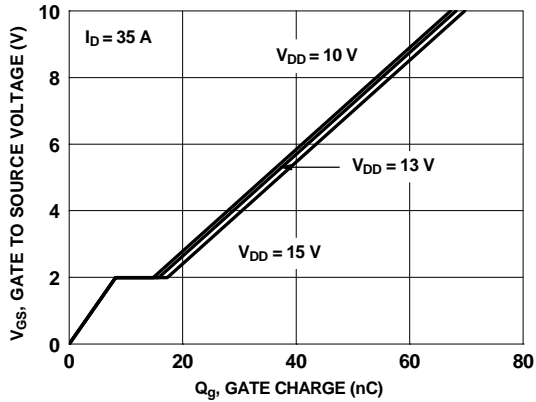
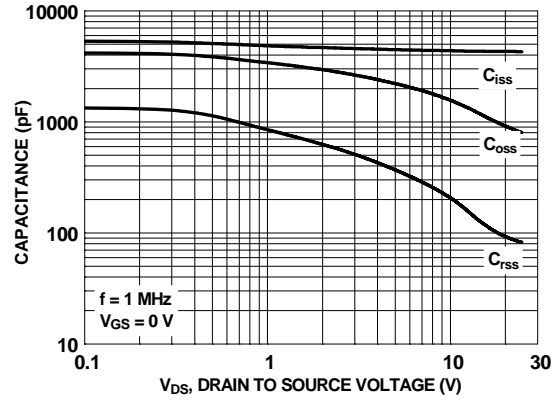


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

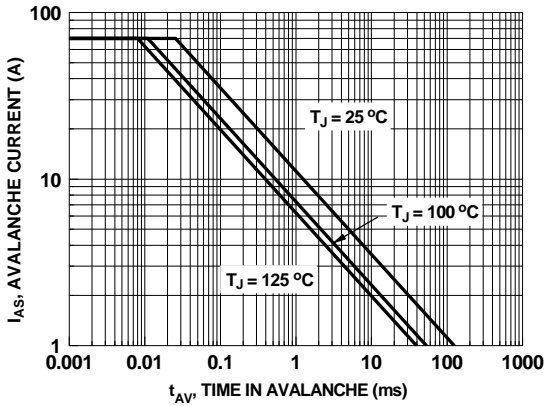
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



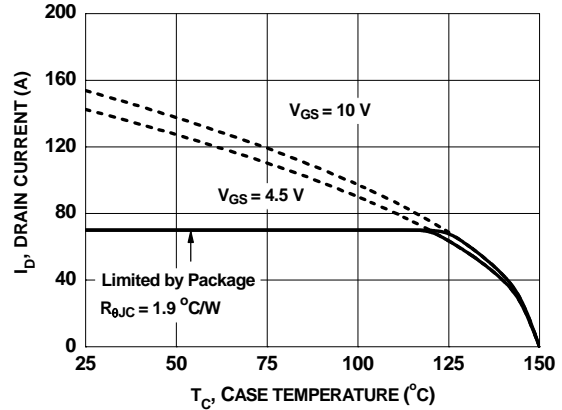
**Figure 7. Gate Charge Characteristics**



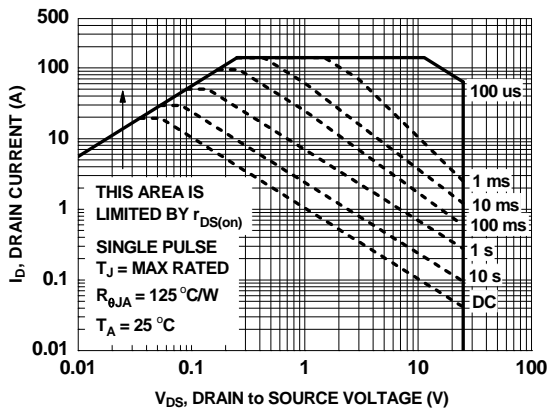
**Figure 8. Capacitance vs Drain to Source Voltage**



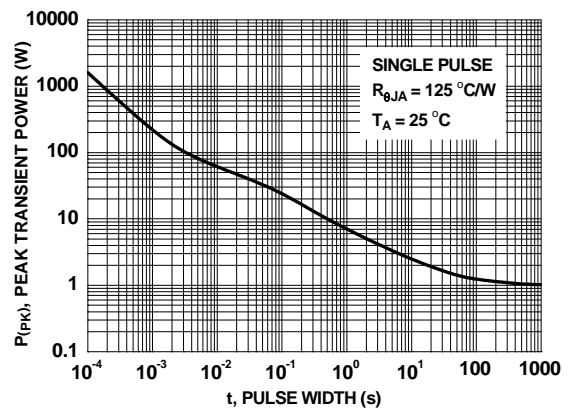
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

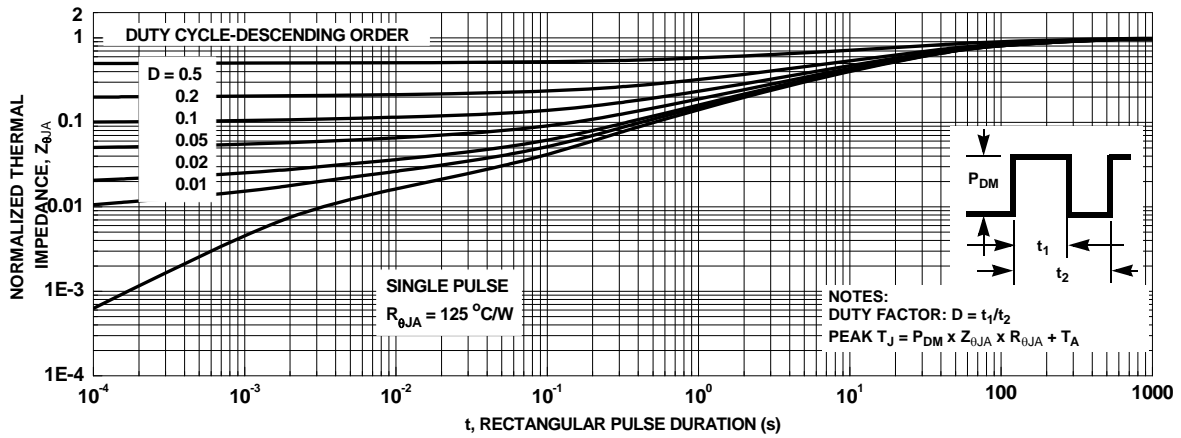


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

### SyncFET<sup>™</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>™</sup> process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8560S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

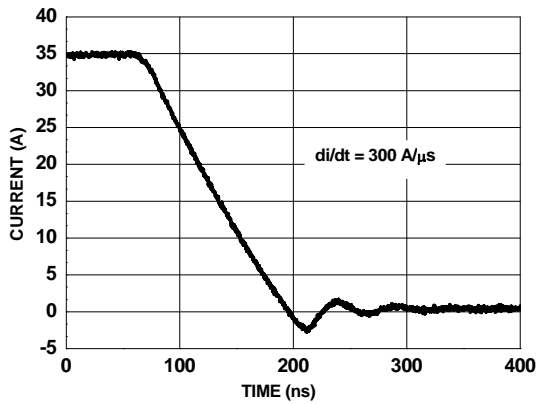


Figure 14. FDMS8560S SyncFET<sup>™</sup> body diode reverse recovery characteristic

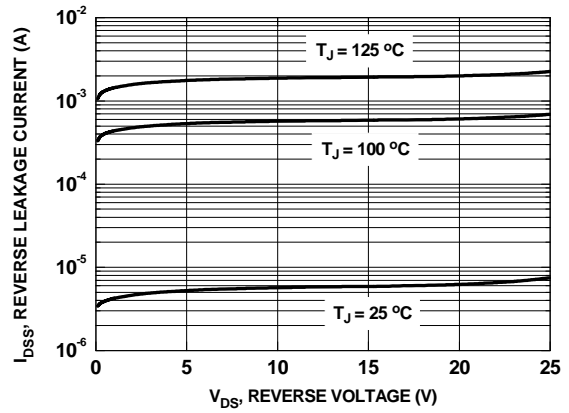
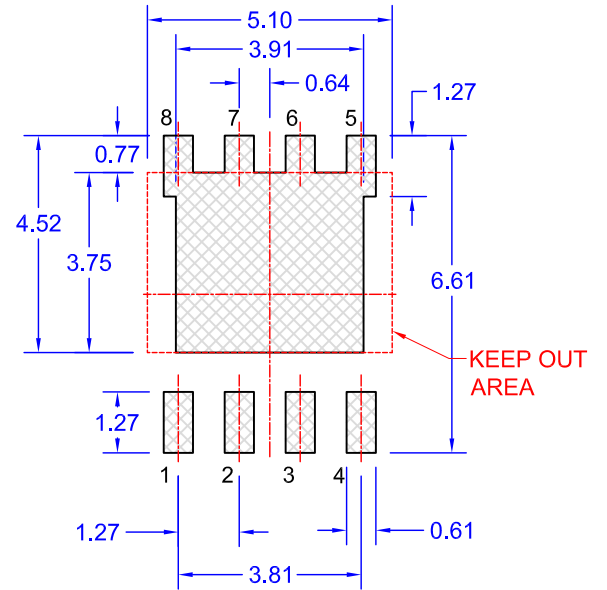


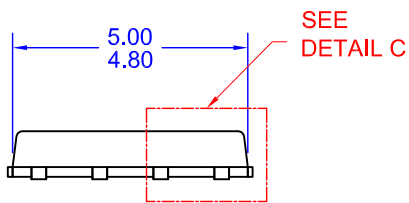
Figure 15. SyncFET<sup>™</sup> body diode reverse leakage versus drain-source voltage



TOP VIEW

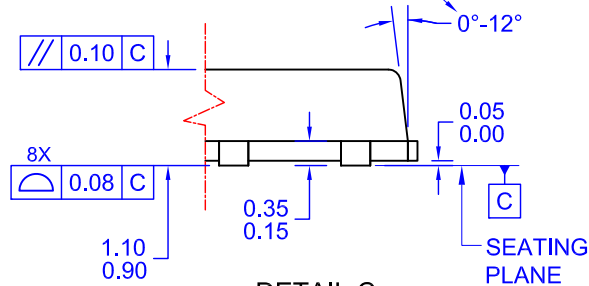


LAND PATTERN RECOMMENDATION

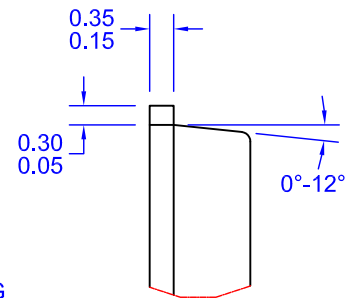


SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10



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