FAIRCHILD

October 2014

FDMS86263P

P-Channel PowerTrench® MOSFET

-150 V, -22 A, 53 mΩ

Features

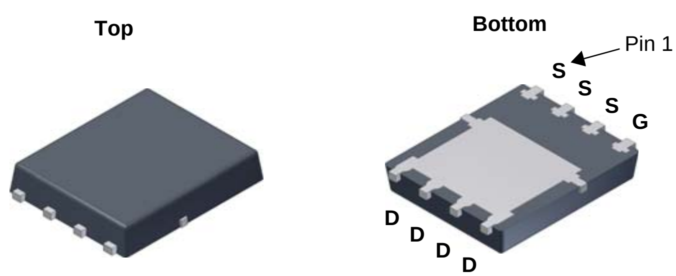
- Max $r_{DS(on)}$ = 53 mΩ at V_{GS} = -10 V, I_D = -4.4 A
- Max $r_{DS(on)}$ = 64 mΩ at V_{GS} = -6 V, I_D = -4 A
- Very low Rds-on in Mid-Voltage P-Channel silicon technology optimized for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL tested
- RoHS Compliant

General Description

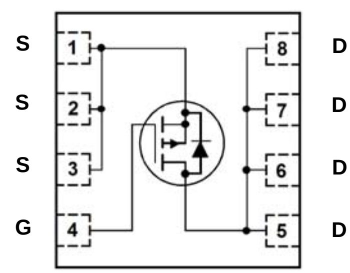
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

Applications

- Active Clamp Switch
- Load Switch



Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-150	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current -Continuous T_C = 25 °C	-22	A
	-Continuous T_A = 25 °C (Note 1a)	-4.4	
	-Pulsed	-70	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	384	mJ
P_D	Power Dissipation T_C = 25 °C	104	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86263P	FDMS86263P	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-116		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -120 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-2	-2.9	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -4.4 A		42	53	mΩ
		V_{GS} = -6 V, I_D = -4 A		45	64	
		V_{GS} = -10 V, I_D = -4.4 A, T_J = 125 °C		71	94	
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -4.4 A		19		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -75 V, V_{GS} = 0 V, f = 1 MHz		2935	3905	pF
C_{oss}	Output Capacitance			238	315	pF
C_{rss}	Reverse Transfer Capacitance			11	20	pF
R_g	Gate Resistance		0.1	2.7	5.4	Ω

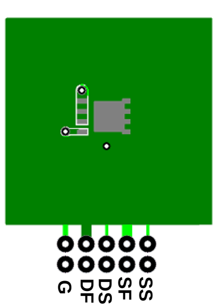
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75 V, I_D = -4.4 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		17	31	ns
t_r	Rise Time			10	21	ns
$t_{d(off)}$	Turn-Off Delay Time			37	59	ns
t_f	Fall Time			14	25	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -75 V, I_D = -4.4 A		45	63	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to -6 V; V_{DD} = -75 V, I_D = -4.4 A		29	40	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -75 V, I_D = -4.4 A		11.3		nC
Q_{gd}	Gate to Drain "Miller" Charge			8.9		nC

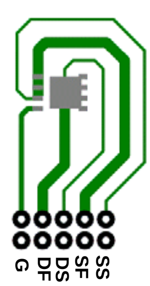
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -4.4 A (Note 2)		-0.79	-1.3	V
		V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.75	-1.2	
t_{rr}	Reverse Recovery Time	I_F = -4.4 A, di/dt = 100 A/μs		91	146	ns
Q_{rr}	Reverse Recovery Charge			287	460	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25 °C; P-ch: L = 3 mH, I_{AS} = -16 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.1 mH, I_{AS} = -52 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

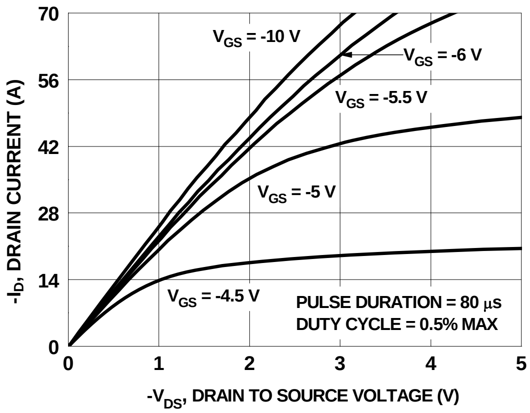


Figure 1. On Region Characteristics

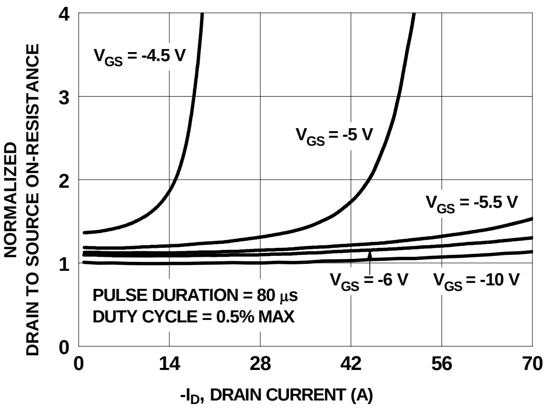


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

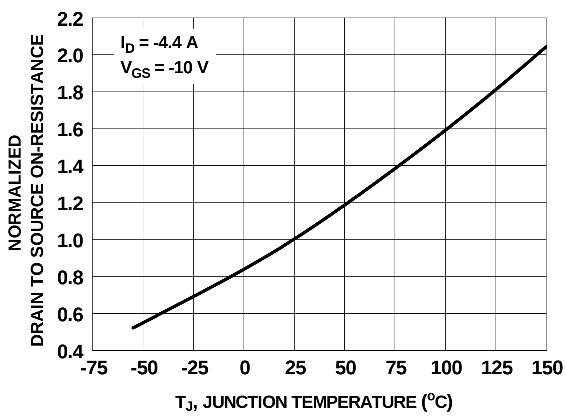


Figure 3. Normalized On Resistance vs Junction Temperature

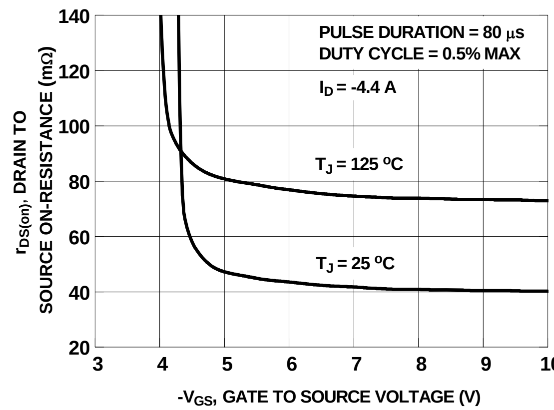


Figure 4. On-Resistance vs Gate to Source Voltage

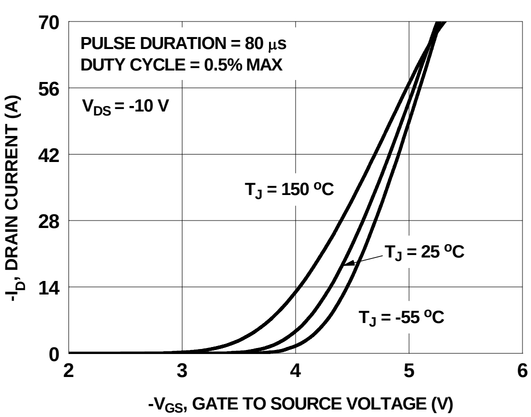


Figure 5. Transfer Characteristics

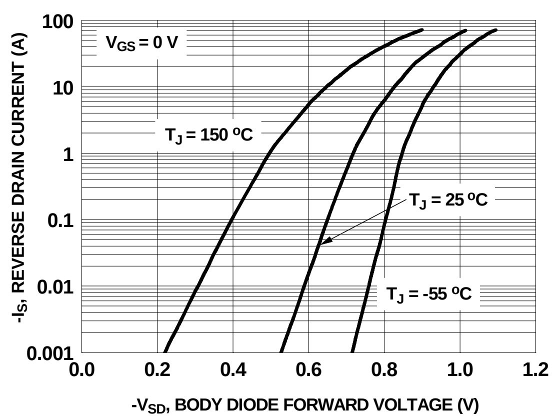


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

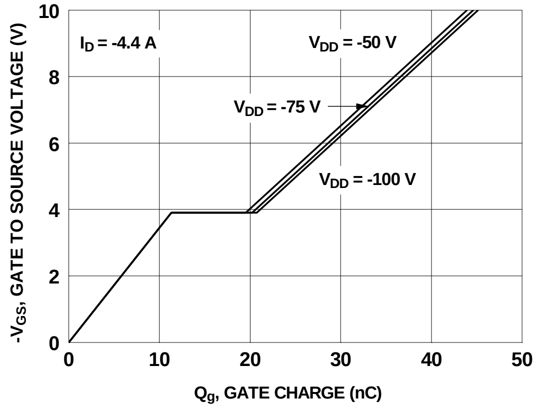


Figure 7. Gate Charge Characteristics

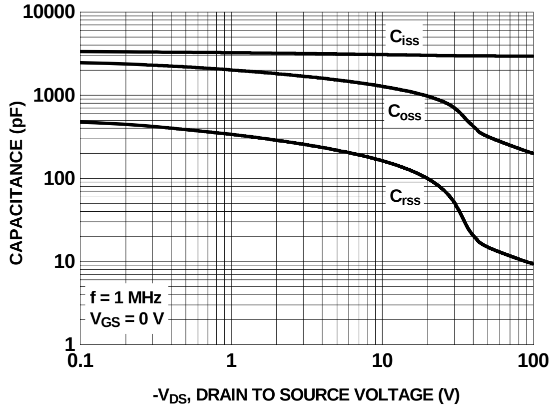


Figure 8. Capacitance vs Drain to Source Voltage

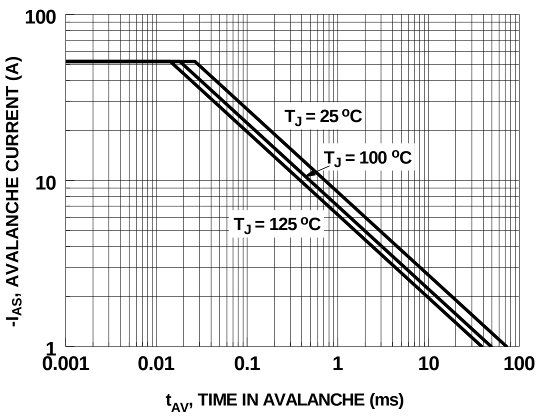


Figure 9. Unclamped Inductive Switching Capability

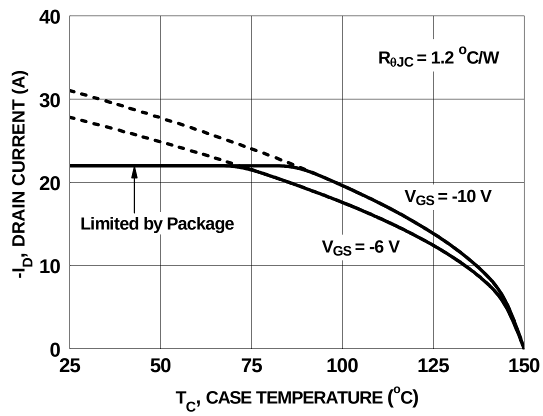


Figure 10. Maximum Continuous Drain Current vs Case Temperature

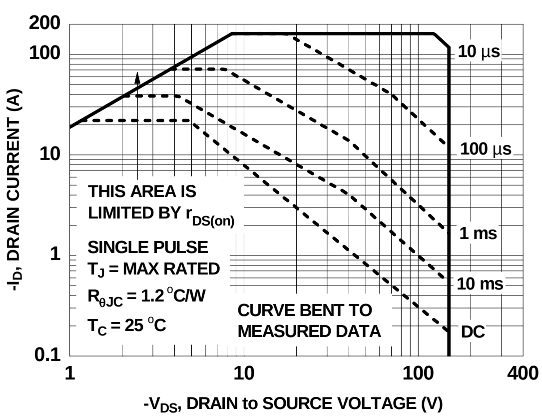


Figure 11. Forward Bias Safe Operating Area

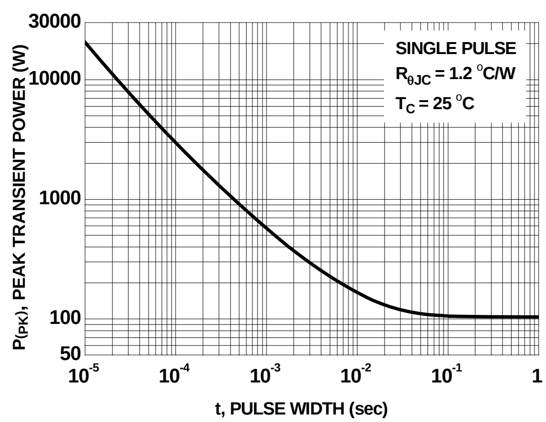


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

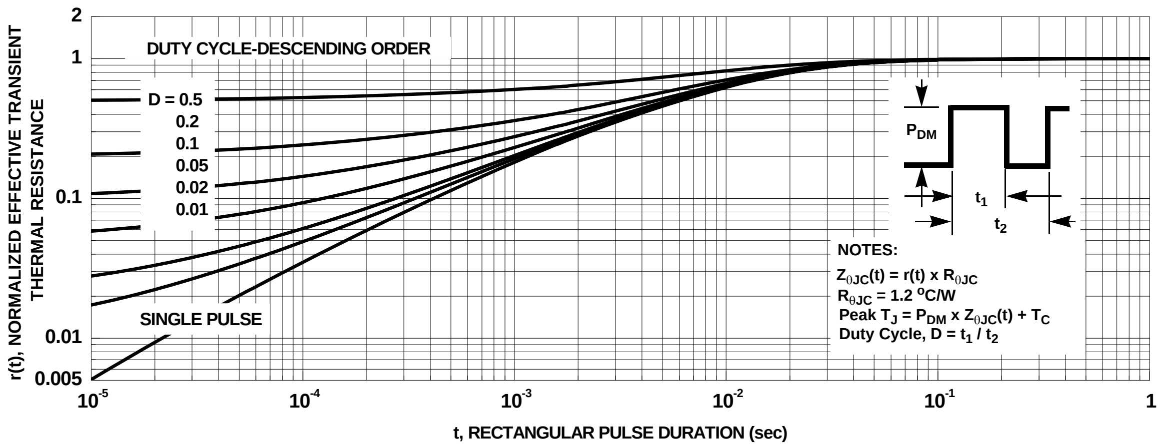
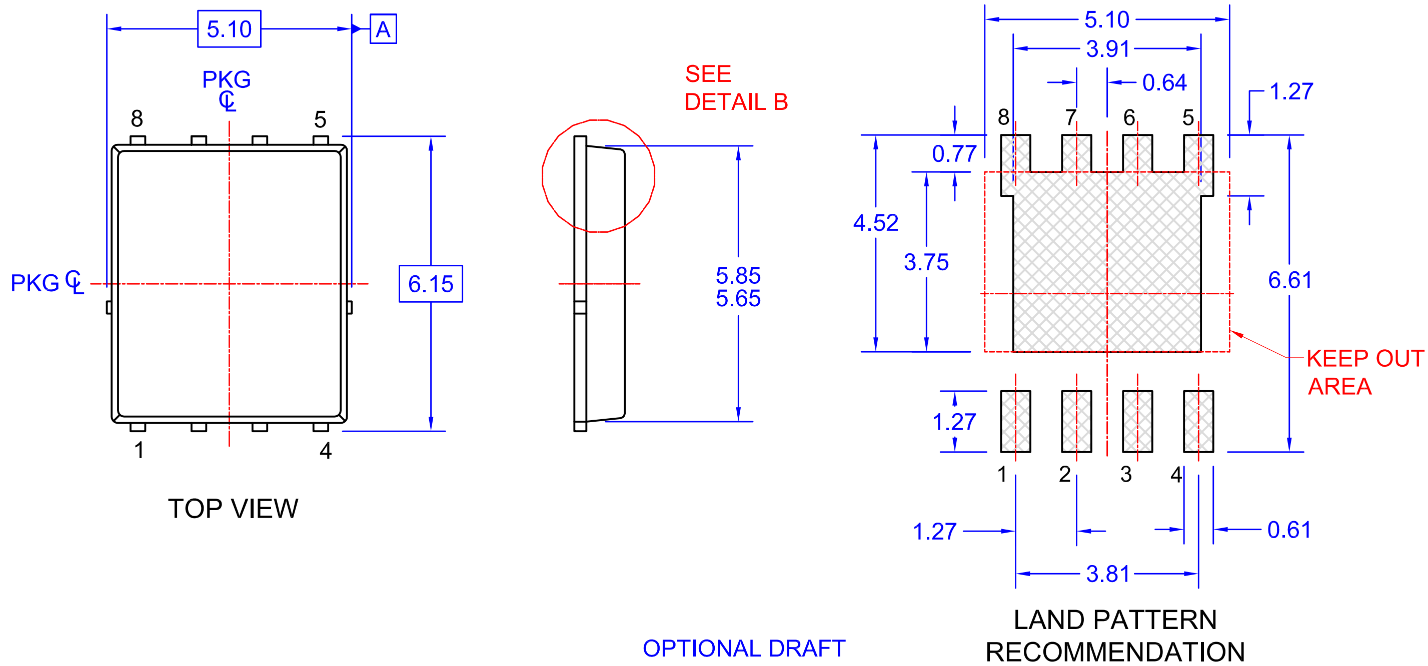
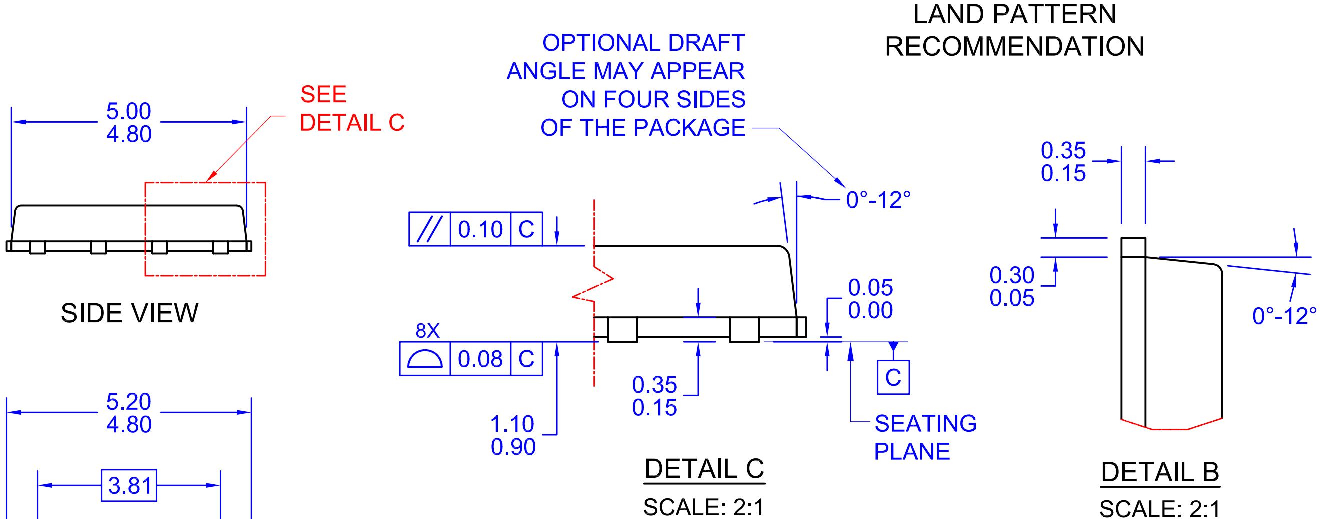
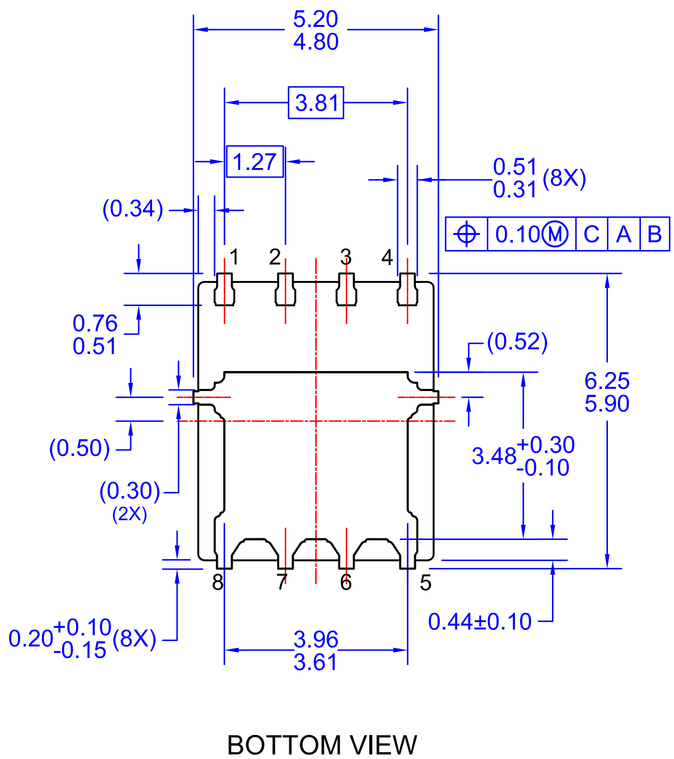


Figure 13. Junction-to-Case Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.

B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F. DRAWING FILE NAME: PQFN08AREV10

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