FAIRCHILD™

December 2014

# FDMS86568_F085

N-Channel PowerTrench® MOSFET

60 V, 80 A, 3.5 mΩ

Features

- Typical $R_{DS(on)}$ = 2.6 mΩ at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 55 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems

100% RoHS COMPLIANT

Top   Bottom   Pin 1
S S S G
D D D D

Power 56

D	5		4	G
D	6		3	S
D	7		2	S
D	8		1	S
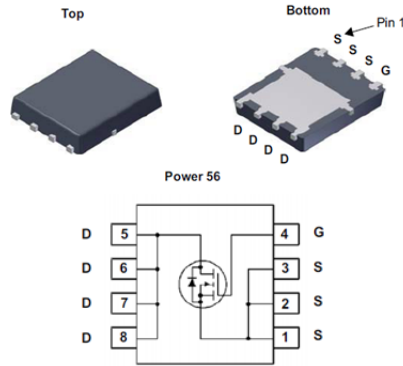
For current package drawing, please refer to the Fairchild web-site at https://www.fairchildsemi.com/package-drawings/PQ/PQFN08M.pdf

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		60	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1) T_C = 25°C		80	A
	Pulsed Drain Current T_C = 25°C		See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)		102	mJ
P_D	Power Dissipation		214	W
	Derate Above 25°C		1.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.7	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)		50	°C/W

Notes:
1: Current is limited by bondwire configuration.
2: Starting T_J = 25°C, L = 50uH, I_{AS} = 64A, V_{DD} = 60V during inductor charging and V_{DD} = 0V during time in avalanche.
3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86568	FDMS86568_F085	Power56	13"	12mm	3000units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V		60	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=60V V_{GS} = 0V	T_J = 25°C	-	-	1	µA
			T_J = 175°C (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA		2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80A, V_{GS}= 10V	T_J = 25°C	-	2.6	3.5	mΩ
			T_J = 175°C (Note 4)	-	4.9	6.6	mΩ
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz		-	4335	-	pF
C_{oss}	Output Capacitance			-	1065	-	pF
C_{rss}	Reverse Transfer Capacitance			-	36	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.5	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10V	V_{DD} = 48V I_D = 80A	-	55	71	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	8	-	nC
Q_{gs}	Gate-to-Source Gate Charge			-	23	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	9	-	nC
Switching Characteristics							
t_{on}	Turn-On Time	V_{DD} = 30V, I_D = 80A, V_{GS} = 10V, R_{GEN} = 6Ω		-	-	64	ns
$t_{d(on)}$	Turn-On Delay			-	21	-	ns
t_r	Rise Time			-	20	-	ns
$t_{d(off)}$	Turn-Off Delay			-	33	-	ns
t_f	Fall Time			-	13	-	ns
t_{off}	Turn-Off Time			-	-	64	ns
Drain-Source Diode Characteristics							
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} =80A, V_{GS} = 0V		-	-	1.25	V
		I_{SD} = 40A, V_{GS} = 0V		-	-	1.2	V
t_{rr}	Reverse-Recovery Time	I_F = 80A, dI_{SD}/dt = 100A/ms V_{DD} = 48V		-	67	87	ns
Q_{rr}	Reverse-Recovery Charge			-	70	99	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

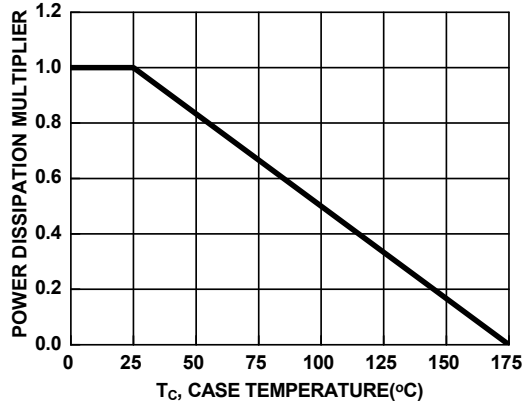FDMS86568_F085 N-Channel PowerTrench® MOSFET

Typical Characteristics

Figure 1. Normalized Power Dissipation vs. Case Temperature
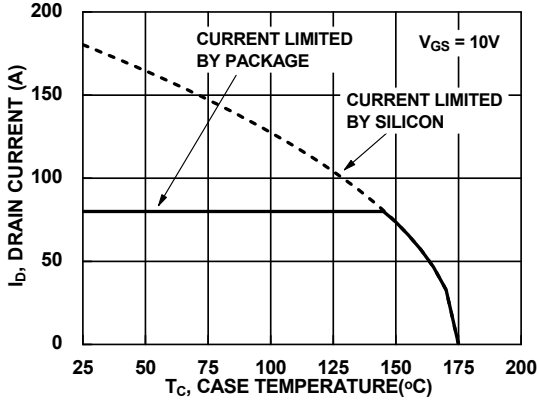
Figure 2. Maximum Continuous Drain Current vs. Case Temperature
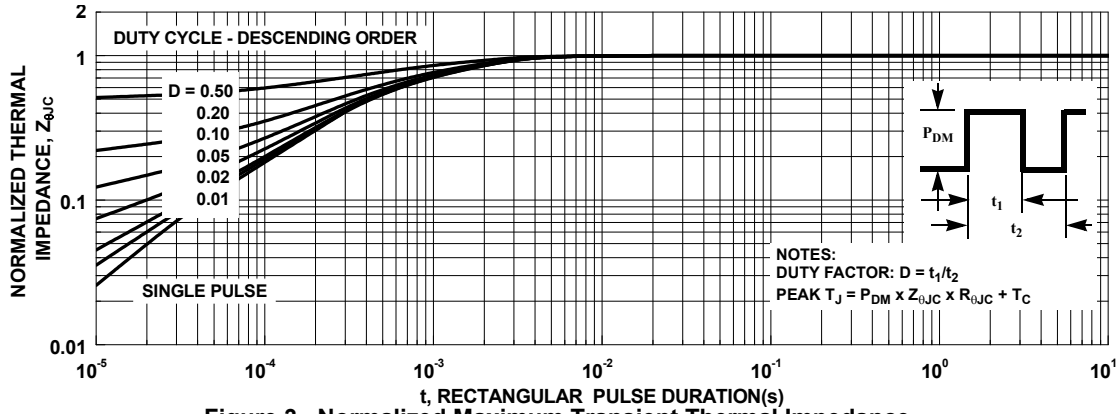

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 3. Normalized Maximum Transient Thermal Impedance

$V_{GS} = 10V$

$T_C = 25^oC$
FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_2 \left[\sqrt{\frac{175 - T_C}{150}} \right]$$
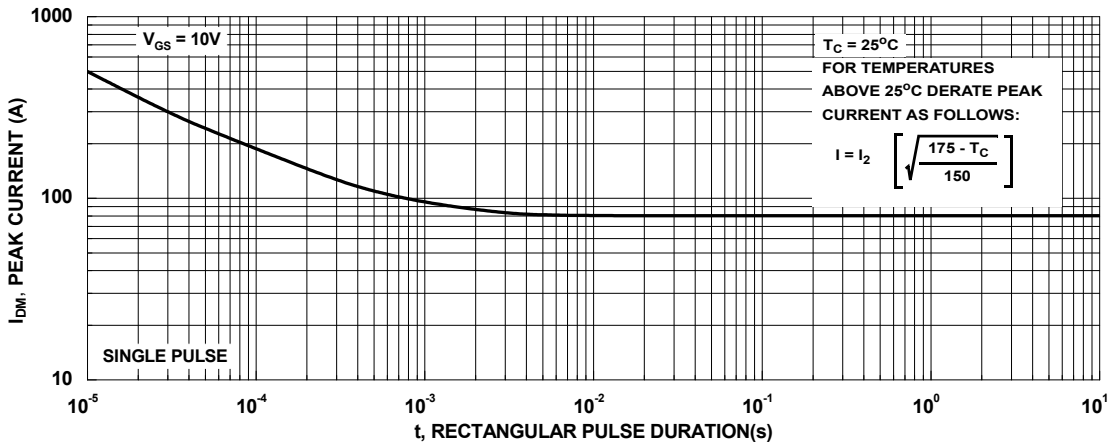
Figure 4. Peak Current Capability

Typical Characteristics
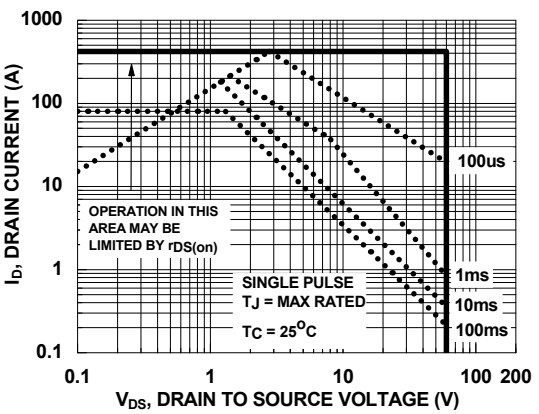
Figure 5. Forward Bias Safe Operating Area
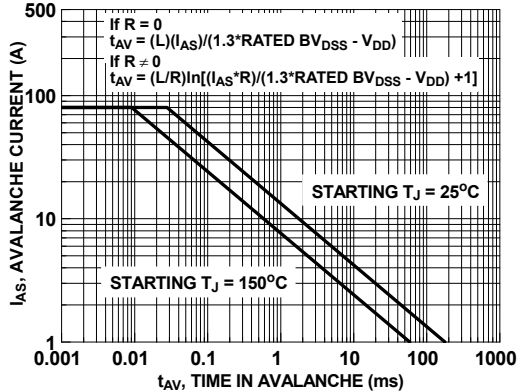
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability
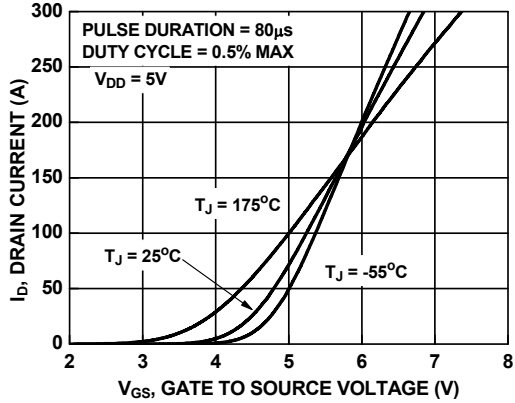
Figure 7. Transfer Characteristics
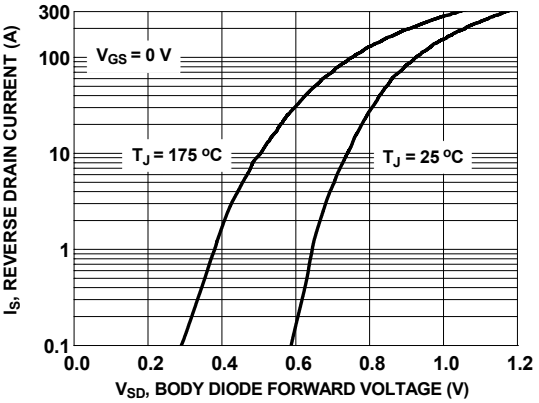
Figure 8. Forward Diode Characteristics
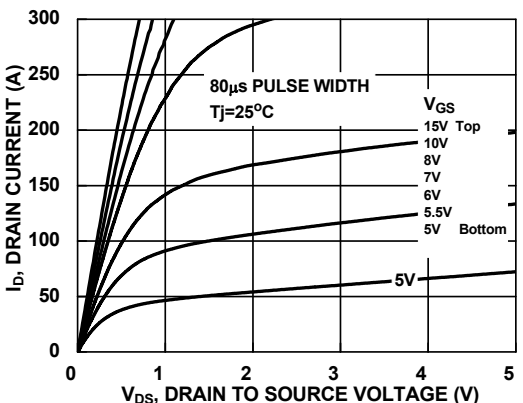
Figure 9. Saturation Characteristics
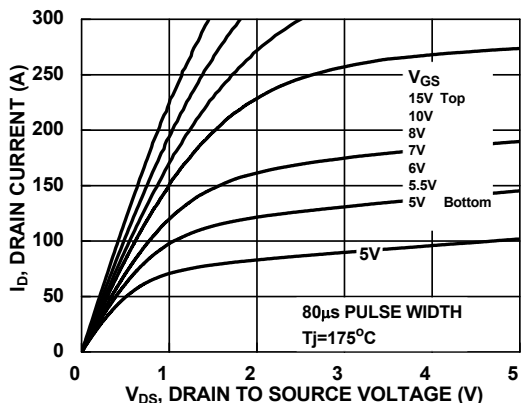
Figure 10. Saturation Characteristics

Typical Characteristics
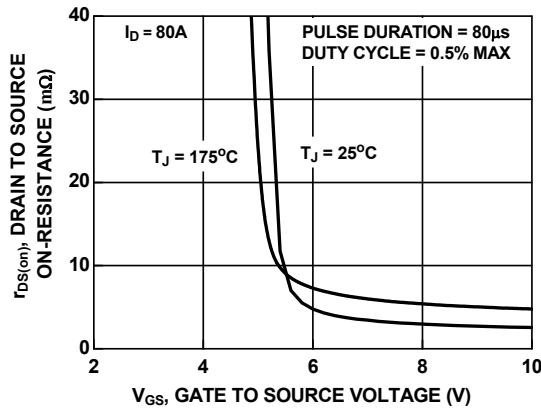
Figure 11. R~DSON~ vs. Gate Voltage
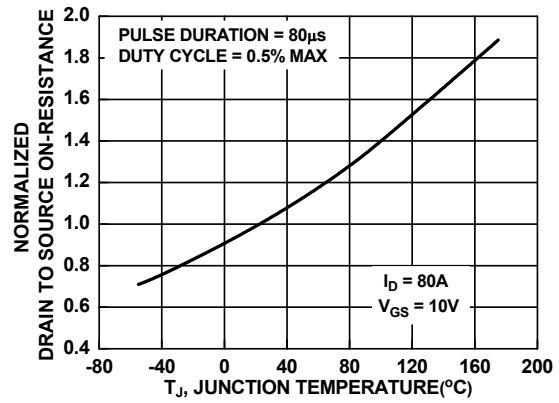
Figure 12. Normalized R~DSON~ vs. Junction Temperature
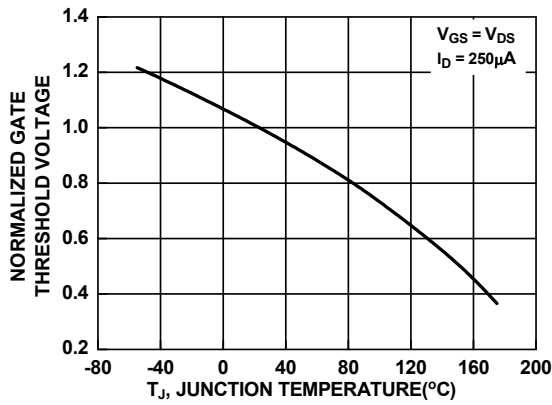
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
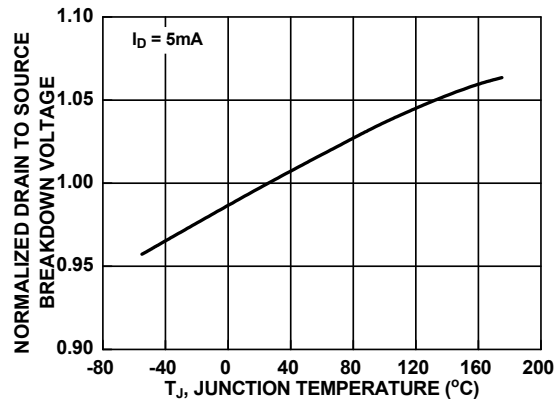
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
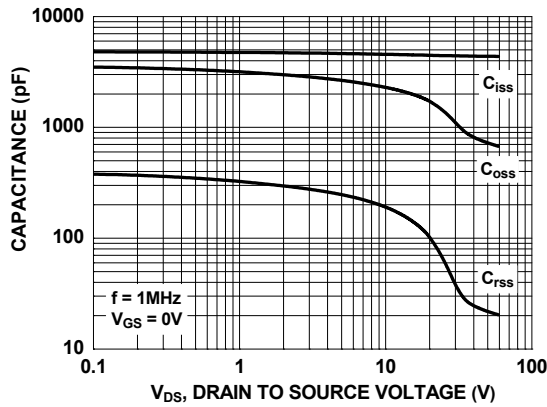
Figure 15. Capacitance vs. Drain to Source Voltage
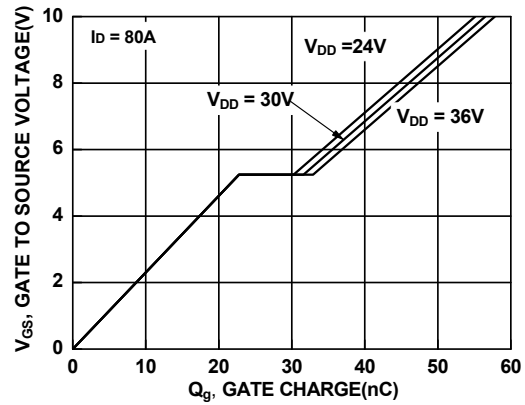
Figure 16. Gate Charge vs. Gate to Source Voltage

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