

MOSFET – N-Channel, 2.5 V Specified, POWERTRENCH®

20 V, 1.7 A, 100 mΩ

FDN335N

General Description

This N-Channel 2.5 V specified MOSFET is produced using onsemi advanced POWERTRENCH® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Features

- 1.7 A, 20 V
 - $R_{DS(ON)} = 0.07 \Omega @ V_{GS} = 4.5 V$
 - $R_{DS(ON)} = 0.1 \Omega @ V_{GS} = 2.5 V$
- Low Gate Charge (3.5 nC typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and is RoHS Compliant

Applications

- DC-DC Converter
- Load Switch

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$, unless otherwise noted)

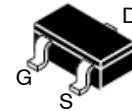
Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 8	V
I_D	Drain Current	Continuous (Note 1a)	1.7
		Pulsed	8
P_D	Power Dissipation for Single Operation	(Note 1a)	0.5
		(Note 1b)	0.46
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise noted)

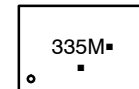
Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ C/W$

V_{DS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
20 V	$0.07 \Omega @ 4.5 V$	1.7 A
	$0.1 \Omega @ 2.5 V$	



SOT-23/SUPERSOT™-23, 3 LEAD, 1.4x2.9
CASE 527AG

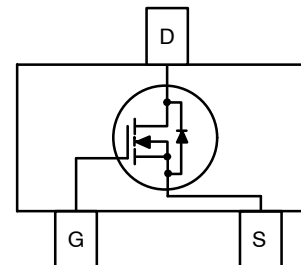
MARKING DIAGRAM



335 = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)
* Date Code orientation and/or overbar may vary depending upon manufacturing location

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDN335N

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	14	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V	–	–	1	μA
I _{GSSF}	Gate to Source Leakage Current, Forward	V _{GS} = 8 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate to Source Leakage Current, Reverse	V _{GS} = –8 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.4	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–3	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5 V, I _D = 1.7 A	–	0.055	0.07	Ω
		V _{GS} = 4.5 V, I _D = 1.7 A, T _J = 125°C	–	0.079	0.12	
		V _{GS} = 2.5 V, I _D = 1.5 A	–	0.078	0.10	
I _{D(on)}	On–State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	8	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 1.5 A	–	7	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	–	310	–	pF
C _{oss}	Output Capacitance		–	80	–	pF
C _{rss}	Reverse Transfer Capacitance		–	40	–	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 4.5 V, R _{GEN} = 6 Ω	–	5	15	ns
t _r	Turn–On Rise Time		–	8.5	17	ns
t _{d(off)}	Turn–Off Delay Time		–	11	20	ns
t _f	Turn–Off Fall Time		–	3	10	ns
Q _g	Total Gate Charge	V _{DS} = 10 V, I _D = 1.7 A, V _{GS} = 4.5 V	–	3.5	5	nC
Q _{gs}	Gate–Source Charge		–	0.55	–	nC
Q _{gd}	Gate–Drain Charge		–	0.95	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	0.42	A
V _{SD}	Source–Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.42 A (Note 2)	–	0.7	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 250°C/W when mounted on
a 0.02 in² pad of 2 oz copper



b) 270°C/W when mounted on
a minimum pad

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

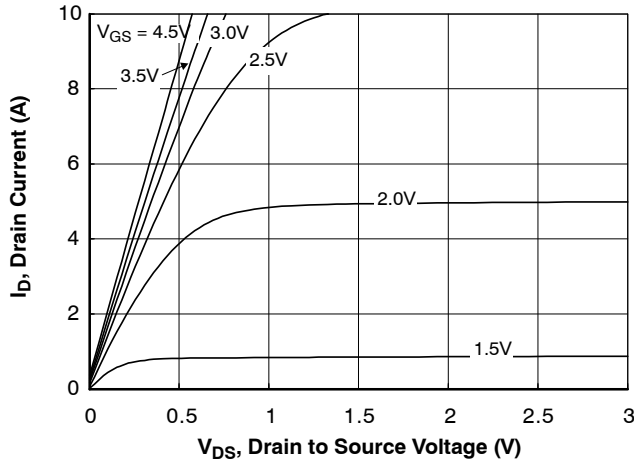


Figure 1. On Region Characteristics

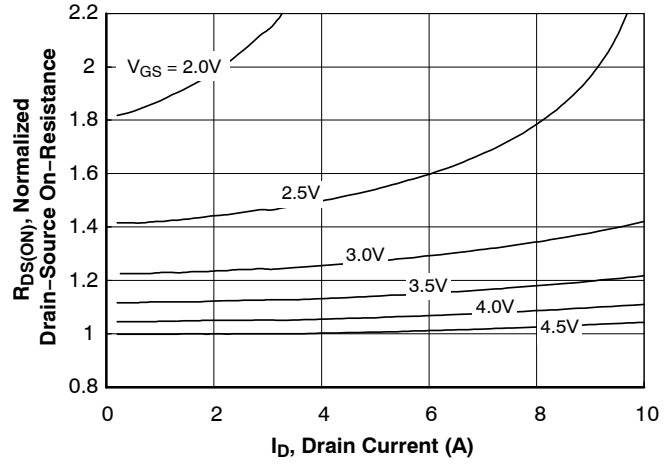


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

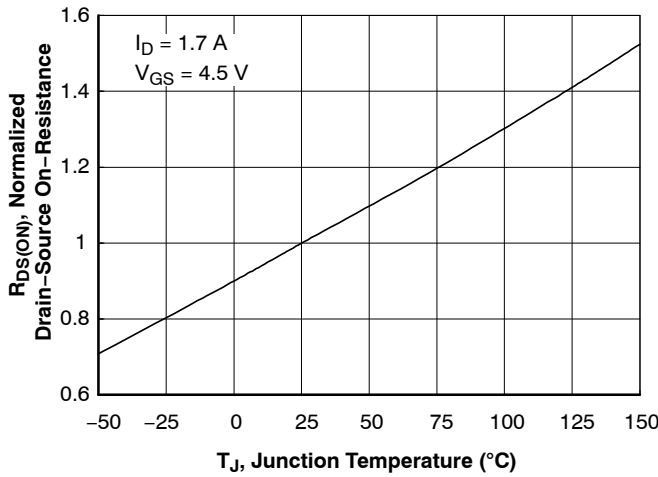


Figure 3. On-Resistance Variation with Temperature

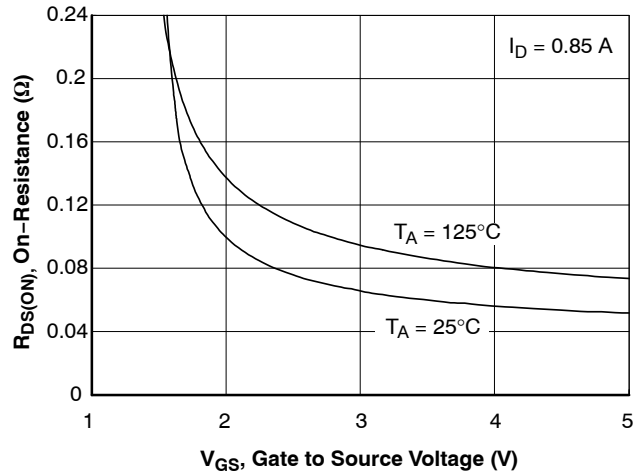


Figure 4. On-Resistance Variation with Gate to Source Voltage

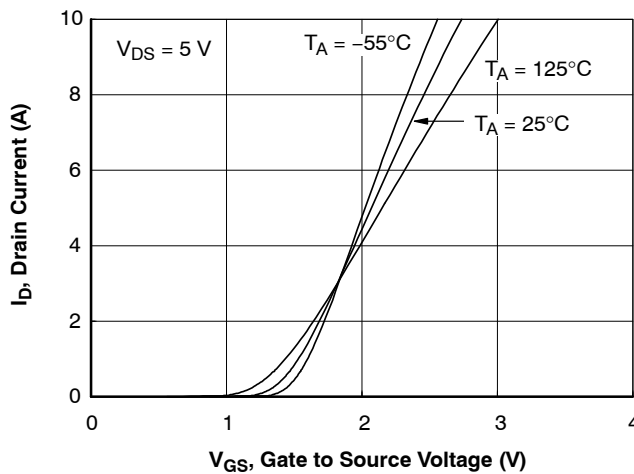


Figure 5. Transfer Characteristics

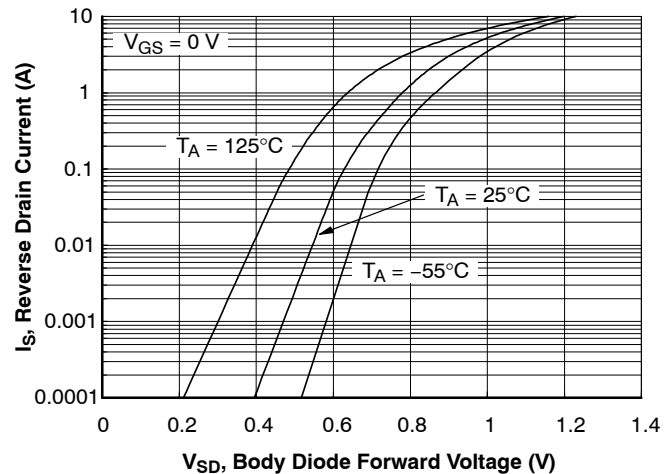


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

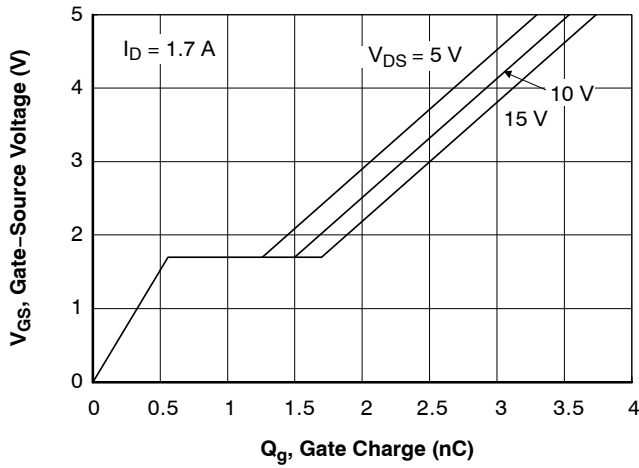


Figure 7. Gate Charge Characteristics

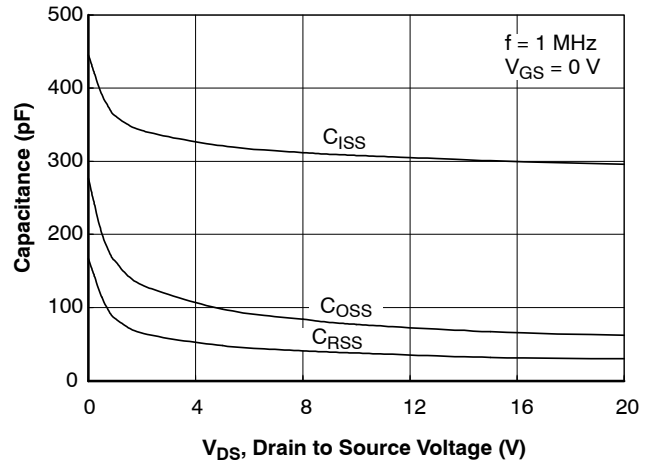


Figure 8. Capacitance vs Drain to Source Voltage

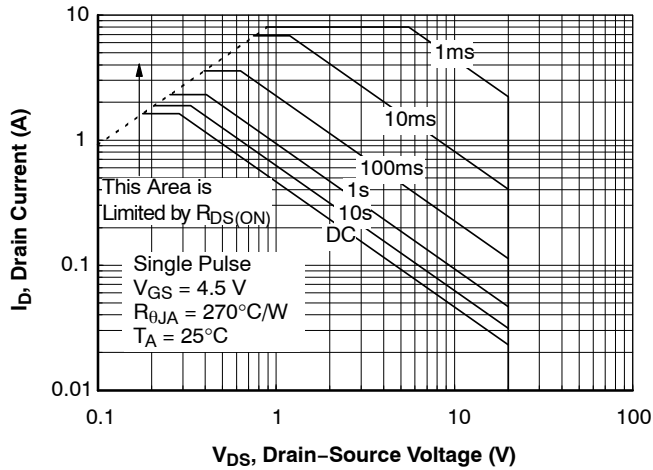


Figure 9. Maximum Safe Operating Area

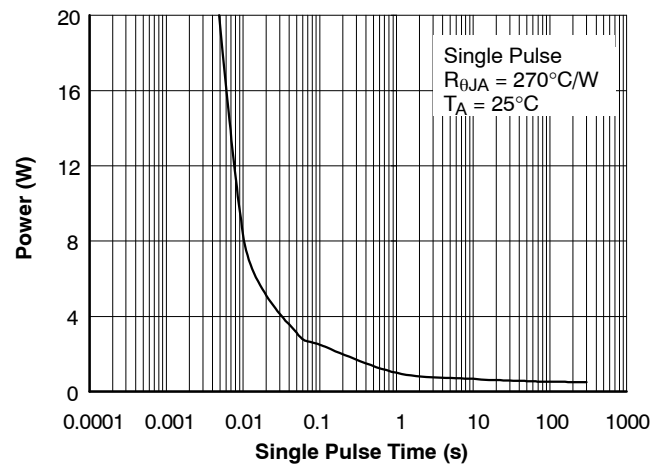


Figure 10. Single Pulse Maximum Power Dissipation

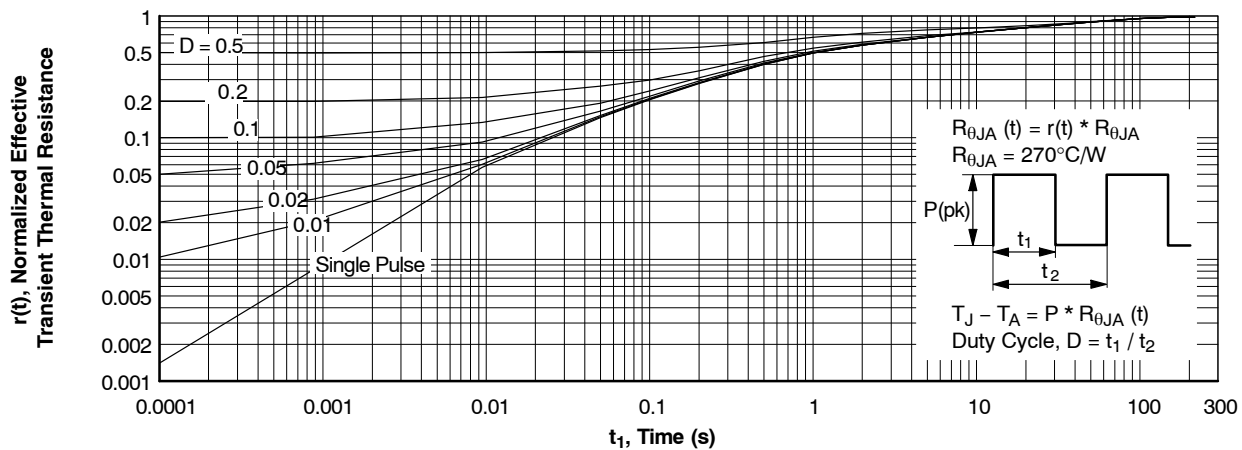


Figure 11. Transient Thermal Response Curve

NOTE: Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

FDN335N

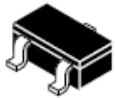
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
FDN335N	335M (see Marking Diagram on the front page)	SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

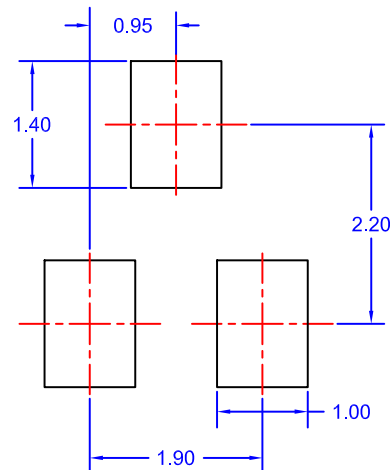
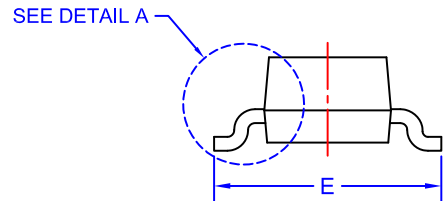
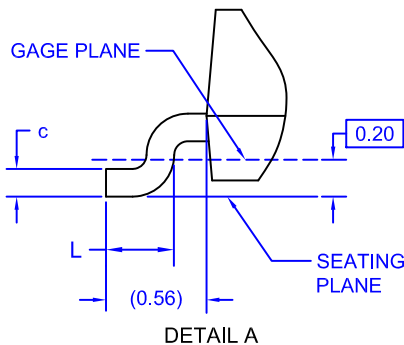
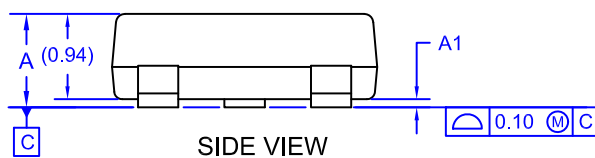
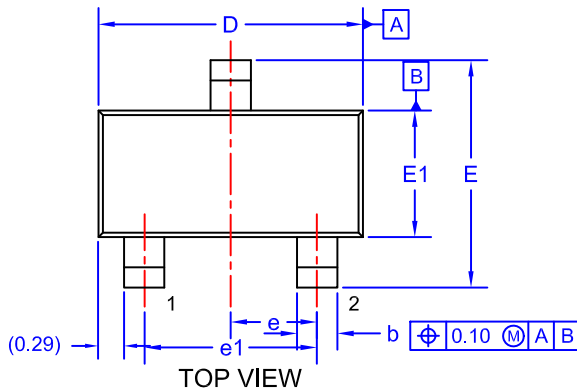
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9 CASE 527AG ISSUE A

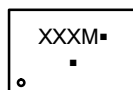
DATE 09 DEC 2019



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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