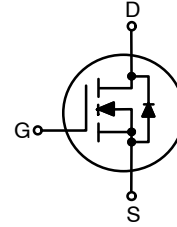


# Transistor - N-Channel, Logic Level, Enhancement Mode Field Effect

## FDN337N



### General Description

SUPERSOT™ –3 N-Channel logic level enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 2.2 A, 30 V
  - ♦  $R_{DS(on)} = 0.065 \Omega @ V_{GS} = 4.5 \text{ V}$
  - ♦  $R_{DS(on)} = 0.082 \Omega @ V_{GS} = 2.5 \text{ V}$
- Industry Standard Outline SOT–23 Surface Mount Package Using Proprietary SUPERSOT–3 Design for Superior Thermal and Electrical Capabilities
- High Density Cell Design for Extremely Low  $R_{DS(on)}$
- Exceptional on-Resistance and Maximum DC Current Capability
- This Device is Pb-Free and Halogen Free

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

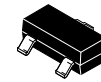
Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage – Continuous	$\pm 8$	V
$I_D$	Drain/Output Current – Continuous	2.2	A
	Drain/Output Current – Pulsed	10	
$P_D$	Maximum Power Dissipation (Note 1a)	0.5	W
	Maximum Power Dissipation (Note 1b)	0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

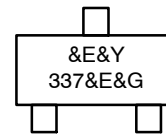
$T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C}/\text{W}$



SOT–23–3  
CASE 527AG

### MARKING DIAGRAM



- &E; = Designates Space
- &Y; = Binary Calendar Year Coding Scheme
- 337 = Specific Device Code
- &G; = Date Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDN337N	SOT–23–3 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDN337N

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	41	–	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ , $T_J = 55^\circ\text{C}$	–	–	10	
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA

## ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	0.7	1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	-2.3	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.2\text{ A}$	–	0.054	0.065	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 2.2\text{ A}$ , $T_J = 125^\circ\text{C}$	–	0.08	0.11	
		$V_{GS} = 2.5\text{ V}, I_D = 2\text{ A}$	–	0.07	0.082	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	10	–	–	A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.2\text{ A}$	–	13	–	S

## DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	–	300	–	$\text{pF}$
$C_{oss}$	Output Capacitance		–	145	–	
$C_{riss}$	Reverse Transfer Capacitance		–	35	–	

## SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 5\text{ V}, I_D = 1\text{ A}$ , $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	–	4	10	ns
$t_r$	Turn–On Rise Time		–	10	18	
$t_{d(off)}$	Turn–Off Delay Time		–	17	28	
$t_f$	Turn–Off Fall Time		–	4	10	
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 2.2\text{ A}$ , $V_{GS} = 4.5\text{ V}$	–	7	9	nC
$Q_{gs}$	Gate–Source Charge		–	1.1	–	
$Q_{gd}$	Gate–Drain Charge		–	1.9	–	

## DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain–Source Diode Forward Current	–	–	0.42	A	
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note 2)	–	0.65	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTE:

- $R_{\theta JA}$  is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design. Typical  $R_{\theta JA}$  using the board layouts shown below on FR–4 PCB in a still air environment:



a)  $250^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz. copper.



b)  $270^\circ\text{C/W}$  when mounted on a  $0.001\text{ in}^2$  pad of 2 oz. copper.

Scale 1:1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

TYPICAL CHARACTERISTICS

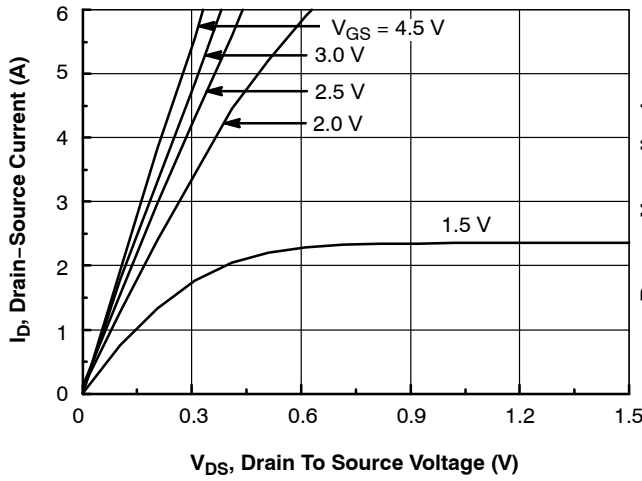


Figure 1. On-Region Characteristics

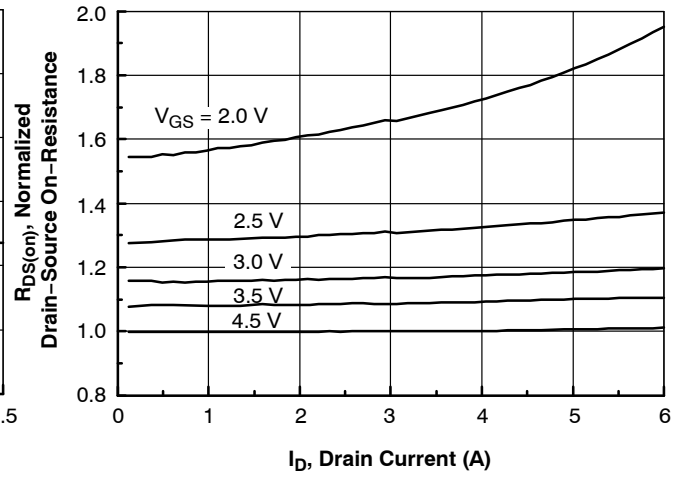


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

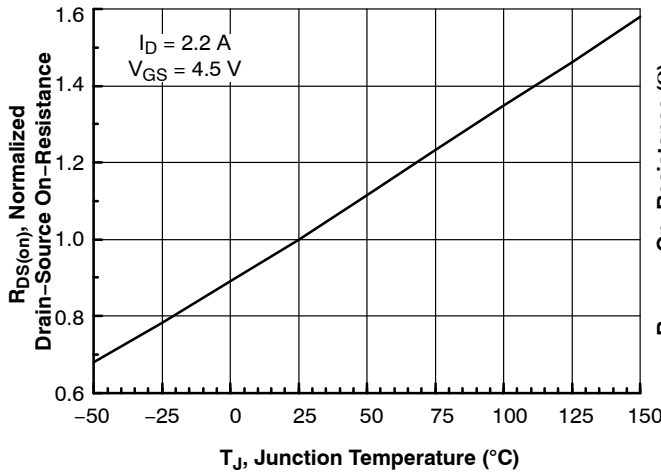


Figure 3. On-Resistance Variation with Temperature

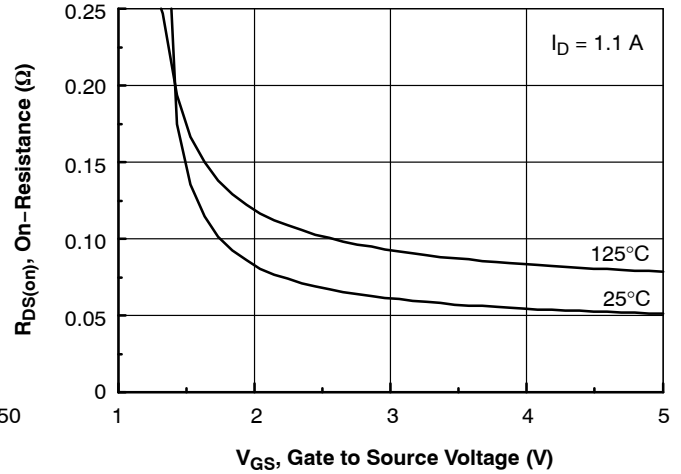


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

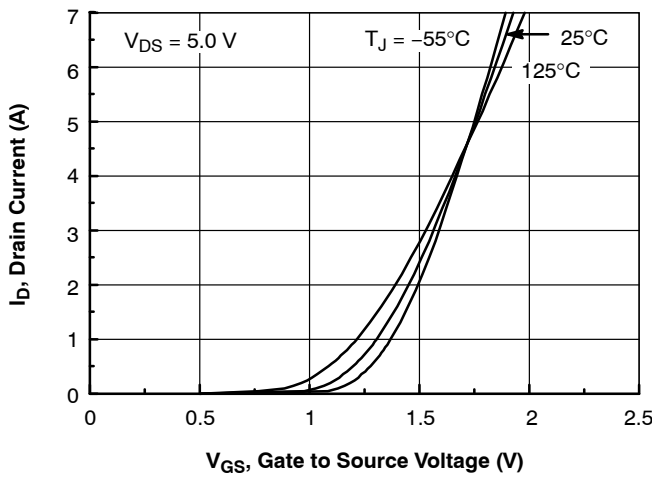


Figure 5. Transfer Characteristics

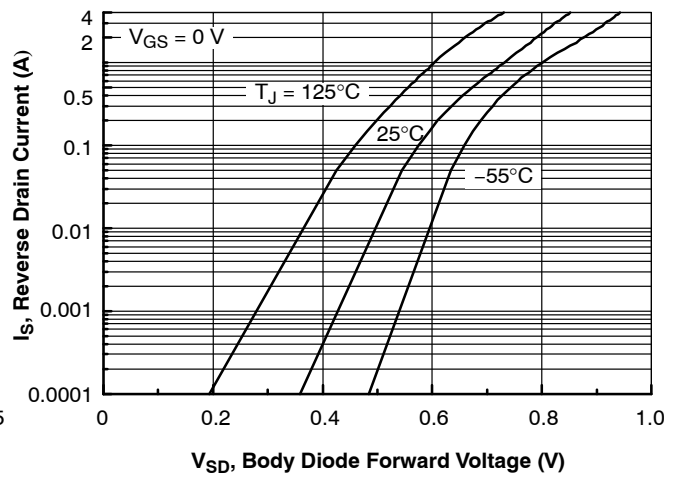


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

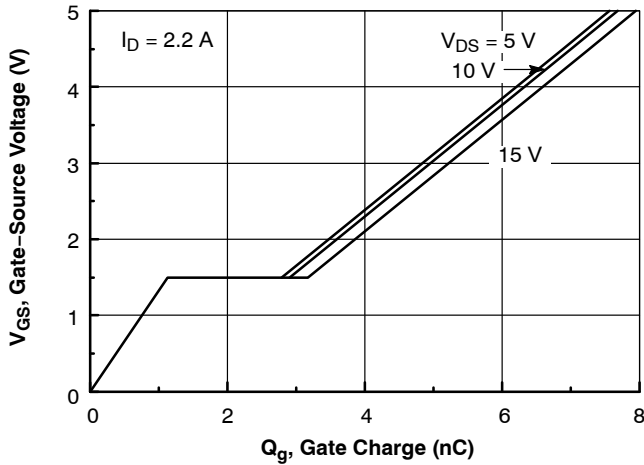


Figure 7. Gate Charge Characteristics

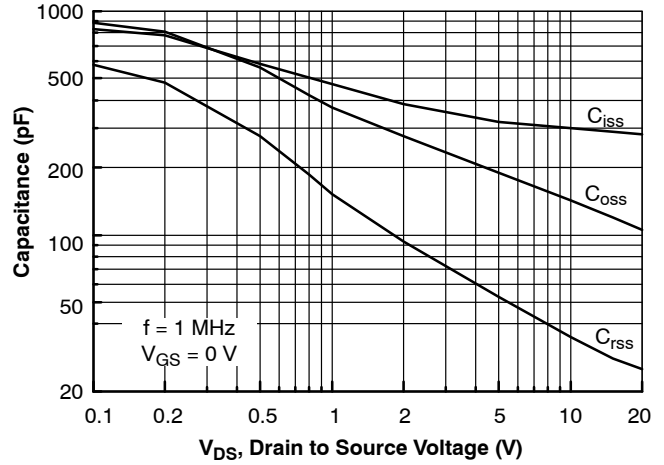


Figure 8. Capacitance Characteristics

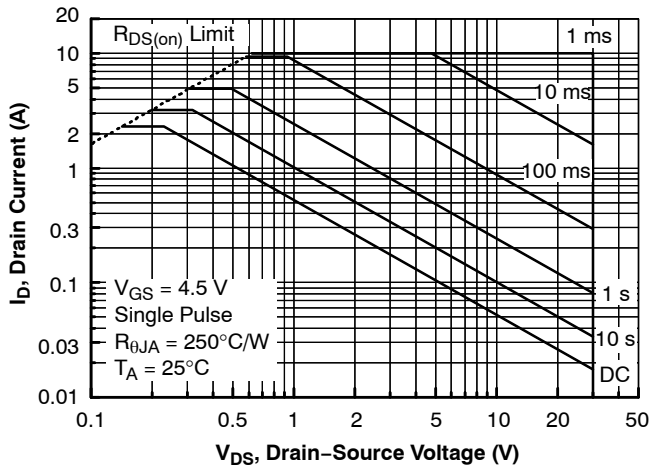


Figure 9. Maximum Safe Operating Area

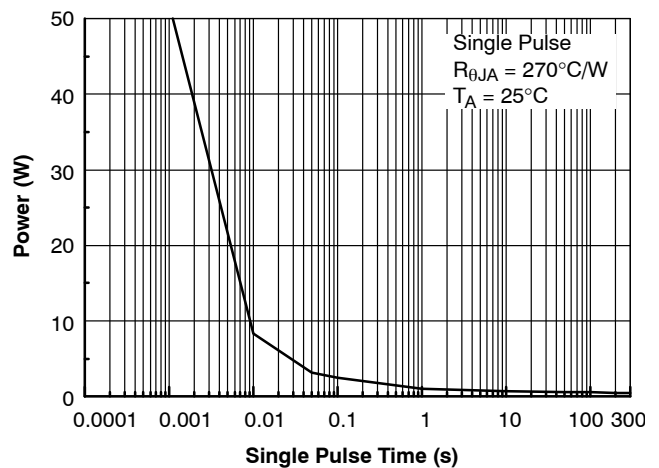


Figure 10. Single Pulse Maximum Power Dissipation

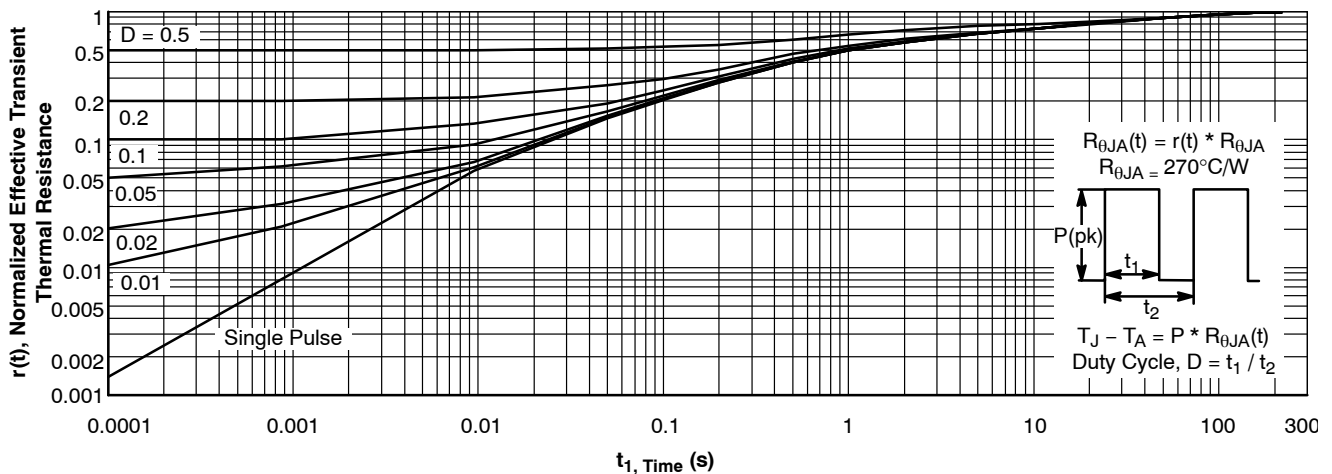


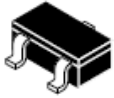
Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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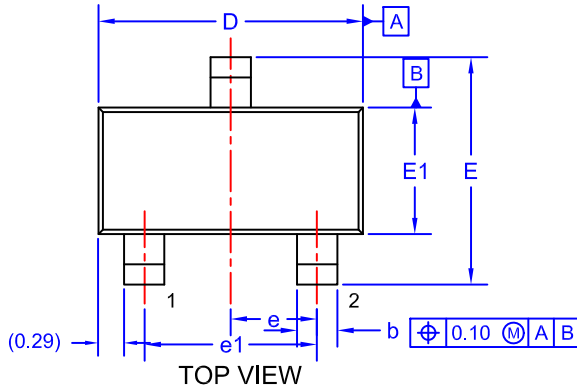
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



SOT-23/SUPERSOT™ -23, 3 LEAD, 1.4x2.9  
 CASE 527AG  
 ISSUE A

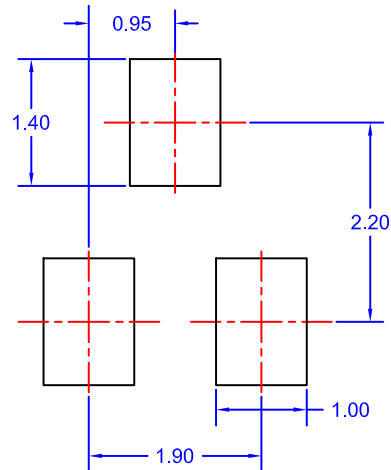
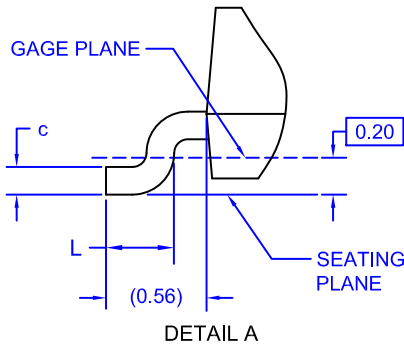
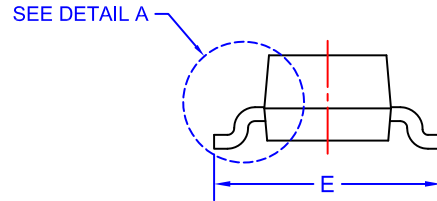
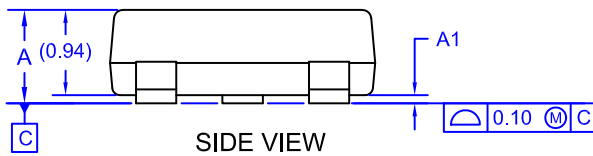
DATE 09 DEC 2019



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

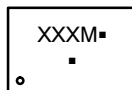
DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43



### LAND PATTERN RECOMMENDATION\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Month Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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