

MOSFET – Single, P-Channel, POWERTRENCH®

FDN352AP

General Description

This P-Channel Logic Level MOSFET is produced using onsemi advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss is needed in a very small outline surface mount package.

Features

- -1.3 A, -30 V $R_{DS(ON)} = 180 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$
- -1.1 A, -30 V $R_{DS(ON)} = 300 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power Version of Industry Standard SOT-23 Package. Identical Pin-out to SOT-23 with 30% Higher Power Handling Capability
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Notebook Computer Power Management

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain–Source Voltage		–30	V
V _{GSS}	Gate–Source Voltage		±25	V
I _D	Drain Current	Continuous (Note 1a)	–1.3	A
		Pulsed	–10	
P _D	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		–55 to 150	°C

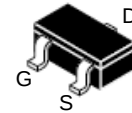
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	

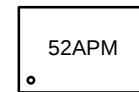
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
 - a. $R_{\theta JA} = 250^\circ\text{C/W}$ when mounted on a 0.02 in² pad of 2 oz. copper.
 - b. $R_{\theta JA} = 270^\circ\text{C/W}$ when mounted on a 0.001 in² pad of 2 oz. copper.

V_{DS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-30 V	180 m Ω @ -10 V	-1.3 A
	300 m Ω @ -4.5 V	-1.1 A



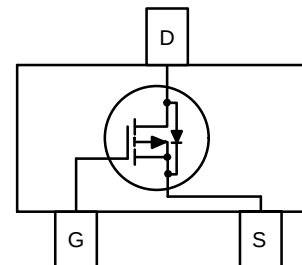
SOT-23/SUPERSOT™ -23, 3 LEAD, 1.4x2.9
CASE 527AG

MARKING DIAGRAM



52AP = Specific Device Code
M = Date Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDN352AP

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C	-	-17	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate-Body Leakage	V _{GS} = ±25 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-0.8	-2.0	-2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C	-	4	-	mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -1.3 A V _{GS} = -4.5 V, I _D = -1.1 A V _{GS} = -4.5 V, I _D = -1.1 A, T _J = 125°C	-	150 250 330	180 300 400	mΩ
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -0.9 A	-	2.0	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz	-	150	-	pF
C _{oss}	Output Capacitance		-	40	-	pF
C _{rss}	Reverse Transfer Capacitance		-	20	-	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn-On Delay Time	V _{DD} = -10 V, I _D = -1 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	-	4	8	ns
t _r	Turn-On Rise Time		-	15	28	ns
t _{d(off)}	Turn-Off Delay Time		-	10	18	ns
t _f	Turn-Off Fall Time		-	1	2	ns
Q _g	Total Gate Charge	V _{DS} = -10 V, I _D = -0.9 A, V _{GS} = -4.5 V	-	1.4	1.9	nC
Q _{gs}	Gate-Source Charge		-	0.5	-	nC
Q _{gd}	Gate-Drain Charge		-	0.5	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	-0.42	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -0.42 A (Note 2)	-	-0.8	-1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = -3.9 A, dI _F /dt = 100 A/μs	-	17	-	ns
Q _{rr}	Diode Reverse Recovery Charge		-	7	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 Ms, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

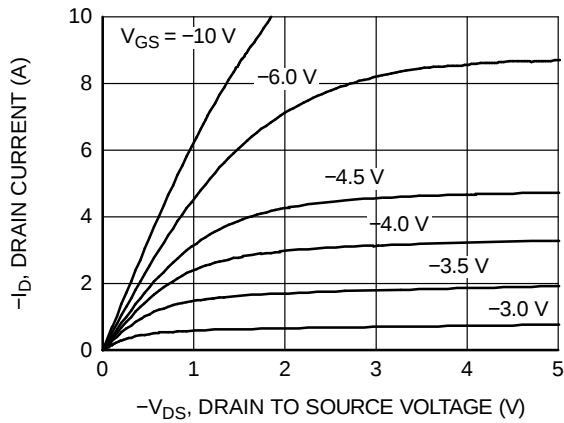


Figure 1. On-Region Characteristics

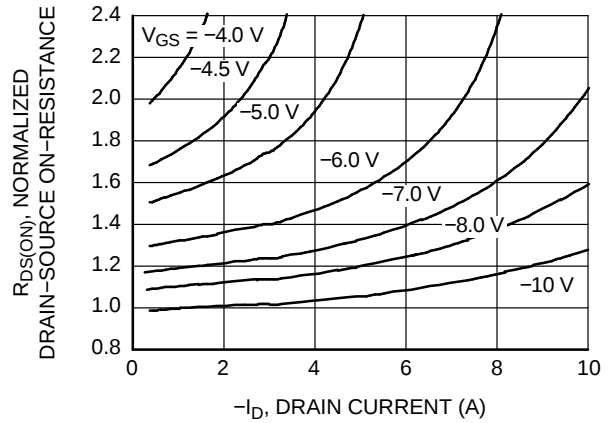


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

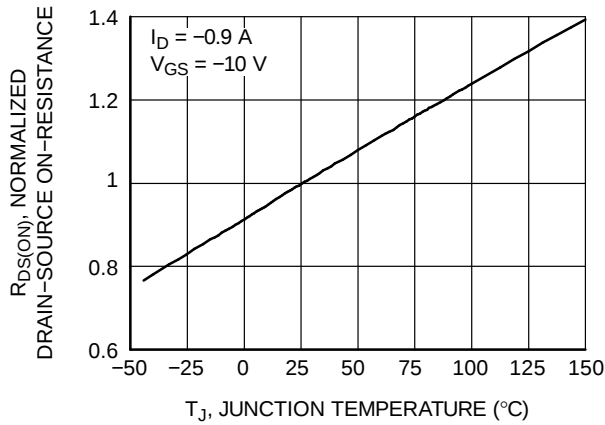


Figure 3. On-Resistance Variation with Temperature

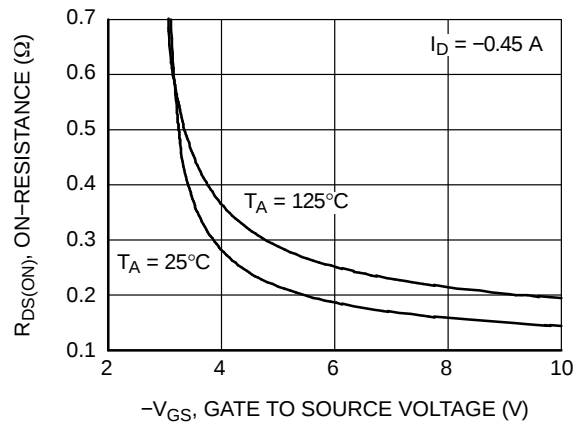


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

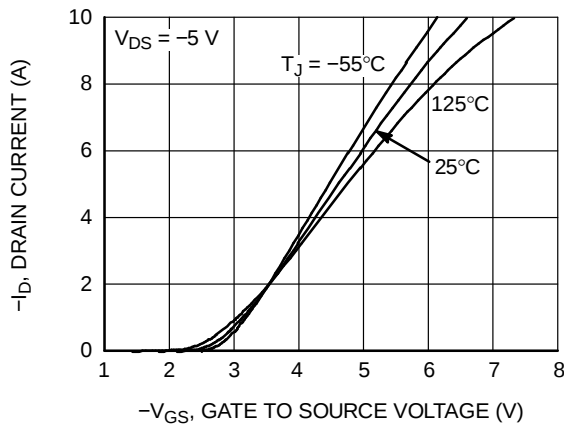


Figure 5. Transfer Characteristics

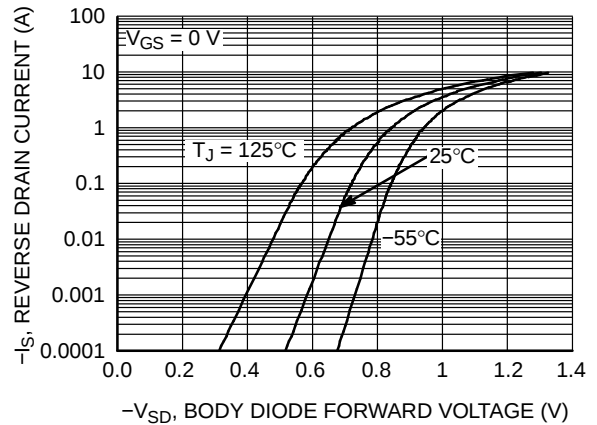


Figure 6. Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

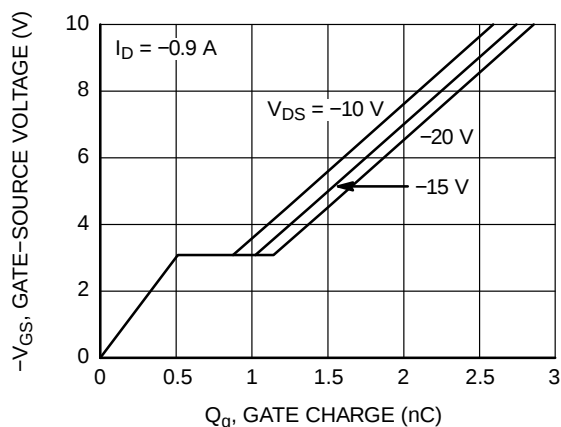


Figure 7. Gate Charge Characteristics

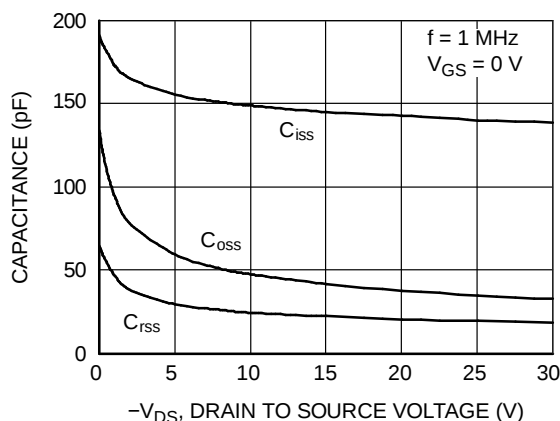


Figure 8. Capacitance Characteristics

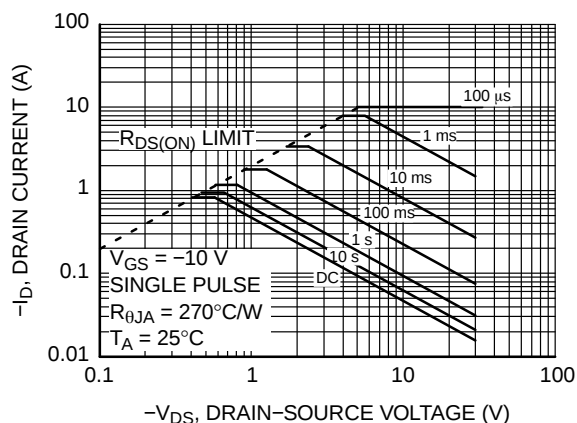


Figure 9. Maximum Safe Operating Area

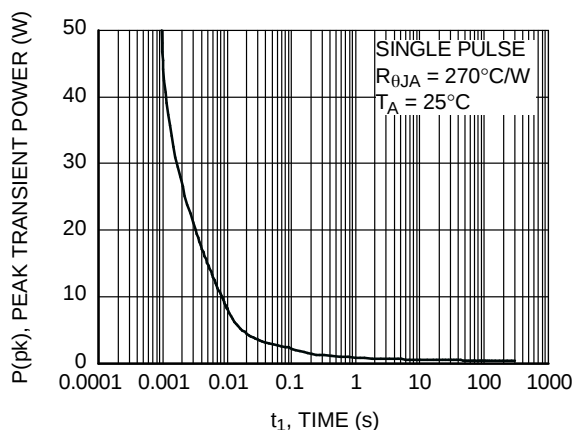


Figure 10. Single Pulse Maximum Power Dissipation

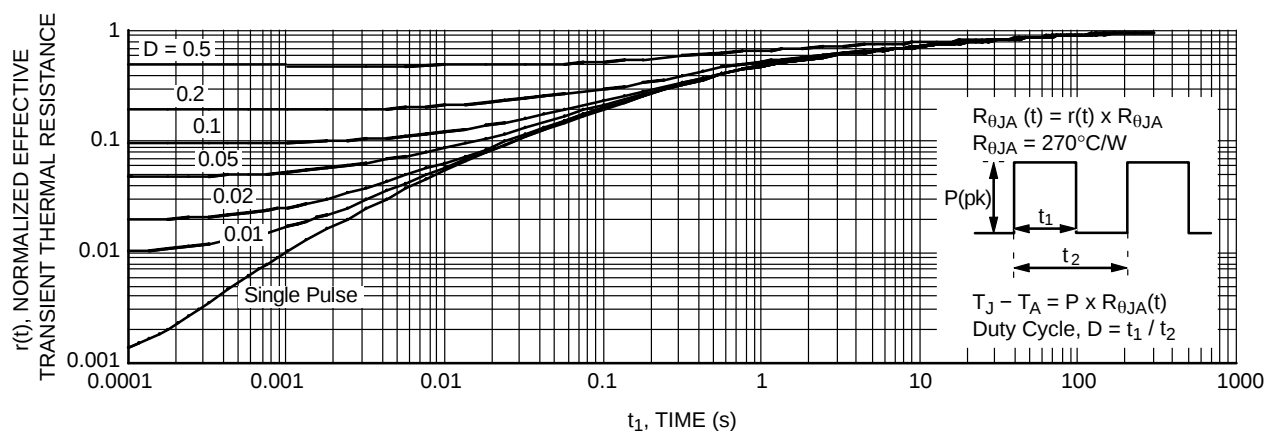


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

FDN352AP

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDN352AP	52AP	SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9 (Pb-Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

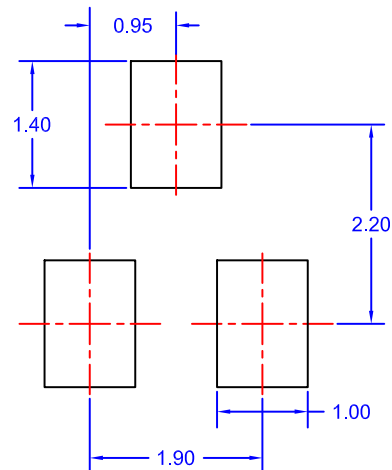
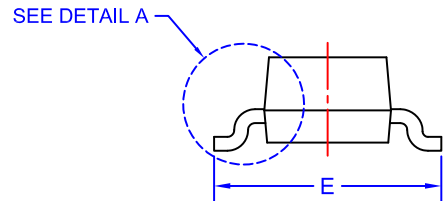
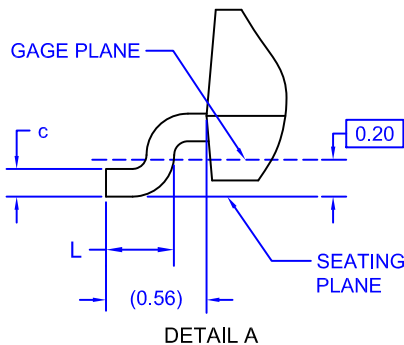
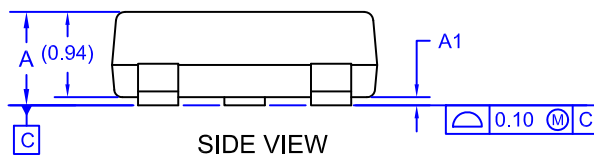
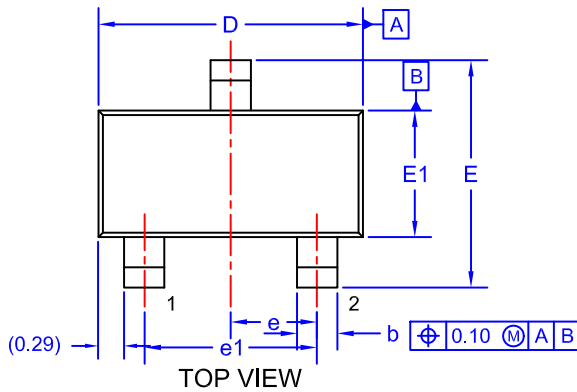
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9 CASE 527AG ISSUE A

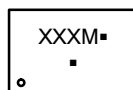
DATE 09 DEC 2019



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-23/SUPERSOT-23, 3 LEAD, 1.4X2.9	PAGE 1 OF 1

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