

# FDP16AN08A0

## N-Channel PowerTrench® MOSFET

75 V, 58 A, 16 mΩ

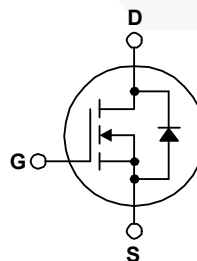
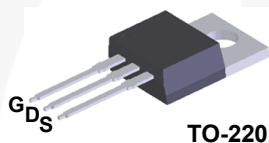
### Features

- $R_{DS(on)} = 13 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 58 \text{ A}$
- $Q_{G(tot)} = 28 \text{ nC}$  (Typ.) @  $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

Formerly developmental type 82660



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP16AN08A0	Unit
$V_{DSS}$	Drain to Source Voltage	75	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	58	A
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	44	
	Continuous ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , with $R_{\theta JA} = 43^\circ\text{C/W}$ )	9	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	117	mJ
$P_D$	Power dissipation	135	W
	Derate above $25^\circ\text{C}$	0.9	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case, Max.	1.11	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2), Max.	62	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP16AN08A0	FDP16AN08A0	TO-220	Tube	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	75	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 58\text{A}, V_{GS} = 10\text{V}$	-	0.013	0.016	$\Omega$
		$I_D = 29\text{A}, V_{GS} = 6\text{V}$	-	0.019	0.029	
		$I_D = 58\text{A}, V_{GS} = 10\text{V},$ $T_J = 175^\circ\text{C}$	-	0.032	0.037	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	1857	-	pF	
$C_{OSS}$	Output Capacitance		-	288	-	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	88	-	pF	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 40\text{V}$ $I_D = 58\text{A}$ $I_g = 1.0\text{mA}$	-	28	42	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 2\text{V}$		-	3.5	5	nC
$Q_{gs}$	Gate to Source Gate Charge			-	11	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau			-	7.6	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	6.4	-	nC

### Switching Characteristics ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 40\text{V}, I_D = 58\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 10\Omega$	-	-	135	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
$t_r$	Rise Time		-	82	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	28	-	ns
$t_f$	Fall Time		-	30	-	ns
$t_{OFF}$	Turn-Off Time		-	-	86	ns

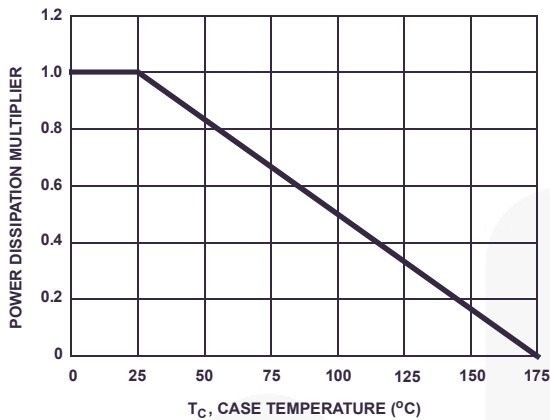
### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 58\text{A}$	-	-	1.25	V
		$I_{SD} = 29\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 58\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	35	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 58\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	36	nC

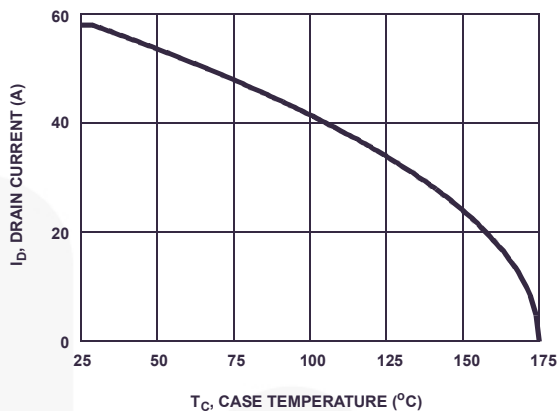
#### Notes:

1: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 260\mu\text{H}$ ,  $I_{AS} = 30\text{A}$ .

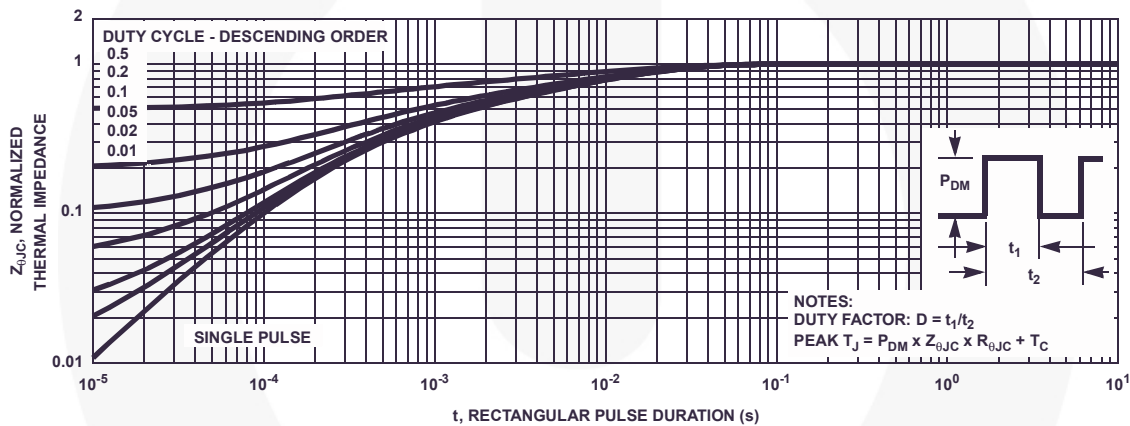
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



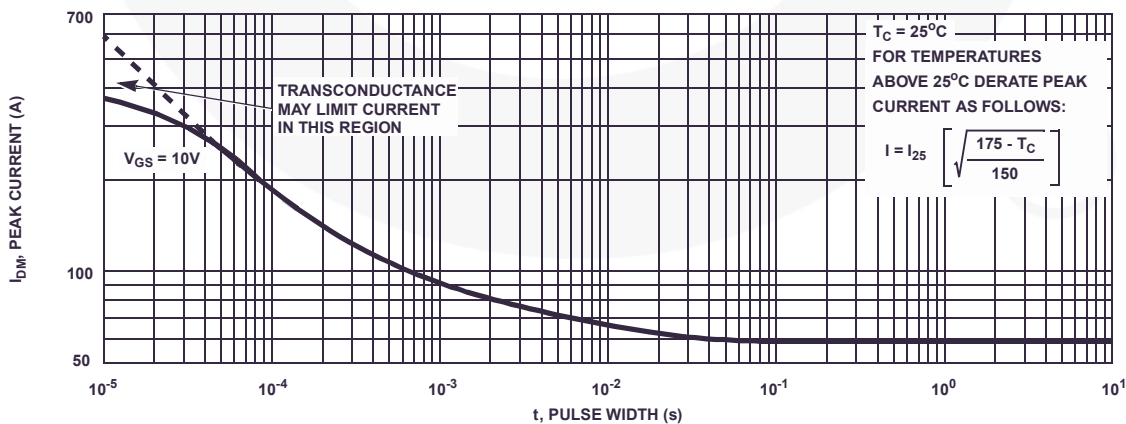
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

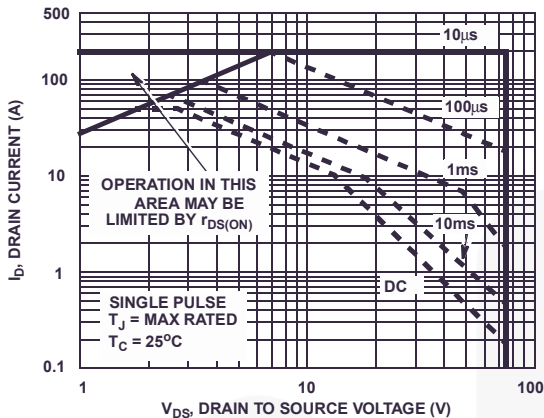


**Figure 3. Normalized Maximum Transient Thermal Impedance**

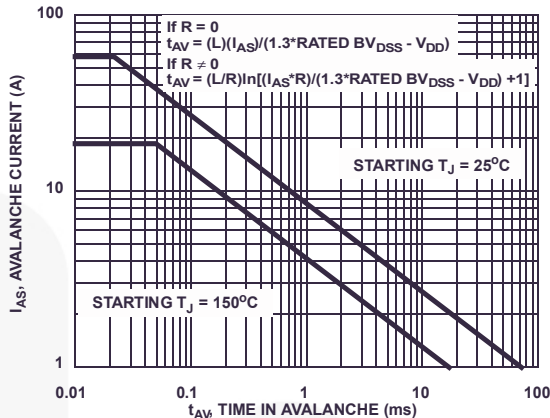


**Figure 4. Peak Current Capability**

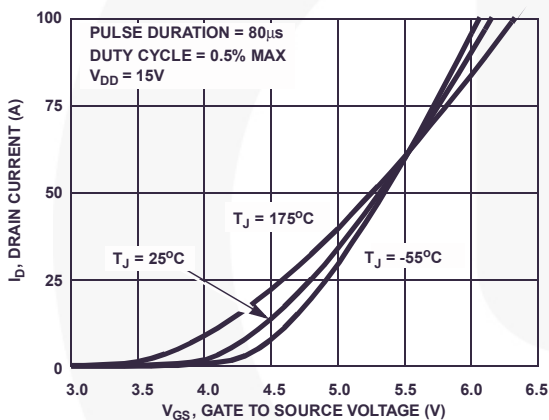
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



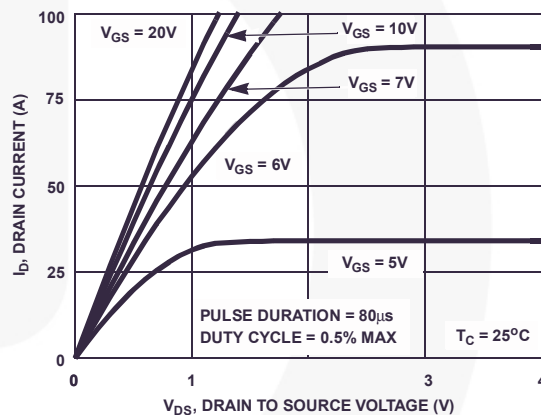
**Figure 5. Forward Bias Safe Operating Area**



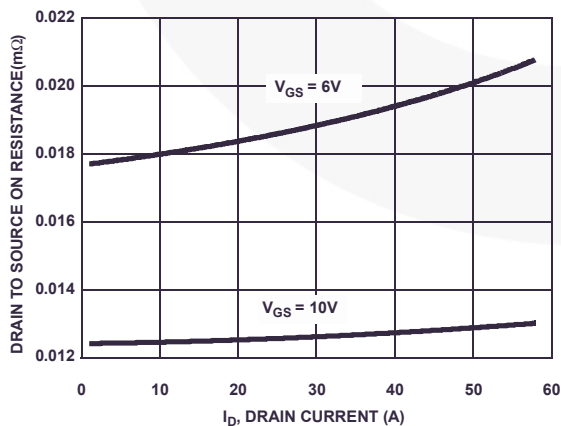
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
**Figure 6. Unclamped Inductive Switching Capability**



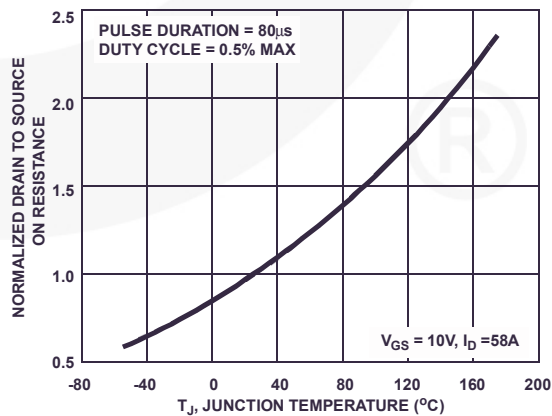
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

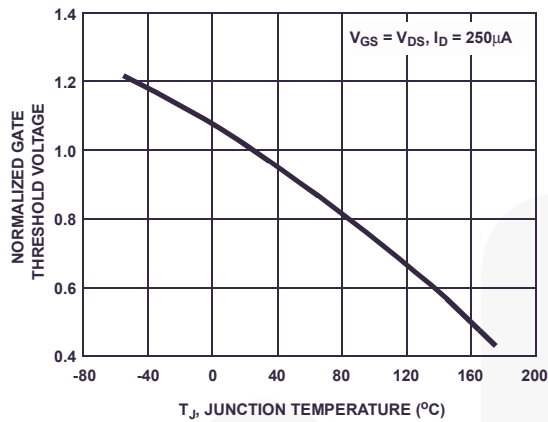


**Figure 9. Drain to Source On Resistance vs Drain Current**

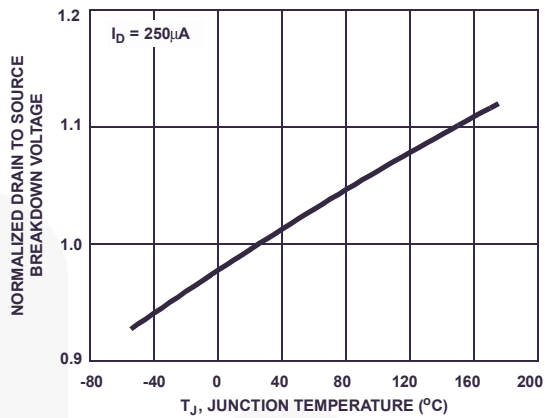


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

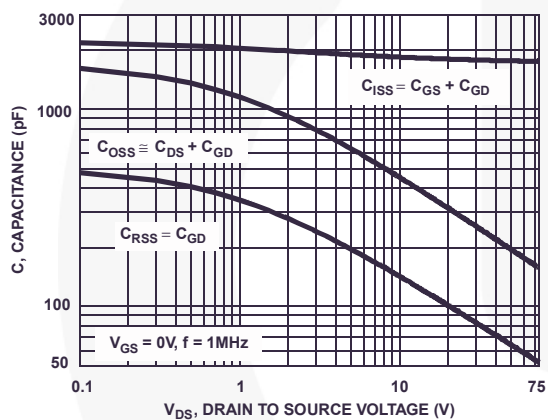
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



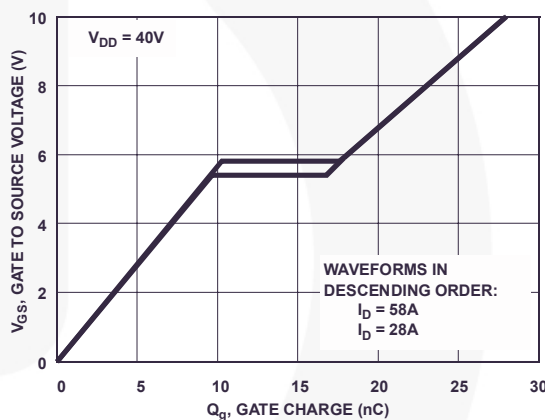
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Current**

### Test Circuits and Waveforms

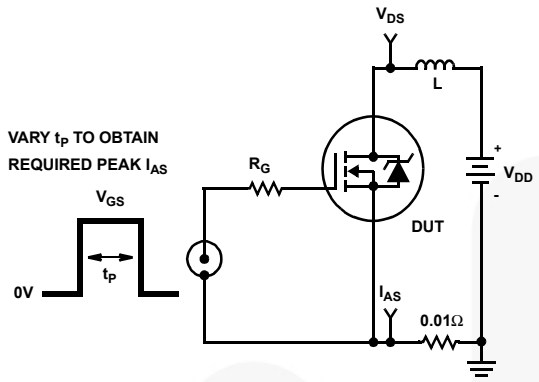


Figure 15. Unclamped Energy Test Circuit

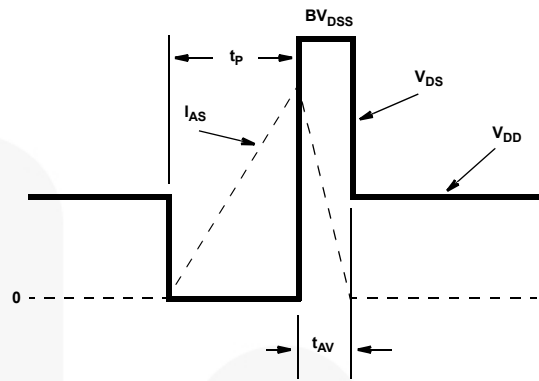


Figure 16. Unclamped Energy Waveforms

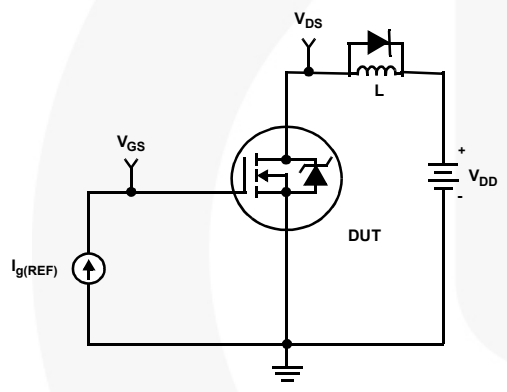


Figure 17. Gate Charge Test Circuit

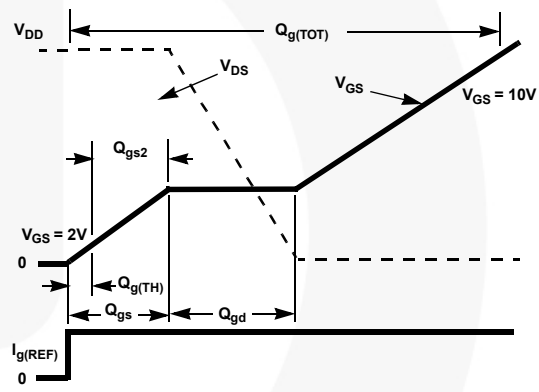


Figure 18. Gate Charge Waveforms

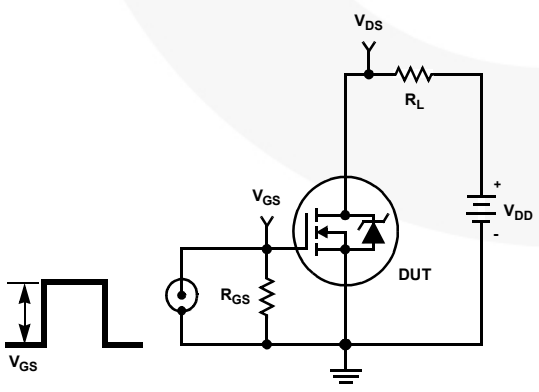


Figure 19. Switching Time Test Circuit

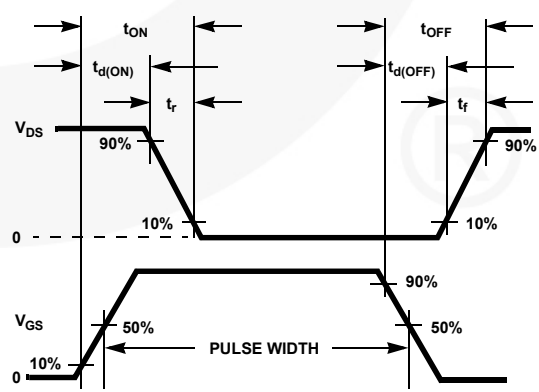


Figure 20. Switching Time Waveforms

### PSPICE Electrical Model

.SUBCKT FDB16AN08A0 2 1 3 ; rev March 2002  
 Ca 12 8 10e-10  
 Cb 15 14 8e-10  
 Cin 6 8 1.7e-9

Dbody 7 5 DbodyMOD  
 Dbreak 5 11 DbreakMOD  
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 85.40  
 Eds 14 8 5 8 1  
 Egs 13 8 6 8 1  
 Esg 6 10 6 8 1  
 Evthres 6 21 19 8 1  
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.96e-9  
 Ldrain 2 5 1.0e-9  
 Lsource 3 7 5.75e-9

RLgate 1 9 59.6  
 RLdrain 2 5 10  
 RLsource 3 7 57.5

Mmed 16 6 8 8 MmedMOD  
 Mstro 16 6 8 8 MstroMOD  
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
 Rdrain 50 16 RdrainMOD 3.3e-3  
 Rgate 9 20 3.31  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 Rsource 8 7 RsourceMOD 7e-3  
 Rvthres 22 8 RvthresMOD 1  
 Rvtemp 18 19 RvtempMOD 1  
 S1a 6 12 13 8 S1AMOD  
 S1b 13 12 13 8 S1BMOD  
 S2a 6 15 14 13 S2AMOD  
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={V(5,51)/ABS(V(5,51))}\*(PWR(V(5,51))/(1e-6\*200),3))

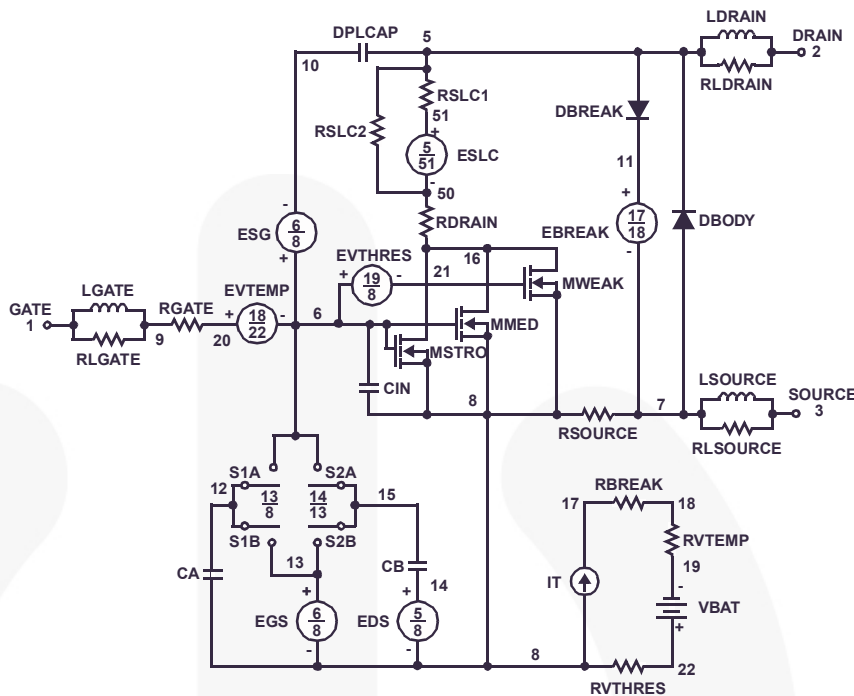
```
.MODEL DbodyMOD D (IS=2.4E-11 N=1.08 RS=3.3e-3 TRS1=2.2e-3 TRS2=2.5e-9
+ CJO=1.2e-9 M=5.6e-1 TT=1.3e-8 XTI=3.9)
.MODEL DbreakMOD D (RS=1.5e-1 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=5e-10 IS=1e-30 N=10 M=0.52)

.MODEL MmedMOD NMOS (VTO=3.2 KP=4 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.31)
.MODEL MstroMOD NMOS (VTO=3.85 KP=70 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=2.7 KP=0.06 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.31e+1 RS=0.1)

.MODEL RbreakMOD RES (TC1=9e-4 TC2=-5e-7)
.MODEL RdrainMOD RES (TC1=1.9e-2 TC2=4e-5)
.MODEL RSLCMOD RES (TC1=1.5e-3 TC2=3e-5)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-5.3e-3 TC2=-1.3e-5)
.MODEL RvtempMOD RES (TC1=-2.7e-3 TC2=1e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=-5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=.5 VOFF=-1)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



### SABER Electrical Model

rev March 2002  
 template FDB16AN08A0 n2,n1,n3  
 electrical n2,n1,n3

```
{
var i iscl
dp..model dbodymod = (isl=2.4e-11,nl=1.08,rs=3.3e-3,trs1=2.2e-3,trs2=2.5e-9,cjo=1.2e-9,m=5.6e-1,tt=1.3e-8,xti=3.9)
dp..model dbreakmod = (rs=1.5e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=5e-10,isl=10e-30,nl=10,m=0.52)
m..model mmedmod = (type=_n,vto=3.2,kp=4,is=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=3.85,kp=70,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=2.7,kp=0.06,is=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-1.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1,voff=-5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=.5,voff=-1)
c.ca n12 n8 = 10e-10
c.cb n15 n14 = 8e-10
c.cin n6 n8 = 1.7e-9
```

```
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
```

```
spe.ebreak n11 n7 n17 n18 = 85.40
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
```

```
i.it n8 n17 = 1
```

```
l.lgate n1 n9 = 5.96e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 5.75e-9
```

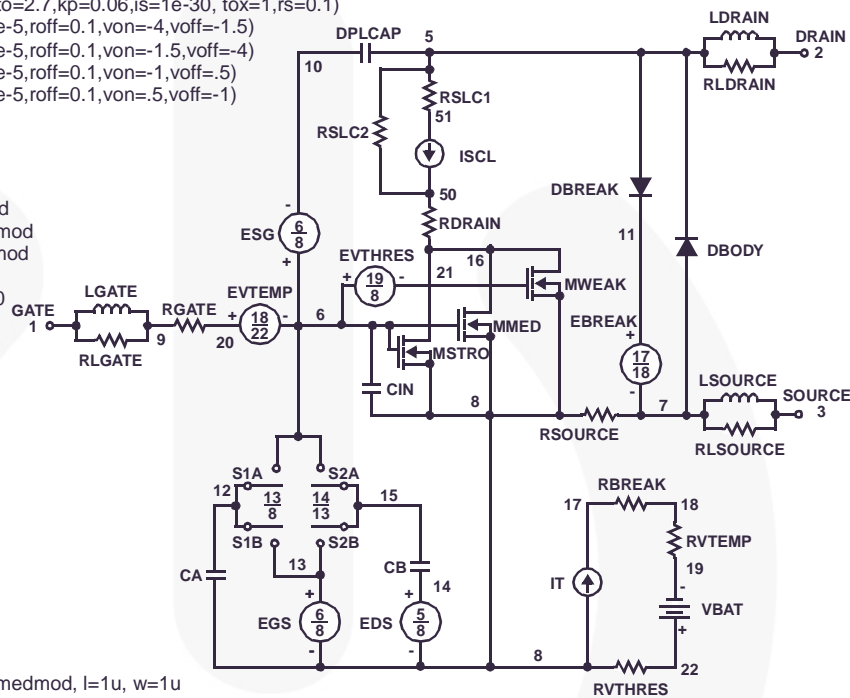
```
res.rlgate n1 n9 = 59.6
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 57.5
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

```
res.rbreak n17 n18 = 1, tc1=9e-4,tc2=-5e-7
res.rdrain n50 n16 = 3.3e-3, tc1=1.9e-2,tc2=4e-5
res.rgate n9 n20 = 3.31
res.rslc1 n5 n51 = 1e-6, tc1=1.5e-3,tc2=3e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 7e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-5.3e-3,tc2=-1.3e-5
res.rvtemp n18 n19 = 1, tc1=-2.7e-3,tc2=1e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/200)** 3)
}
}
```





### SPICE Thermal Model

REV 23 March 2002

FDB16AN08A0T

```

CTHERM1 th 6 0.002
CTHERM2 6 5 0.004
CTHERM3 5 4 0.006
CTHERM4 4 3 0.01
CTHERM5 3 2 0.03
CTHERM6 2 tl 0.08
    
```

```

R THERM1 th 6 0.075
R THERM2 6 5 0.09
R THERM3 5 4 0.1
R THERM4 4 3 0.15
R THERM5 3 2 0.2
R THERM6 2 tl 0.25
    
```

### SABER Thermal Model

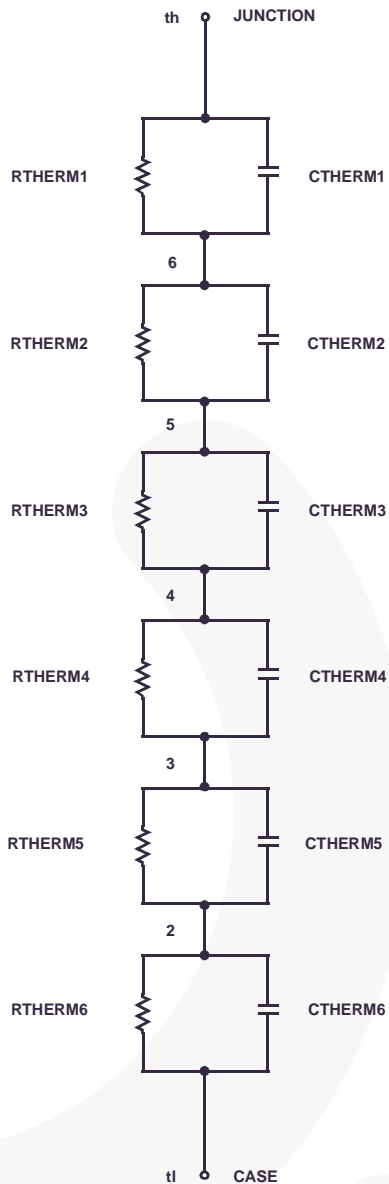
SABER thermal model FDD16AN08A0T  
 template thermal\_model th tl  
 thermal\_c th, tl

```

{
ctherm.ctherm1 th 6 = 0.002
ctherm.ctherm2 6 5 = 0.004
ctherm.ctherm3 5 4 = 0.006
ctherm.ctherm4 4 3 = 0.01
ctherm.ctherm5 3 2 = 0.03
ctherm.ctherm6 2 tl = 0.08
    
```

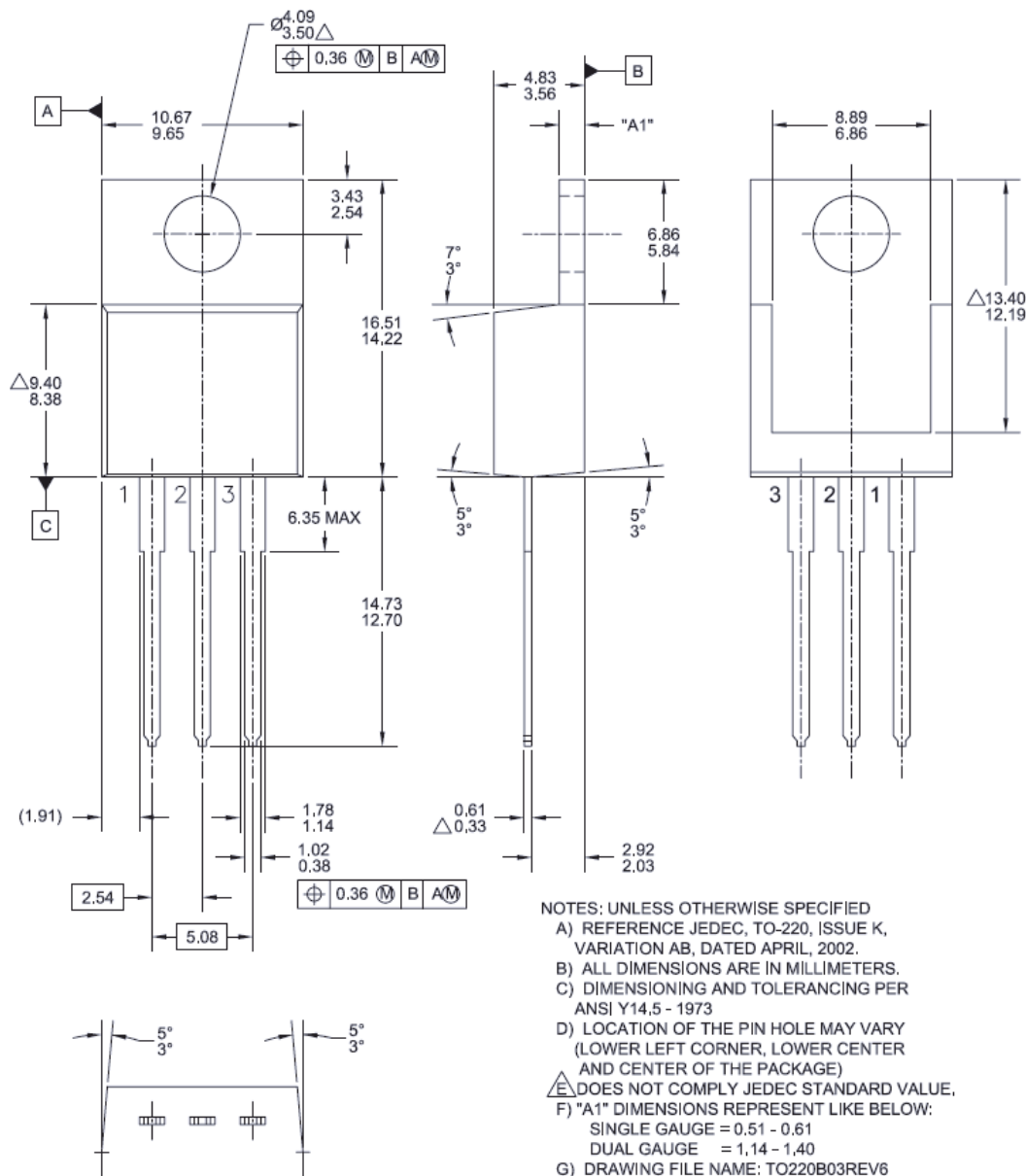
```

rtherm.rtherm1 th 6 = 0.075
rtherm.rtherm2 6 5 = 0.09
rtherm.rtherm3 5 4 = 0.1
rtherm.rtherm4 4 3 = 0.15
rtherm.rtherm5 3 2 = 0.2
rtherm.rtherm6 2 tl = 0.25
}
    
```



## Mechanical Dimensions

### TO-220 3L



**Figure 21. TO-220, Molded, 3Lead, Jedec Variation AB**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT220-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT220-003)

Dimension in Millimeters



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| AX-CAP®*                 | FRFET®                  | PowerXS™  | SYSTEM GENERAL®* |
| BitSiC™                  | Global Power ResourceSM | Programmable Active Droop™                      | TinyBoost®       |
| Build it Now™            | GreenBridge™            | QFET®   | TinyBuck®        |
| CorePLUS™                | Green FPS™              | QS™   | TinyCalc™        |
| CorePOWER™               | Green FPS™ e-Series™    | Quiet Series™                                   | TinyLogic®       |
| CROSSVOLT™               | Gmax™                   | RapidConfigure™                                 | TINYOPTO™        |
| CTL™                     | GTO™                    | ISOPLANAR™                                      | TinyPower™       |
| Current Transfer Logic™  | IntelliMAX™             | Marking Small Speakers Sound Louder and Better™ | TinyPWM™         |
| DEUXPEED®                | ISOPLANAR™              | MegaBuck™                                       | TinyWire™        |
| Dual Cool™               | MICROCOUPLER™           | MicroFET™                                       | TranSiC™         |
| EcoSPARK®                | MicroPak™               | MillerDrive™                                    | TriFault Detect™ |
| EfficientMax™            | MicroPak2™              | MotionMax™                                      | TRUECURRENT®*    |
| ESBC™                    | FAST™                   | mWSaver®  | µSerDes™         |
| <b>F</b> ®               | FastvCore™              | OPTOLOGIC®                                      | <b>U</b> SerDes™ |
| Fairchild®               | FETBench™               | OPTOPLANAR®                                     | UHC®             |
| Fairchild Semiconductor® | FPS™                    | PowerTrench®                                    | Ultra FRFET™     |
| FACT Quiet Series™       |                         | PowerXS™  | UniFET™          |
| FACT®                    |                         | Programmable Active Droop™                      | VCX™             |
| FAST®                    |                         | QFET®   | VisualMax™       |
| FastvCore™               |                         | QS™   | VoltagePlus™     |
| FETBench™                |                         | Quiet Series™                                   | XS™              |
| FPS™                     |                         | RapidConfigure™                                 |                  |

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**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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