FAIRCHILD SEMICONDUCTOR®

November 2013

# FDP5N60NZ / FDPF5N60NZ

## N-Channel UniFET™ II MOSFET

**600 V, 4.5 A, 2.0 Ω**

## Features

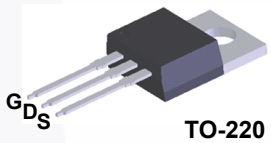
- $R_{DS(on)}$ = 1.65 Ω (Typ.) @ $V_{GS}$ = 10 V, $I_D$ = 2.25 A
- Low Gate Charge (Typ. 10 nC)
- Low $C_{rss}$ (Typ. 5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

## Applications

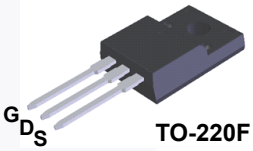
- LCD / LED / PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

## Description

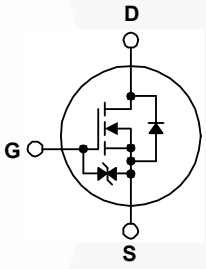
UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.




TO-220




TO-220F




## MOSFET Maximum Ratings $T_C$ = 25°C unless otherwise noted.

| Symbol | Parameter | | FDP5N60NZ | FDPF5N60NZ | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | 600 | | V |
| $V_{GSS}$ | Gate to Source Voltage | | ±25 | | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C) | 4.5 | 4.5* | A |
| | | - Continuous ($T_C$ = 100°C) | 2.7 | 2.7* | |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | 18 | 18* | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 175 | | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 4.5 | | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 10 | | mJ |
| dv/dt | MOSFET dv/dt | | 20 | | V/ns |
| | Peak Diode Recovery dv/dt | (Note 3) | 10 | | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | 100 | 33 | W |
| | | - Derate above 25°C | 0.8 | 0.27 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | | °C |
| $T_L$ | Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds | | 300 | | °C |

*Dran current limited by maximum junction temperature

## Thermal Characteristics

| Symbol | Parameter | FDP5N60NZ | FDPF5N60NZ | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | 1.25 | 3.75 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max. | 62.5 | 62.5 | |

## Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|---|
| FDP5N60NZ | FDP5N60NZ | TO-220 | Tube | N/A | N/A | 50 units |
| FDPF5N60NZ | FDPF5N60NZ | TO-220F | Tube | N/A | N/A | 50 units |

## Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 600 | - | - | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | - | 0.6 | - | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 480 V, $T_C$ = 125°C | - | - | 10 | |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±25 V, $V_{DS}$ = 0 V | - | - | ±10 | μA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 3.0 | - | 5.0 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 2.25 A | - | 1.65 | 2.0 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20 V, $I_D$ = 2.25 A | - | 5 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 450 | 600 | pF |
| $C_{oss}$ | Output Capacitance | | - | 50 | 65 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 5 | 7.5 | pF |
| $Q_g$ | Total Gate Charge at 10V | $V_{DS}$ = 480 V, $I_D$ = 4.5 A, $V_{GS}$ = 10 V (Note 4) | - | 10 | 13 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 2.5 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 4 | - | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 300 V, $I_D$ = 4.5 A, $V_{GS}$ = 10 V, $R_G$ = 25 Ω (Note 4) | - | 15 | 40 | ns |
| $t_r$ | Turn-On Rise Time | | - | 20 | 50 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 35 | 80 | ns |
| $t_f$ | Turn-Off Fall Time | | - | 20 | 50 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 4.5 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 18 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 4.5 A | - | - | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_{SD}$ = 4.5 A, $dI_F/dt$ = 100 A/μs | - | 230 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 0.9 | - | μC |

**Notes:**

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 17.3 mH, $I_{AS}$ = 4.5 A, $V_{DD}$ = 50 V, $R_G$ = 25 Ω, starting $T_J$ = 25°C.
3. $I_{SD}$ ≤ 4.5 A, di/dt ≤ 200 A/μs, $V_{DD}$ ≤ $BV_{DSS}$, starting $T_J$ = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

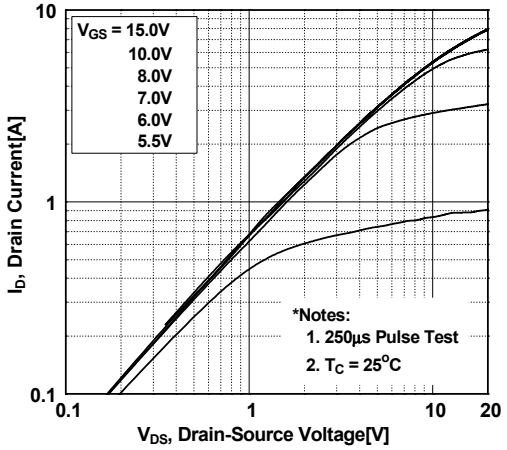



**Figure 2. Transfer Characteristics**

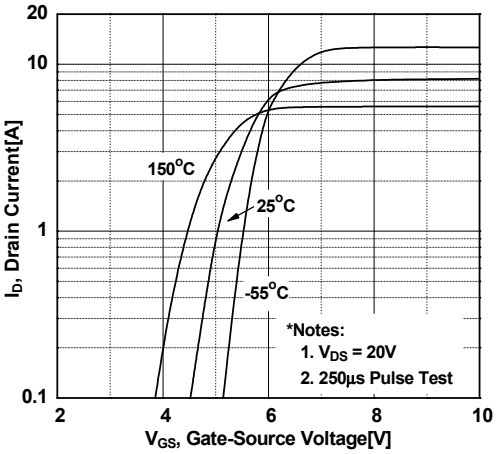



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

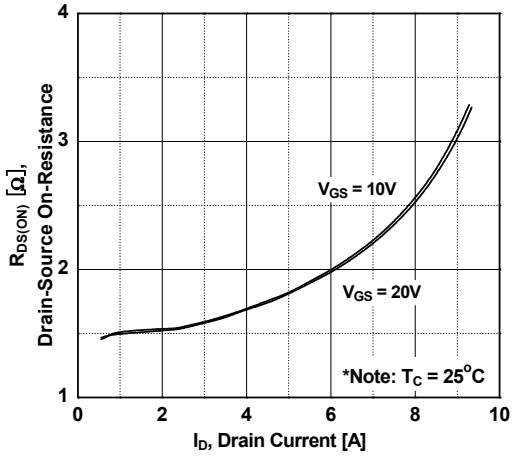



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

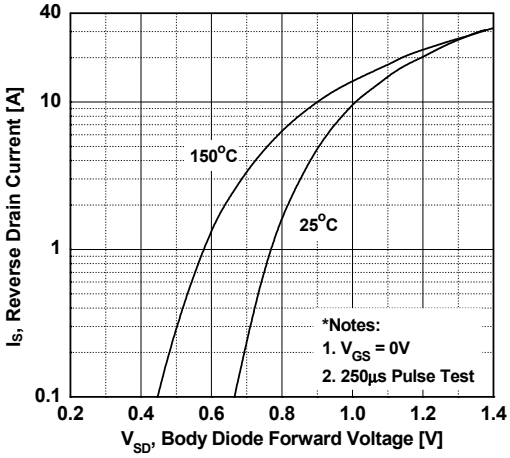



**Figure 5. Capacitance Characteristics**

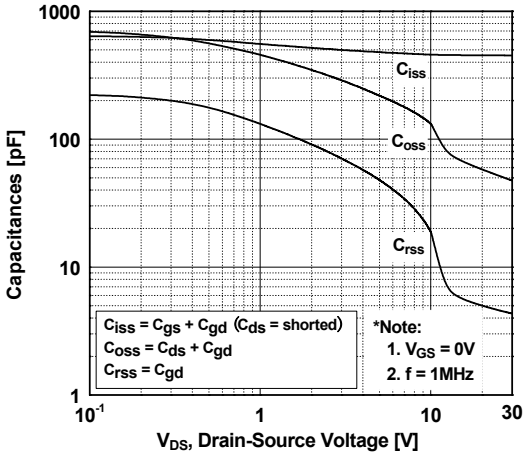
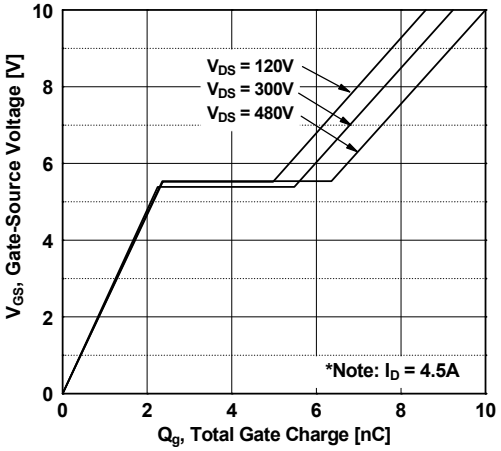



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

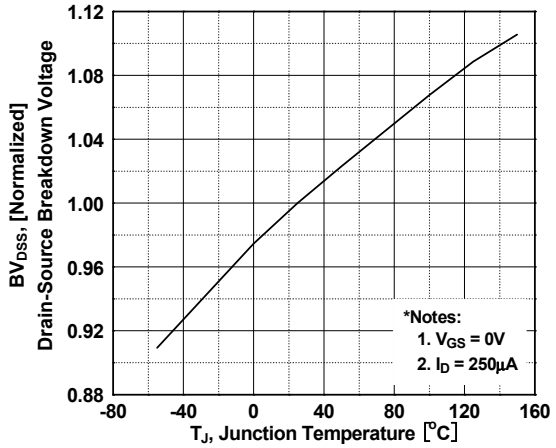



**Figure 8. On-Resistance Variation vs. Temperature**

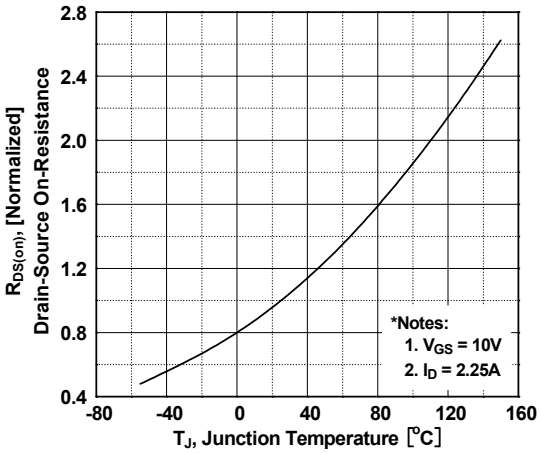



**Figure 9. Maximum Safe Operating Area - FDP5N60NZ**

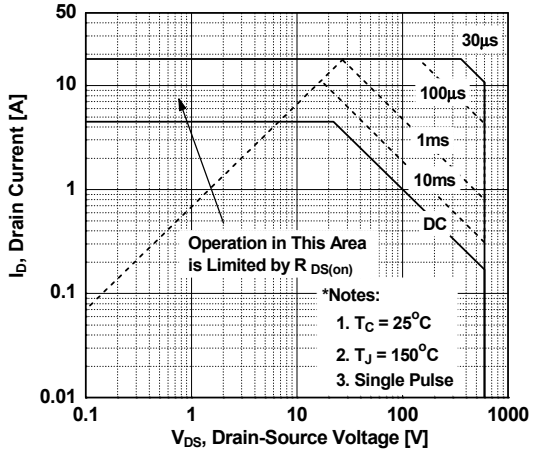



**Figure 10. Maximum Safe Operating Area - FDPF5N60NZ**

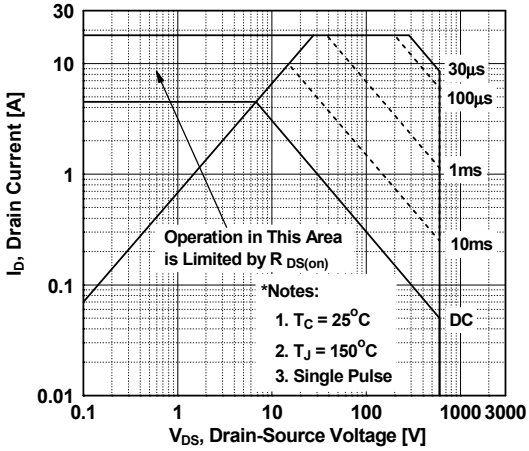



**Figure 11. Maximum Drain Current vs. Case Temperature**

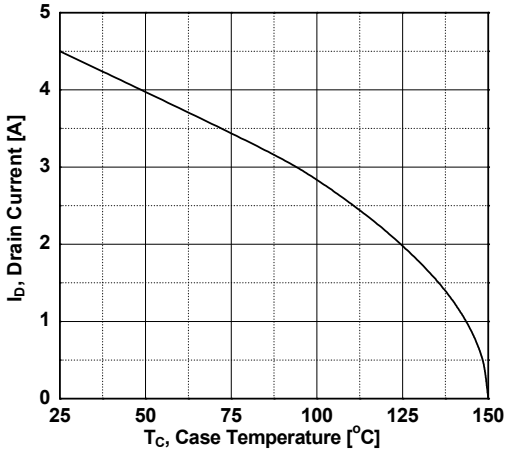
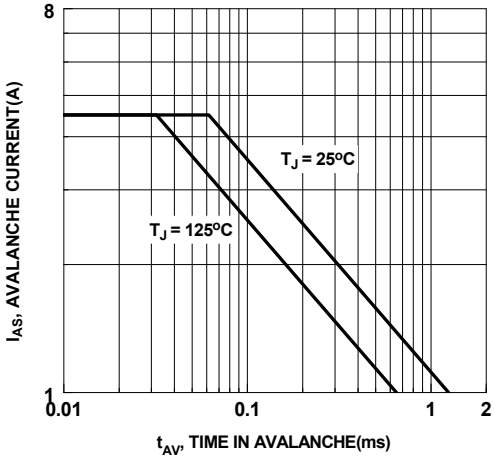



**Figure 12. Unclamped Inductive Switching Capability**



## Typical Performance Characteristics (Continued)

**Figure 13. Transient Thermal Response Curve - FDP5N60NZ**

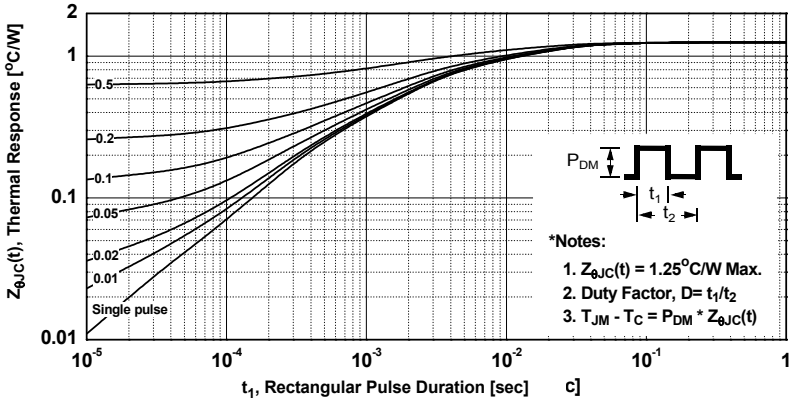
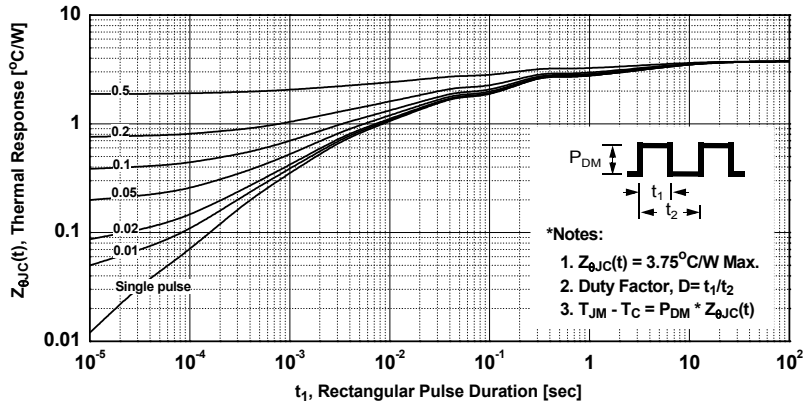



**Figure 14. Transient Thermal Response Curve - FDPF5N60NZ**



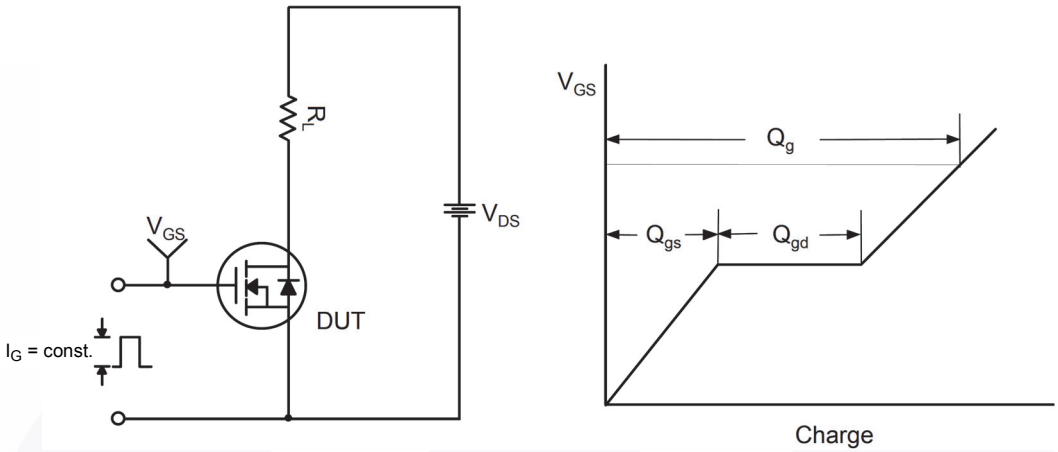



**Figure 15. Gate Charge Test Circuit & Waveform**

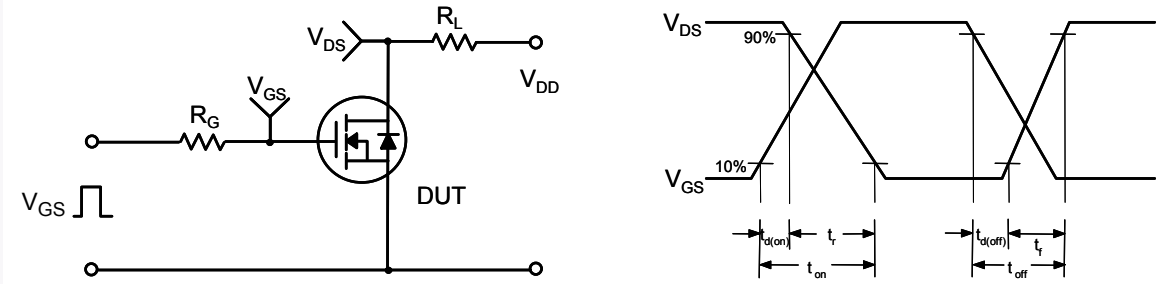



**Figure 16. Resistive Switching Test Circuit & Waveforms**

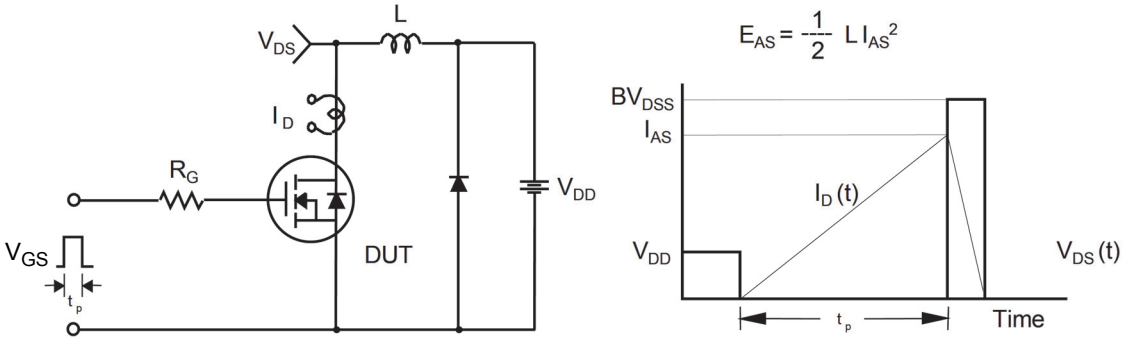



**Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms**

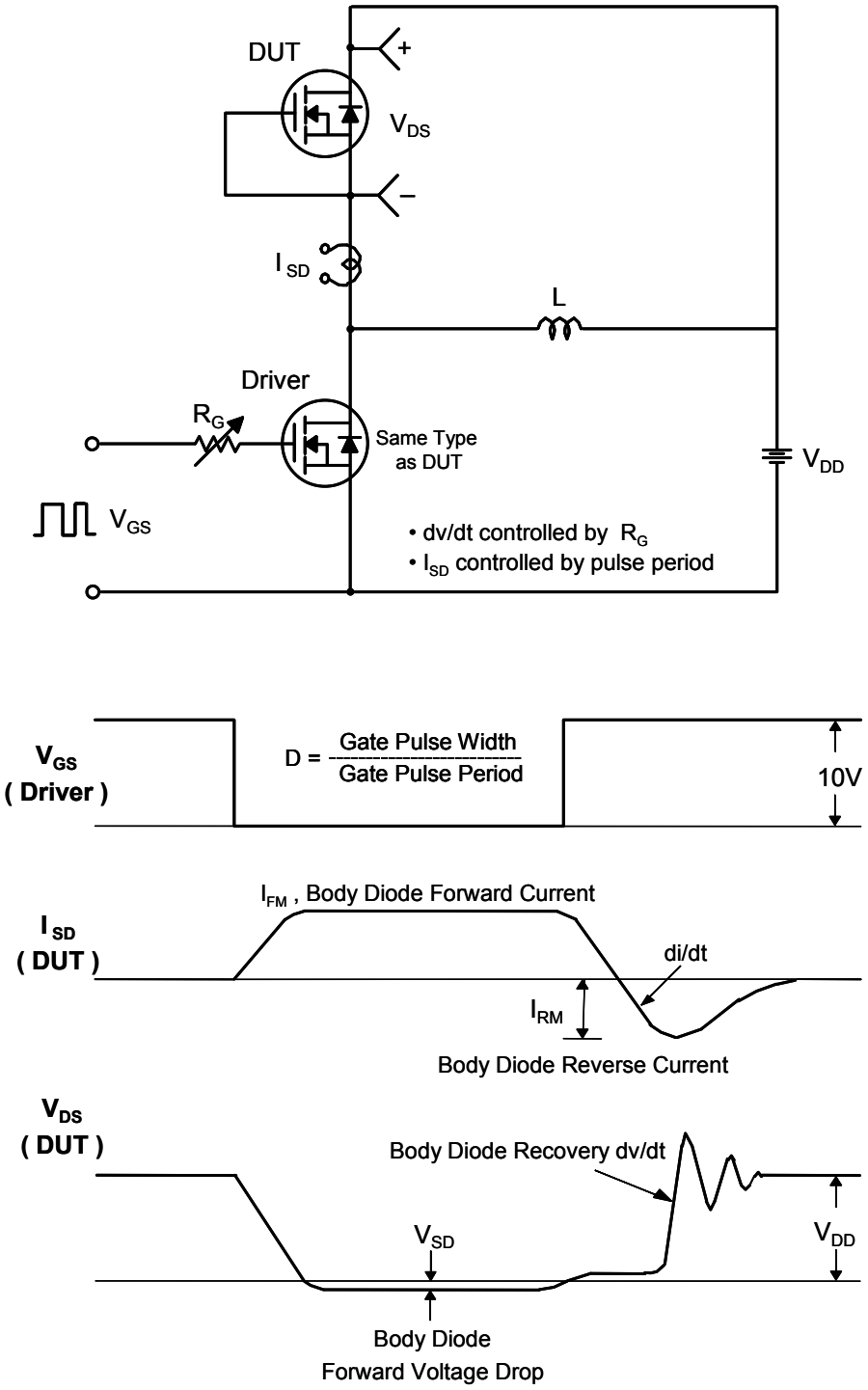



**Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

## Mechanical Dimensions

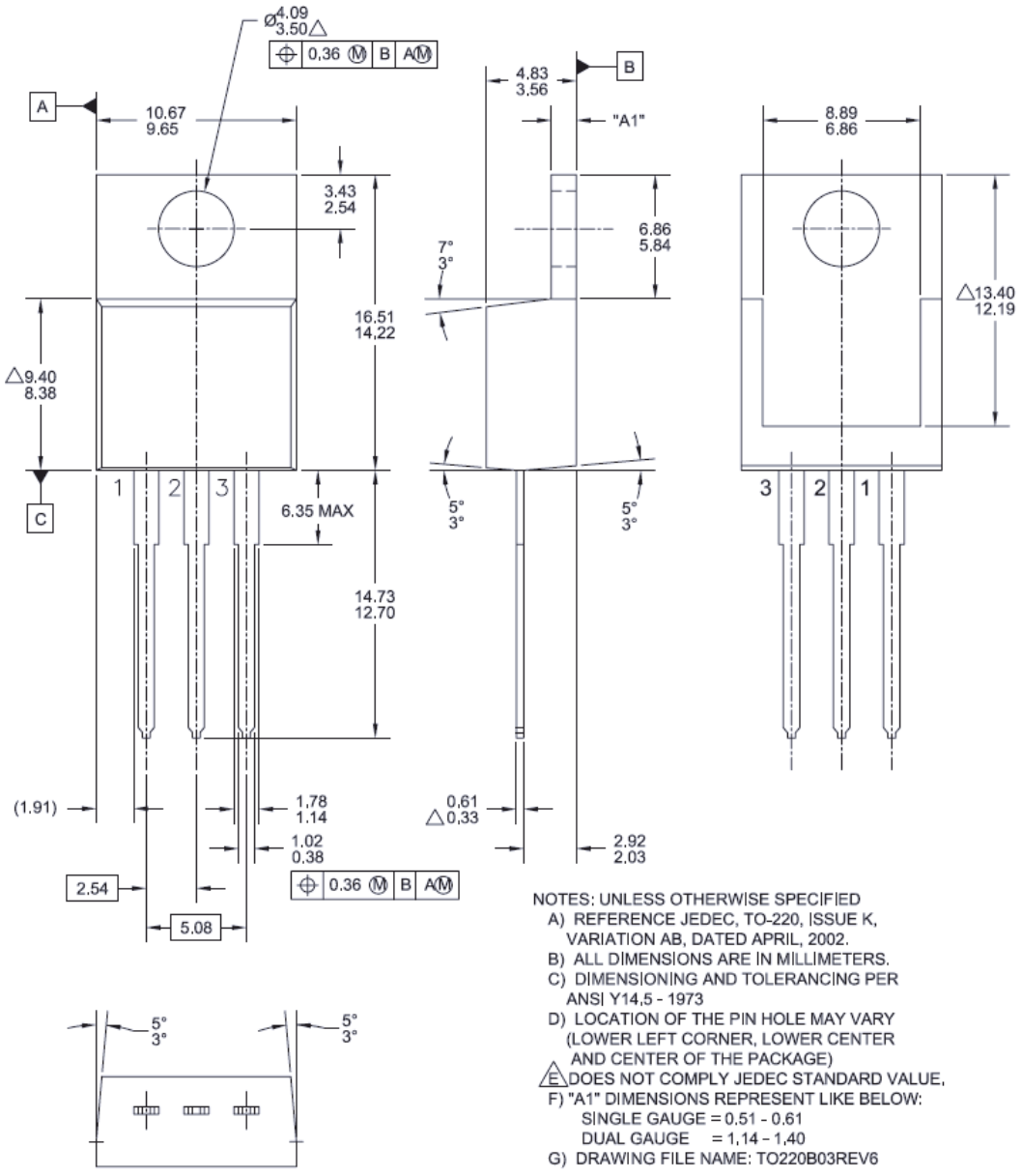



**Figure 19. TO-220, Molded, 3-Lead, Jedec Variation AB**

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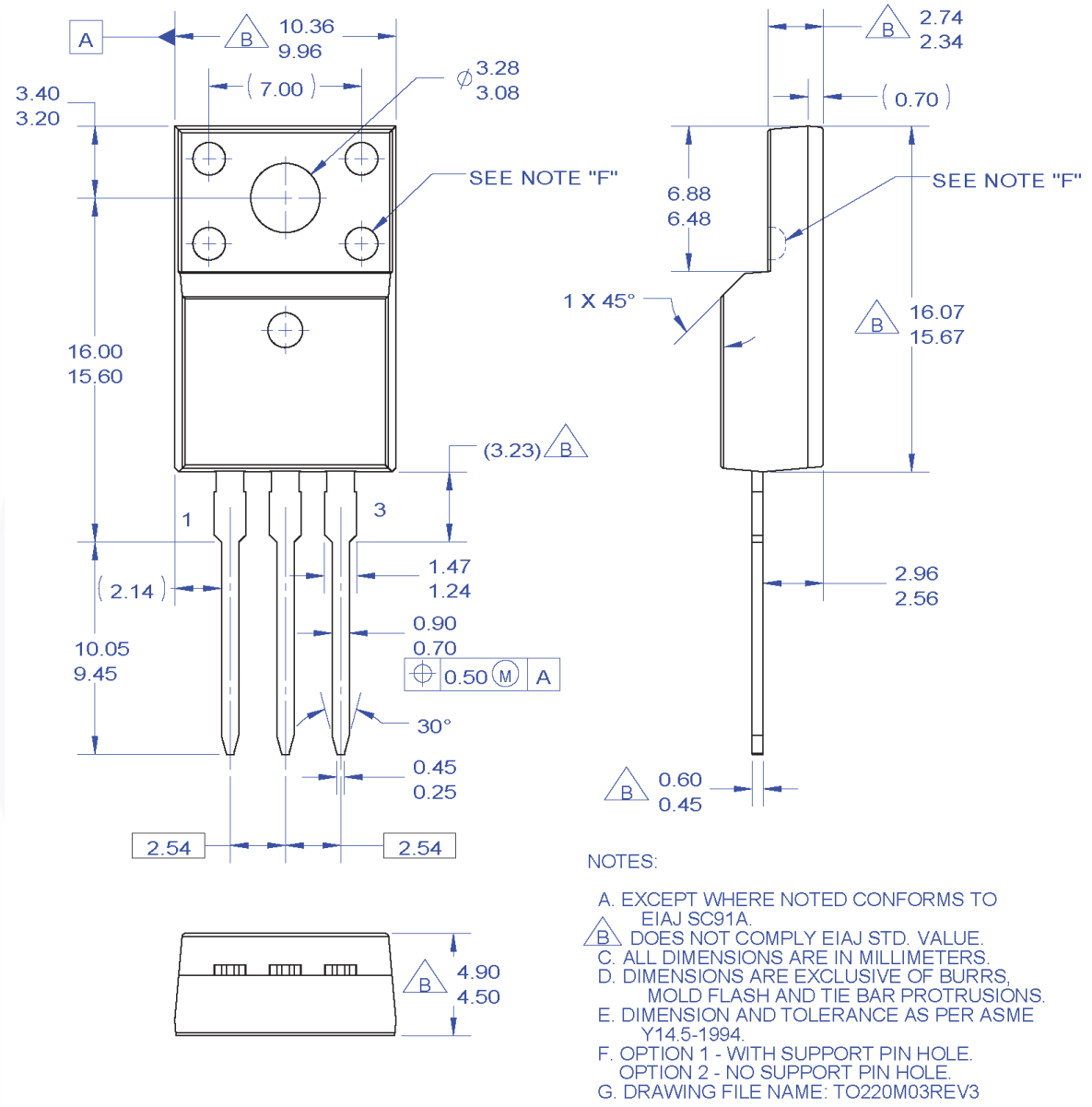


**Figure 20. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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| Datasheet Identification | Product Status | Definition |
|---|---|---|
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| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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