FAIRCHILD
SEMICONDUCTOR®

FDP80N06

N-Channel UniFET™ MOSFET

60 V, 80 A, 10 mΩ

Features

- $R_{DS(on)}$ = 8.5 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 40 A
- Low Gate Charge (Typ. 57nC)
- Low C_{rss} (Typ. 145pF)
- Fast Switching
- Improved dv/dt Capability
- RoHS Compliant

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

TO-220
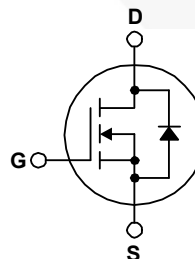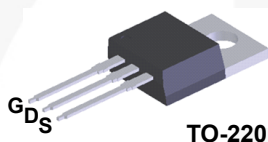
Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain to Source Voltage			60	V
V_{GSS}	Gate to Source Voltage			±20	V
I_D	Drain Current	- Continuous (T_C = 25°C)		80	A
		- Continuous (T_C = 100°C)		65	
I_{DM}	Drain Current	- Pulsed	(Note 1)	320	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	480	mJ
I_{AR}	Avalanche Current		(Note 1)	80	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	17.6	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		176	W
		- Derate above 25°C		1.17	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP80N06	FDP80N06	TO-220	Tube	N/A	50 units

Electrical Characteristics   TC = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	60	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.075	-	V/^oC
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 48V$, $T_C = 150^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm20V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 40A$	-	8.5	10	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 25V$, $I_D = 40A$	-	67	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	2450	3190	pF
C_{oss}	Output Capacitance		-	910	1190	pF
C_{rss}	Reverse Transfer Capacitance		-	145	190	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30V$, $I_D = 80A$ $R_G = 25\Omega$	-	32	75	ns
t_r	Turn-On Rise Time		-	259	528	ns
$t_{d(off)}$	Turn-Off Delay Time		-	136	282	ns
t_f	Turn-Off Fall Time	(Note 4)	-	113	236	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 48V$, $I_D = 80A$ $V_{GS} = 10V$	-	57	74	nC
Q_{gs}	Gate to Source Gate Charge		-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	24	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	80	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	320	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 80A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 80A$ $dI_F/dt = 100A/\mu s$	-	64	-	ns
Q_{rr}	Reverse Recovery Charge		-	127	-	nC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature.
2: $L = 0.15mH$, $I_{AS} = 80A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$.
3: $I_{SD} \leq 80A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$.
4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics
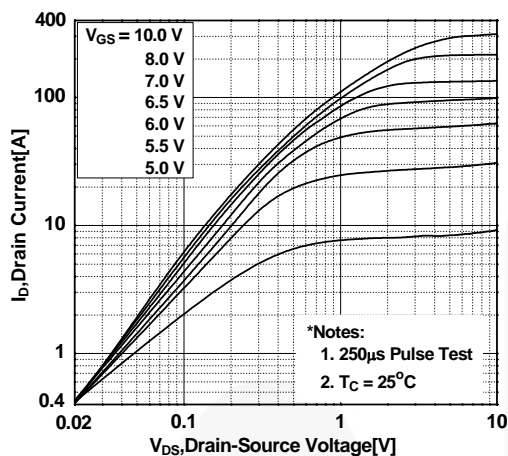
Figure 1. On-Region Characteristics

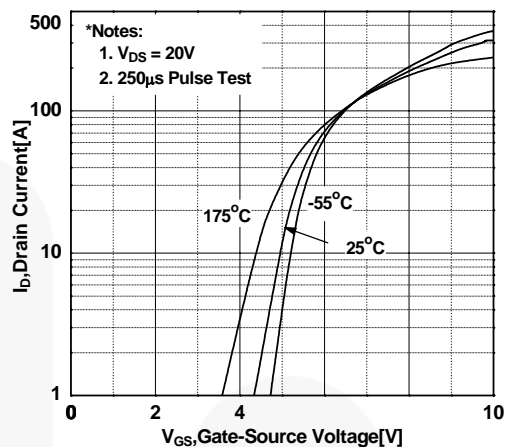### Figure 2. Transfer Characteristics

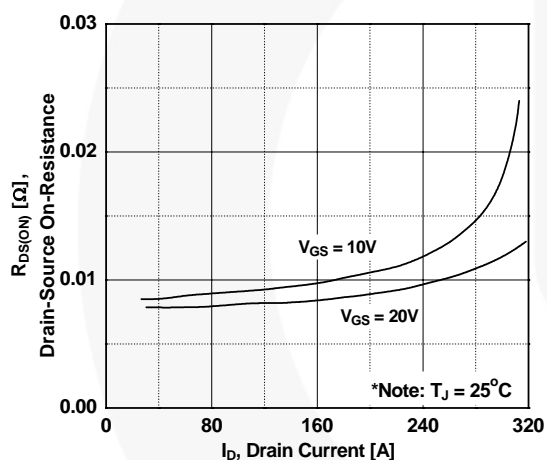### Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
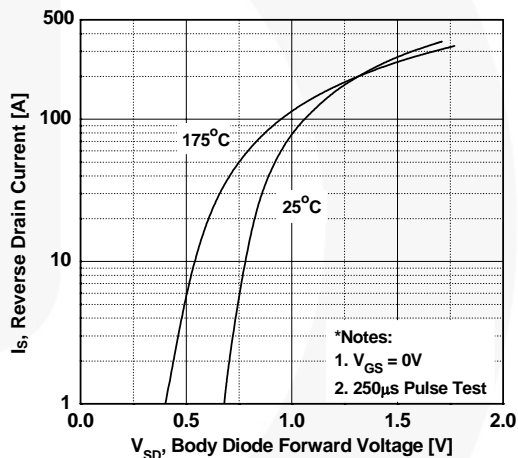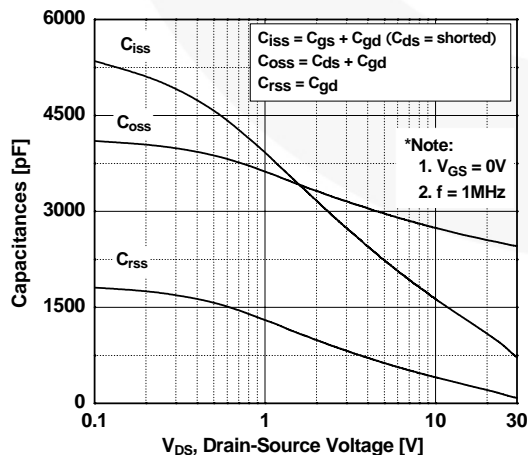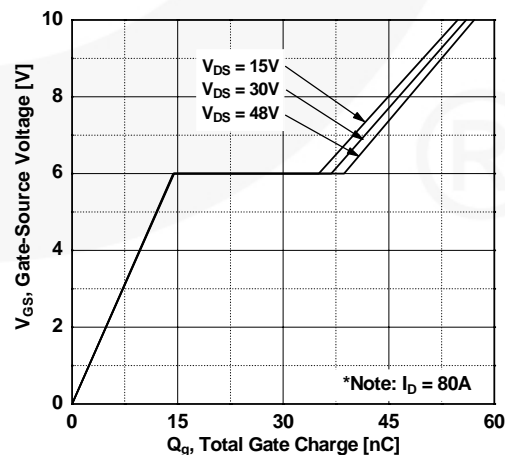

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Performance Characteristics (Continued)
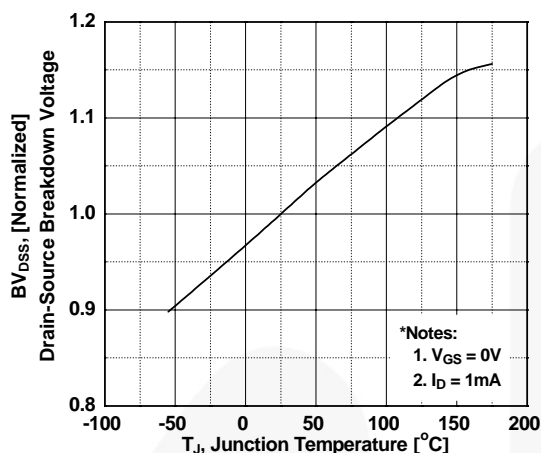
Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. $V_{GS} = 0V$
2. $I_D = 1mA$

Figure 8. On-Resistance Variation vs. Temperature

*Notes:
1. $V_{GS} = 10V$
2. $I_D = 40A$
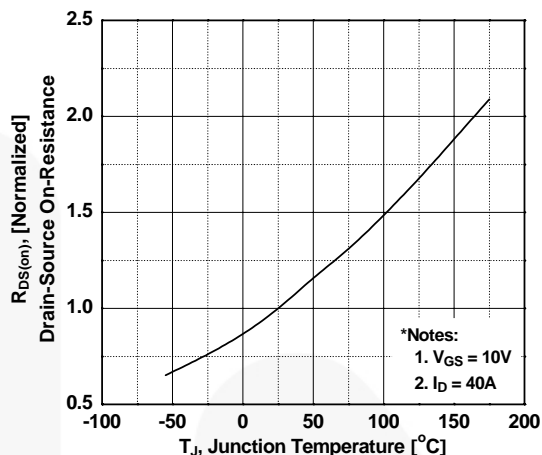
Figure 9. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

30µs
100µs
1ms
10ms
DC

*Notes:
1. $T_C = 25^oC$
2. $T_J = 175^oC$
3. Single Pulse
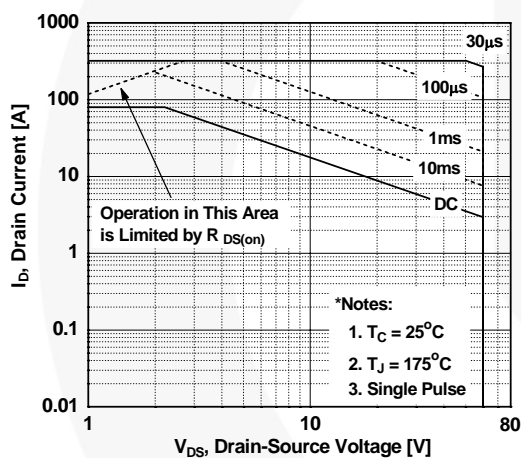
Figure 10. Maximum Drain Current vs. Case Temperature
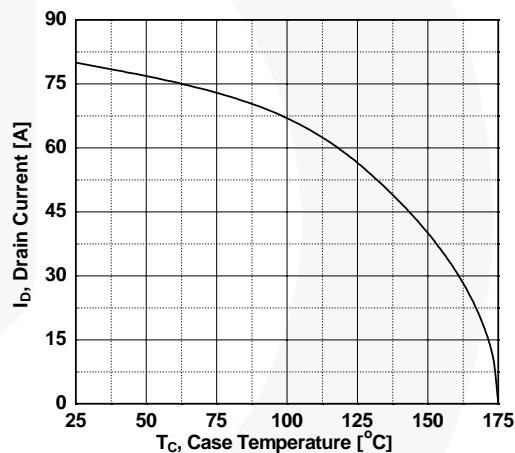
Figure 11. Transient Thermal Response Curve

Single pulse

P_{DM}

t_1
t_2

*Notes:
1. $Z_{\theta JC}(t) = 0.85^oC/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
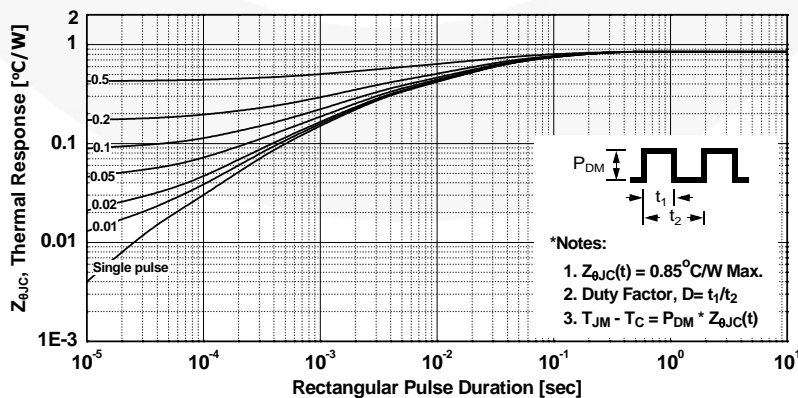
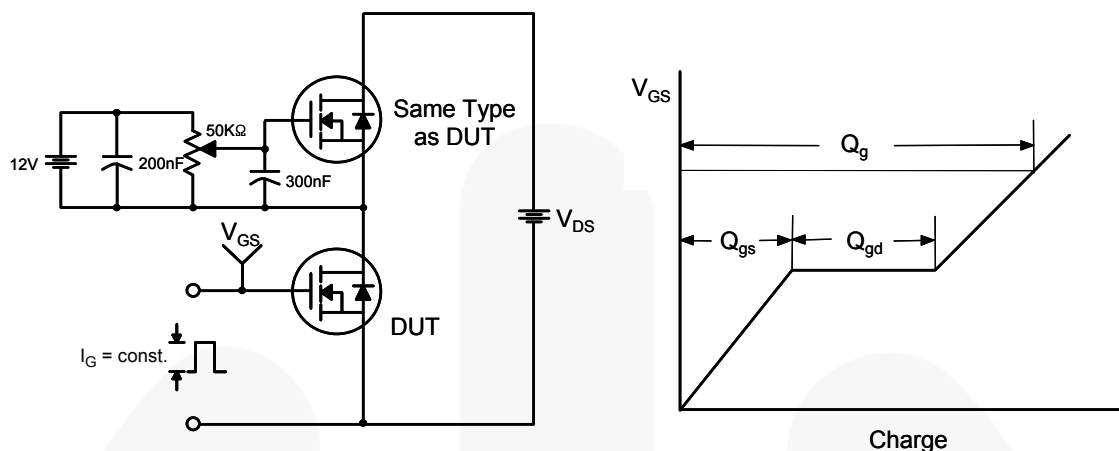## Figure 12. Gate Charge Test Circuit & Waveform

Figure 13. Resistive Switching Test Circuit & Waveforms
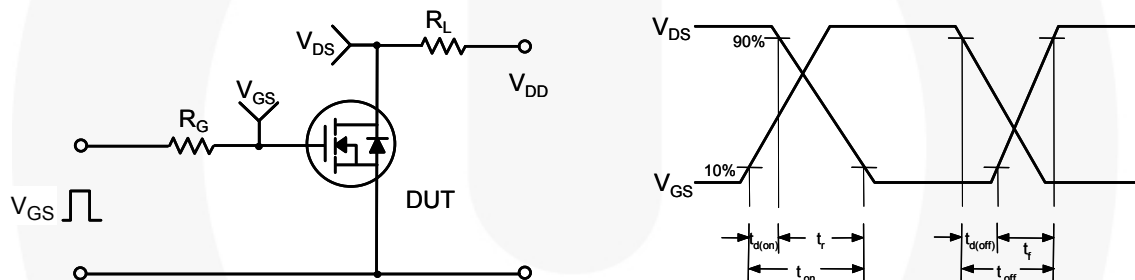
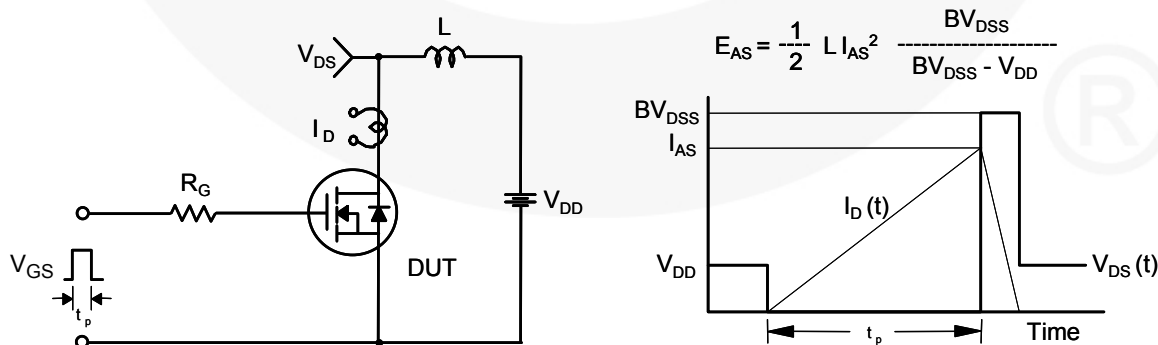## Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

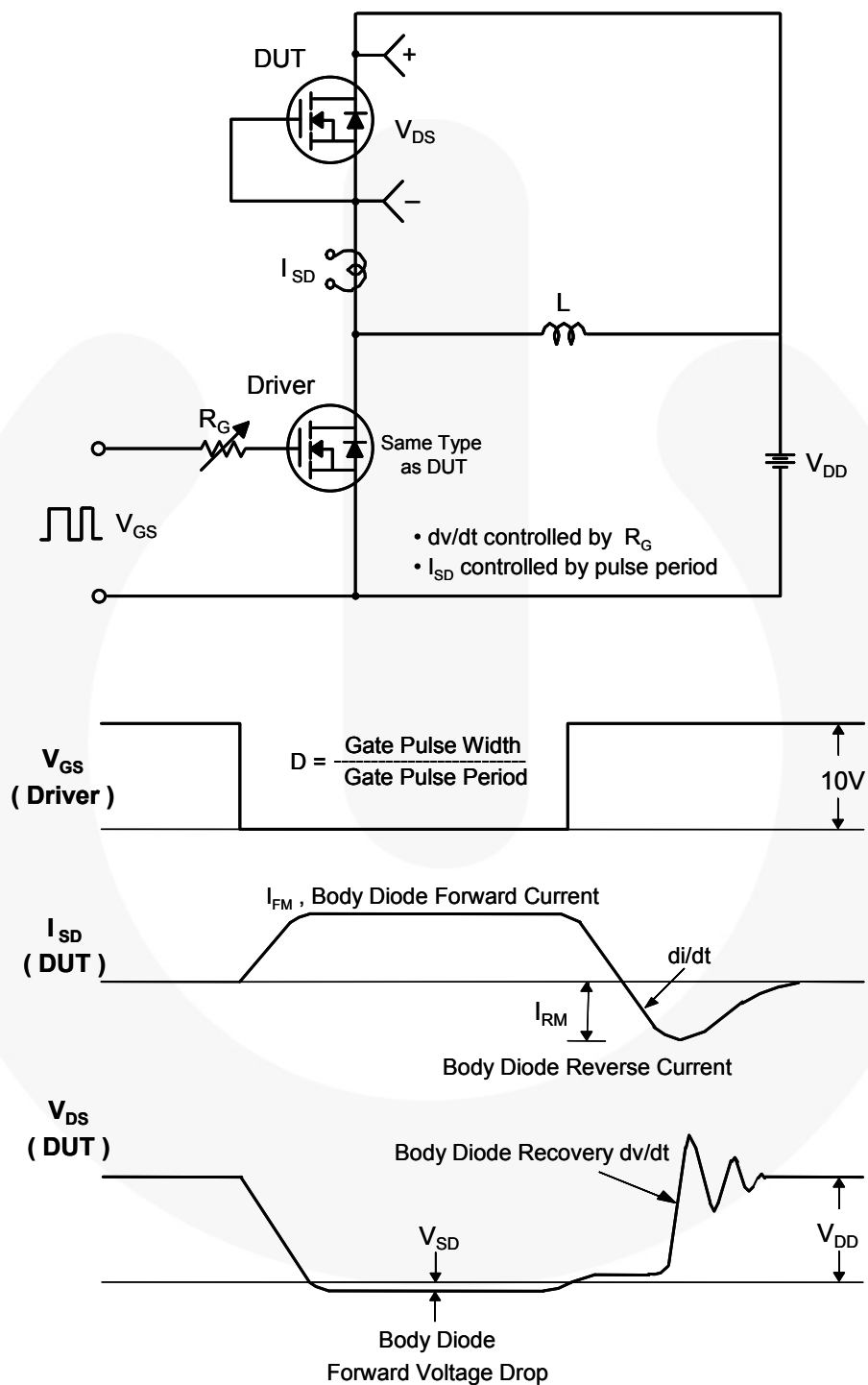$$E_{AS} = \frac{1}{2} L I_{AS}^2 \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Mechanical Dimensions

Ø 4.09
3.50

⊕ | 0.36 Ⓜ | B | AⓂ

A ▶ 10.67
9.65

B ▶

4.83
3.56

"A1"

8.89
6.86

3.43
2.54

7°
3°

6.86
5.84

16.51
14.22

9.40
8.38

C

13.40
12.19

1 2 3

6.35 MAX

5°
3°

5°
3°

3 2 1

14.73
12.70

(1.91)

1.78
1.14

0.61
0.33

1.02
0.38

2.92
2.03

2.54

⊕ | 0.36 Ⓜ | B | AⓂ

5.08

5°
3°

5°
3°

NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K,
   VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
   ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY
   (LOWER LEFT CORNER, LOWER CENTER
   AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE,
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
   SINGLE GAUGE = 0.51 - 0.61
   DUAL GAUGE = 1.14 - 1.40
G) DRAWING FILE NAME: TO220B03REV6

Figure 16. TO-220, Molded, 3Lead, Jedec Variation AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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