

# FDP8447L

## N-Channel PowerTrench® MOSFET 40V, 50A, 8.7mΩ

### Features

- Max  $r_{DS(on)}$  = 8.7mΩ at  $V_{GS} = 10V$ ,  $I_D = 14A$
- Max  $r_{DS(on)}$  = 11.2mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 11A$
- Fast Switching
- RoHS Compliant

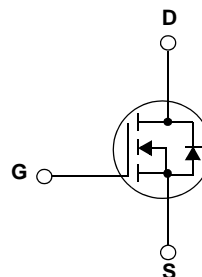
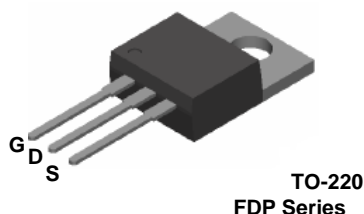


### General Description

This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench technology to deliver low  $r_{DS(on)}$  and optimized  $BV_{DSS}$  capability to offer superior performance benefit in the application.

### Applications

- Inverter
- Power Supplies



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	50	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	65	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1)	12	
	-Pulsed	100	
$E_{AS}$	Drain-Source Avalanche Energy (Note 3)	153	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	60	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1)	2	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	62.5	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8447L	FDP8447L	TO-220AB	Tube	N/A	50units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		34		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$ ,			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 14\text{A}$		7.7	8.7	m $\Omega$
		$V_{GS} = 4.5\text{V}$ , $I_D = 11\text{A}$		8.9	11.2	
		$V_{GS} = 10\text{V}$ , $I_D = 14\text{A}$ , $T_J = 125^\circ\text{C}$		12.1	13.7	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{V}$ , $I_D = 14\text{A}$		74		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$		1880	2500	pF
$C_{oss}$	Output Capacitance			245	325	pF
$C_{rss}$	Reverse Transfer Capacitance			150	225	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		1.4		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}$ , $I_D = 14\text{A}$ , $V_{GS} = 10\text{V}$ , $R_{GEN} = 6\Omega$		9	18	ns
$t_r$	Rise Time			7	14	ns
$t_{d(off)}$	Turn-Off Delay Time			28	45	ns
$t_f$	Fall Time			4	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V}$ to $10\text{V}$	$V_{DD} = 20\text{V}$ , $I_D = 14\text{A}$	35	49	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V}$ to $5\text{V}$		19	27	nC
$Q_{gs}$	Gate to Source Charge			4.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			6.2		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_S = 14\text{A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 14\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$		28	42	ns
$Q_{rr}$	Reverse Recovery Charge			22	33	nC

## NOTES:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
- Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $I_{AS} = 17.5\text{A}$ ,  $V_{DD} = 40\text{V}$ ,  $V_{GS} = 10\text{V}$ .

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

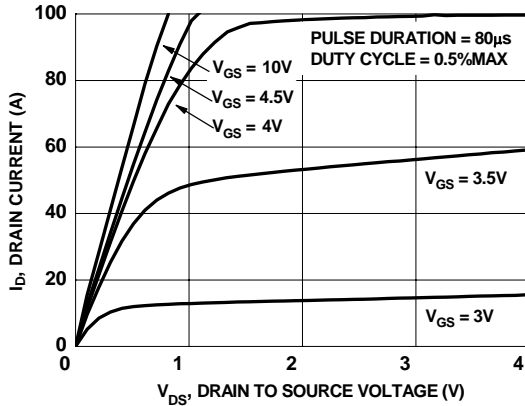


Figure 1. On-Region Characteristics

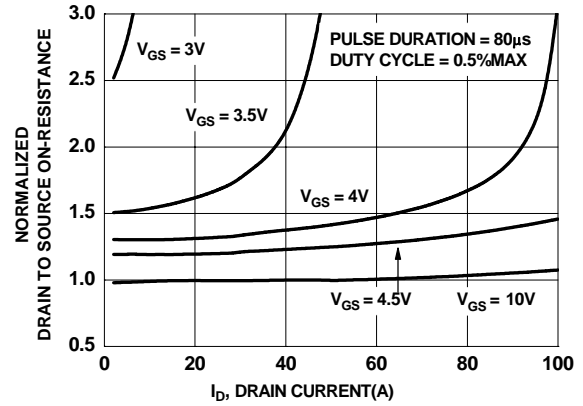


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

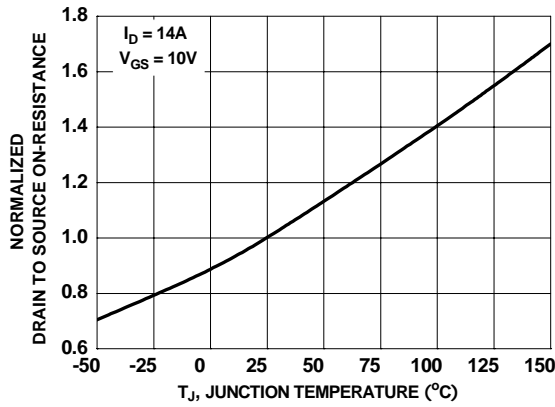


Figure 3. Normalized On-Resistance vs Junction Temperature

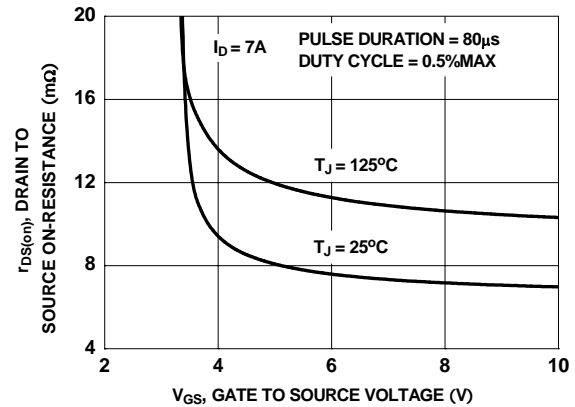


Figure 4. On-Resistance vs Gate to Source Voltage

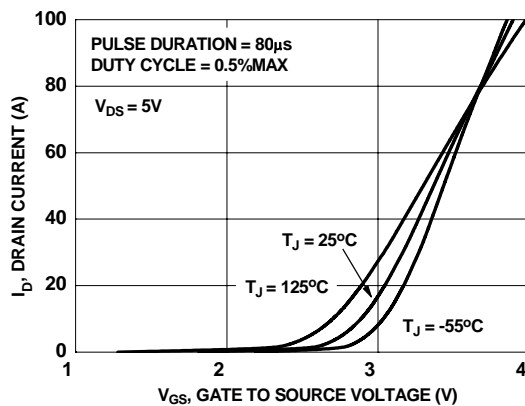


Figure 5. Transfer Characteristics

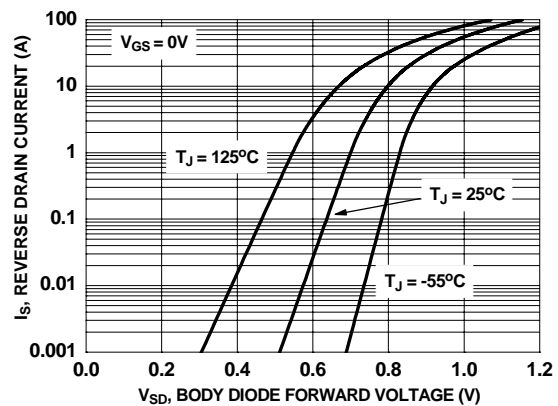


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

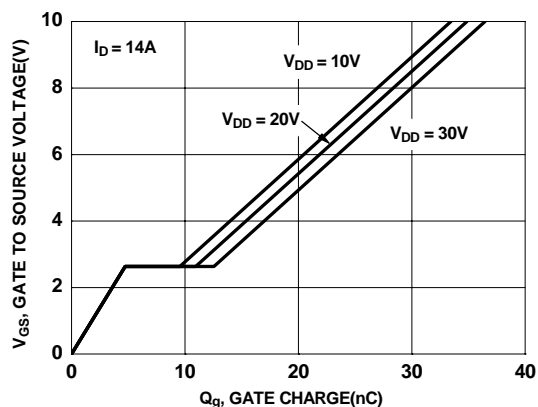


Figure 7. Gate Charge Characteristics

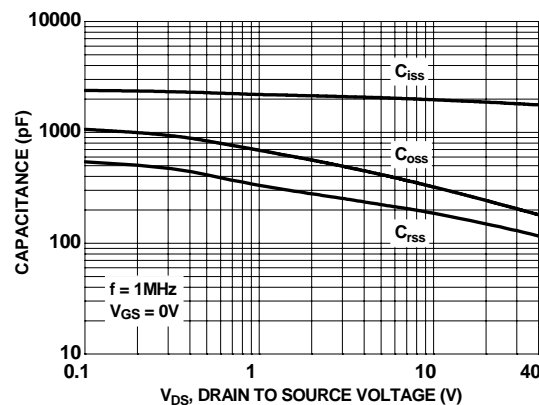


Figure 8. Capacitance vs Drain to Source Voltage

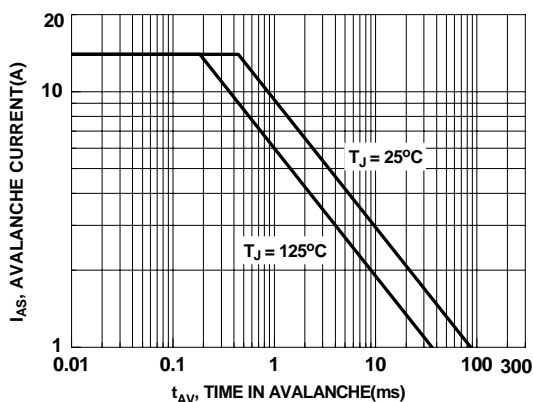


Figure 9. Unclamped Inductive Switching Capability

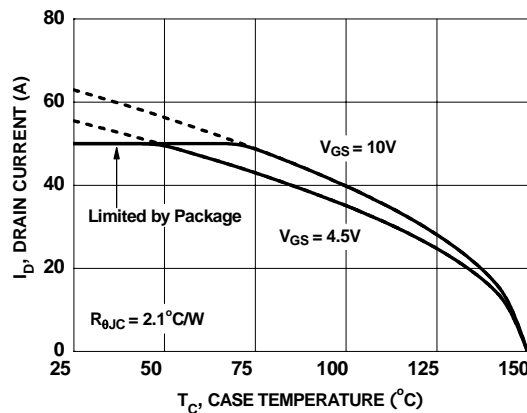


Figure 10. Maximum Continuous Drain Current vs Case Temperature

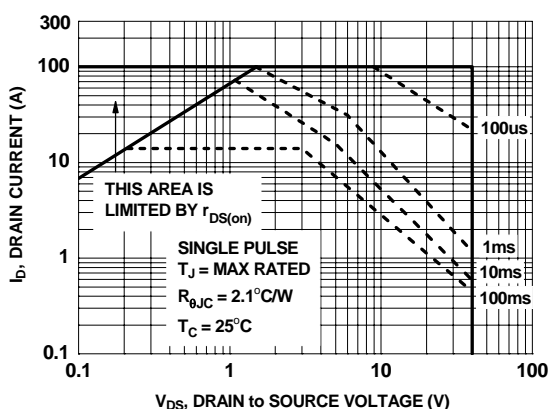


Figure 11. Forward Bias Safe Operating Area

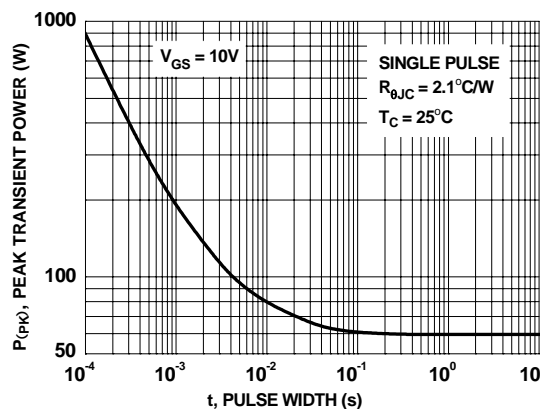
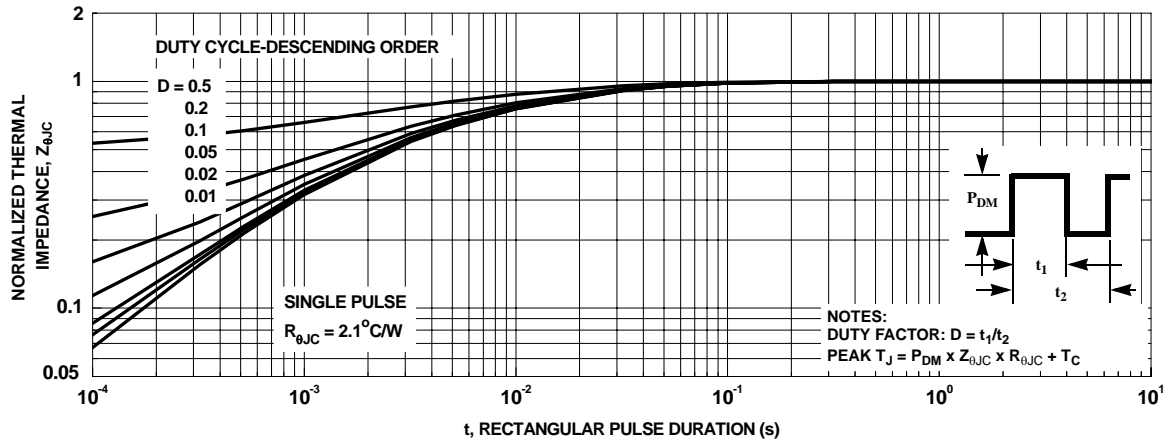


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted





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