

MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 76 A, 8.5 mΩ

FDP8D5N10C,
FDPF8D5N10C

General Description

This N-Channel MV MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

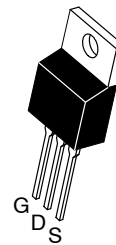
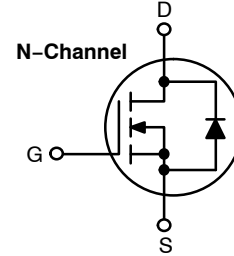
- Max $R_{DS(on)}$ = 8.5 mΩ at $V_{GS} = 10$ V, $I_D = 76$ A
- Extremely Low Reverse Recovery Charge, Q_{rr}
- 100% UIL Tested
- RoHS Compliant

Applications

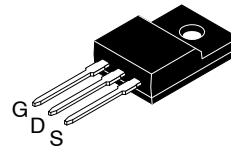
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	8.5 mΩ @ 10 V	76 A*

*Drain current limited by maximum junction temperature.



TO-220
CASE 221A



TO-220 Fullpack, 3-Lead
/ TO-220F-3SG
CASE 221AT

MARKING DIAGRAM



XXX8D5N10C = Device Code (XXX = FDP, FDPF)
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FDP8D5N10C	TO-220	800 Units / Tube
FDPF8D5N10C	TO-220F	1000 Units / Tube

FDP8D5N10C, FDPF8D5N10C

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Rating		Unit
			FDP8D5N10C	FDPF8D5N10C	
V_{DS}	Drain to Source Voltage		100	100	V
V_{GS}	Gate to Source Voltage		± 20	± 20	V
I_D	Drain Current	- Continuous, $T_C = 25^\circ\text{C}$ (Note 3)	76	76*	A
		- Continuous, $T_C = 100^\circ\text{C}$ (Note 3)	54	54*	
		- Pulsed (Note 1)	304	304*	
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		181		mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	107	35	W
		$T_A = 25^\circ\text{C}$	2.4	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +175		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Pulsed I_D please refer to Figure 11 and Figure 12 "Forward Bias Safe Operating Area" for more details.
2. E_{AS} of 181 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 11\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 25\text{ A}$.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP8D5N10C	FDPF8D5N10C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	4.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

FDP8D5N10C, FDPF8D5N10C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100	–	–	V
$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	57	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 80 V, T _J = 150°C	–	–	500	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 130 μA	2.0	3.0	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 76 A	–	7.4	8.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 76 A	–	68	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	–	1765	2475	pF
C _{oss}	Output Capacitance		–	1010	1415	pF
C _{rss}	Reverse Transfer Capacitance		–	16	25	pF
R _g	Gate Resistance		0.1	0.8	1.6	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 50 V, I _D = 76 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	12	22	ns
t _r	Rise Time		–	11	20	ns
t _{d(off)}	Turn-Off Delay Time		–	18	28	ns
t _f	Fall Time		–	4	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 50 V, I _D = 76 A	–	25	34	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 50 V, I _D = 76 A	–	9	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	5	–	nC
Q _{oss}	Output Charge	V _{DD} = 50 V, V _{GS} = 0 V	–	68	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	76	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	304	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 76 A	–	1.0	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 50 V, I _F = 76 A, dI _F /dt = 100 A/μs	–	58	92	ns
Q _{rr}	Reverse Recovery Charge		–	53	85	nC
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 50 V, I _F = 76 A, dI _F /dt = 300 A/μs	–	51	81	ns
Q _{rr}	Reverse Recovery Charge		–	141	226	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDP8D5N10C, FDPF8D5N10C

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

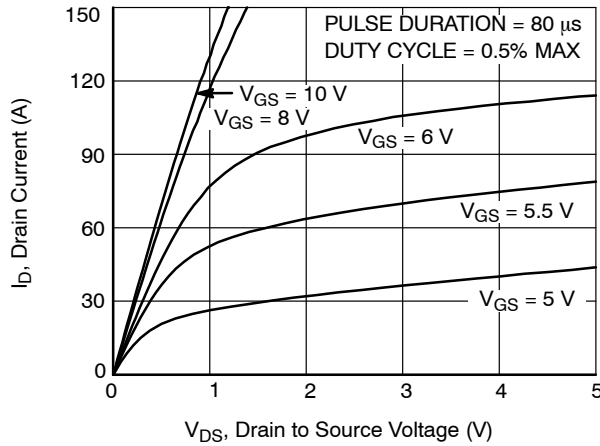


Figure 1. On-Region Characteristics

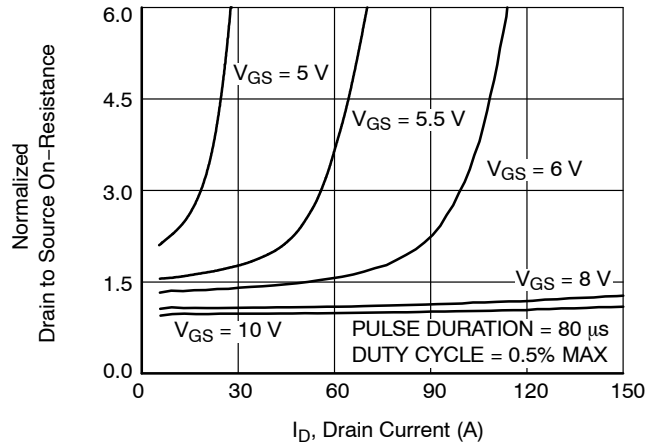


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

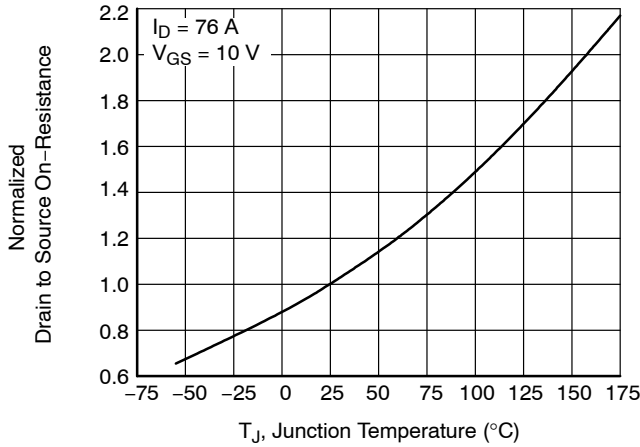


Figure 3. Normalized On-Resistance vs. Junction Temperature

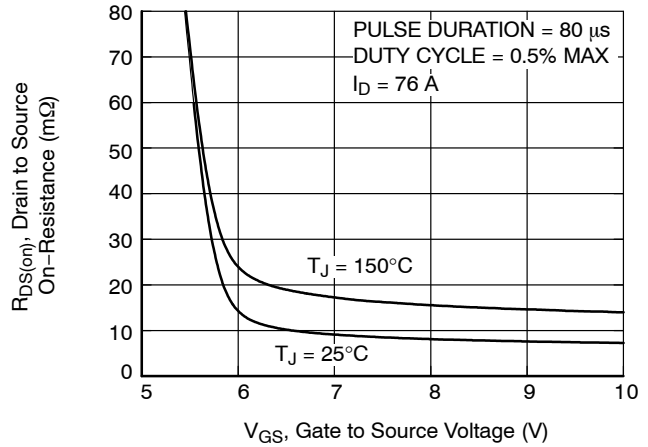


Figure 4. On-Resistance vs. Gate to Source Voltage

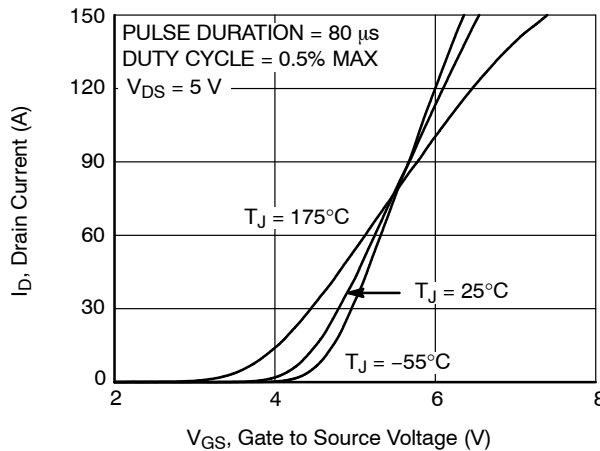


Figure 5. Transfer Characteristics

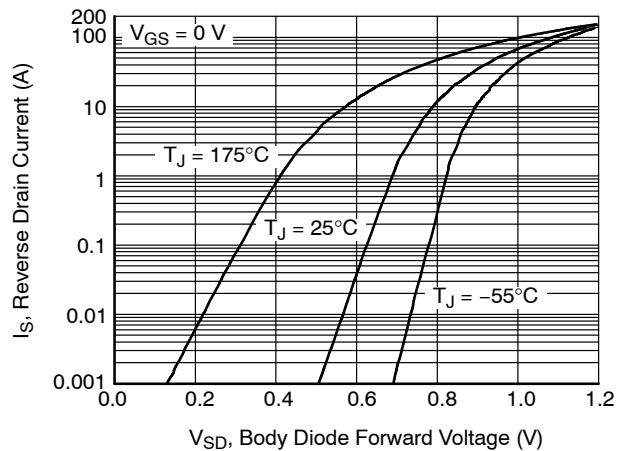


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDP8D5N10C, FDPF8D5N10C

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

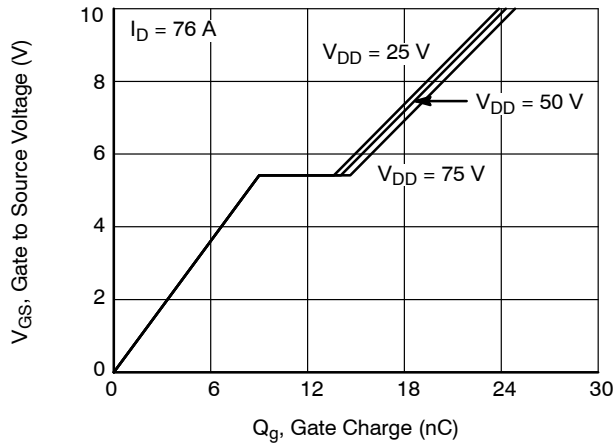


Figure 7. Gate Charge Characteristics

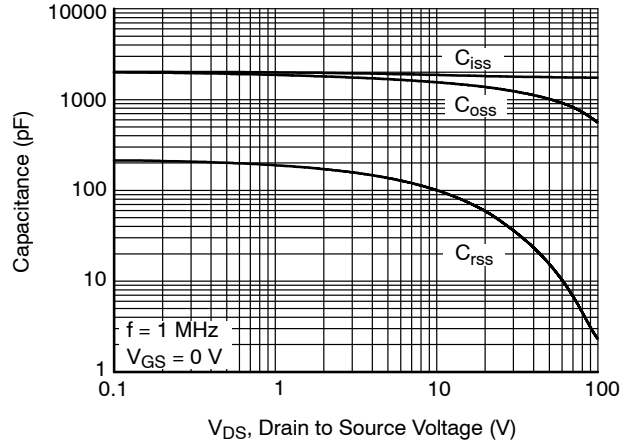


Figure 8. Capacitance vs. Drain to Source Voltage

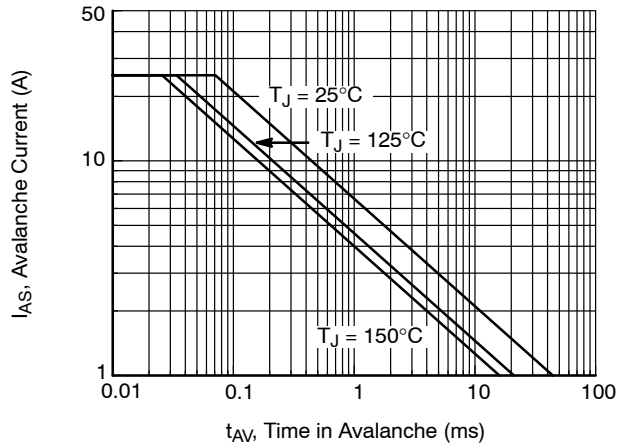


Figure 9. Unclamped Inductive Switching Capability

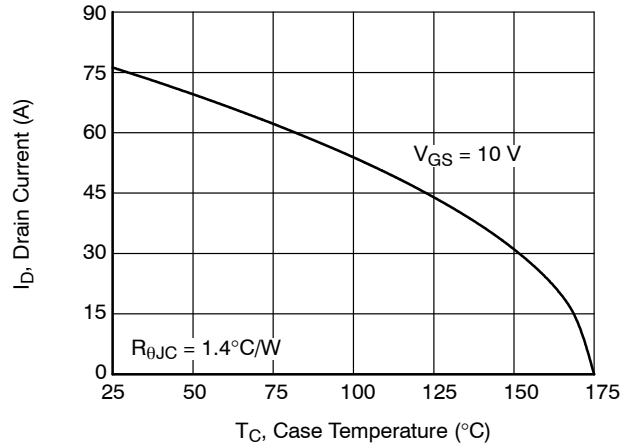


Figure 10. Maximum Continuous Drain Current vs. Case Temperature for FDP8D5N10C

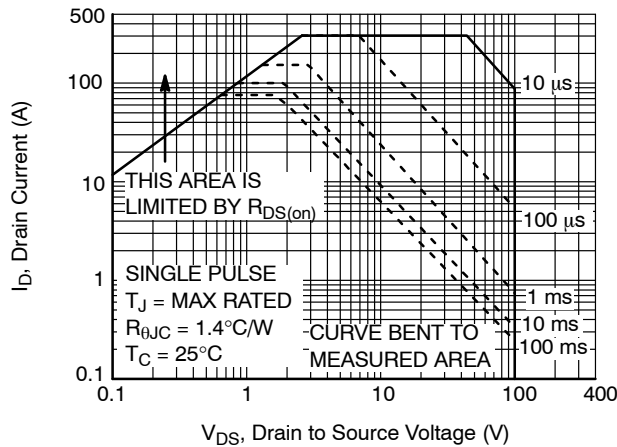


Figure 11. Forward Bias Safe Operating Area for FDP8D5N10C

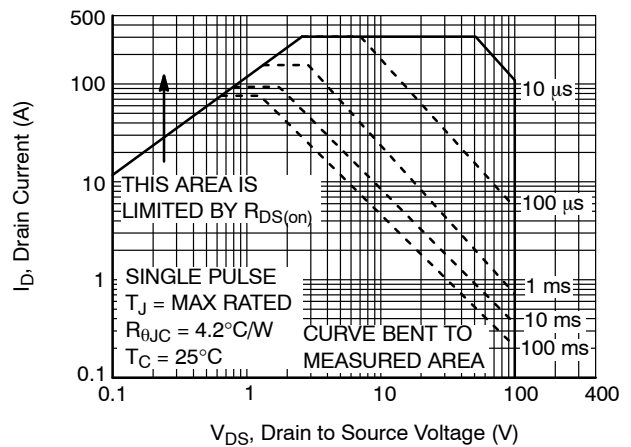


Figure 12. Forward Bias Safe Operating Area for FDPF8D5N10C

FDP8D5N10C, FDPF8D5N10C

TYPICAL PERFORMANCE CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

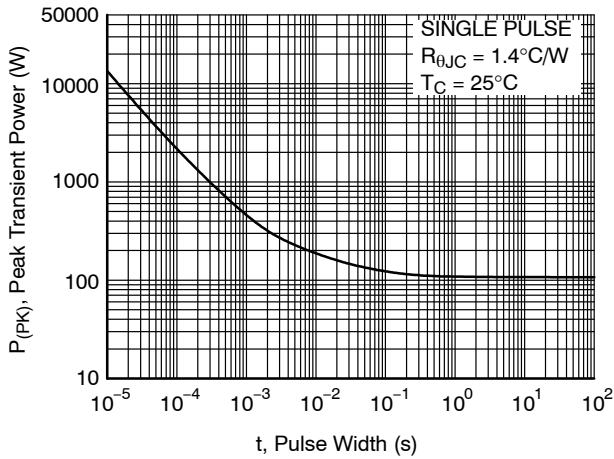


Figure 13. Single Pulse Maximum Power Dissipation for FDP8D5N10C

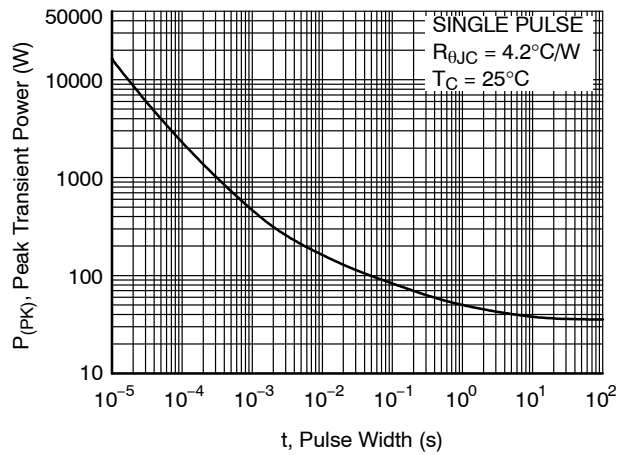


Figure 14. Single Pulse Maximum Power Dissipation for FDPF8D5N10C

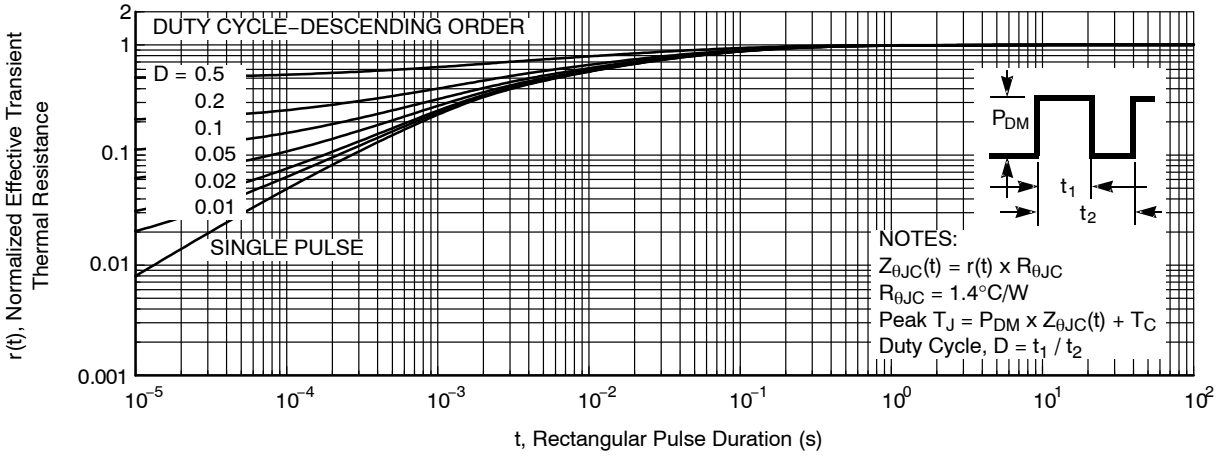


Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP8D5N10C

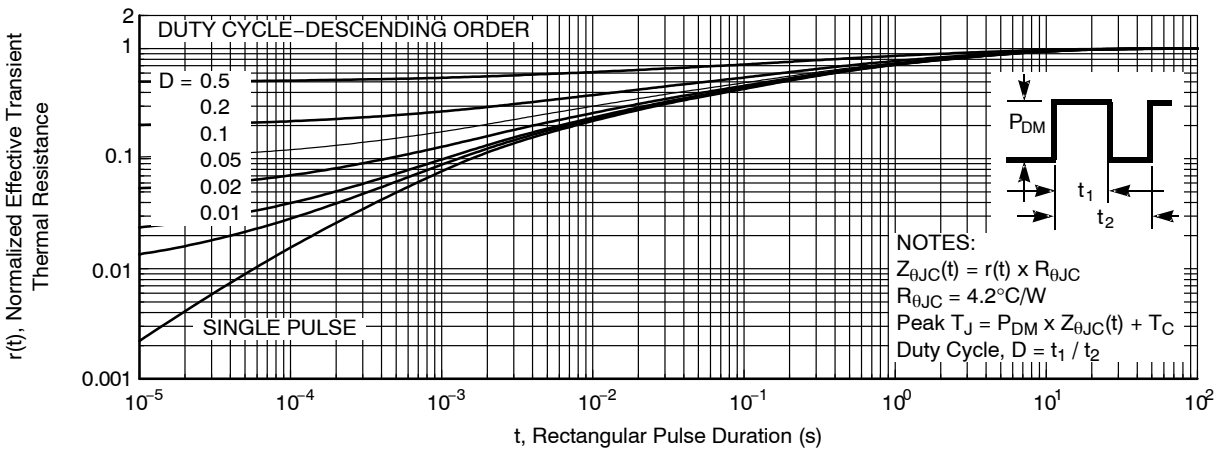
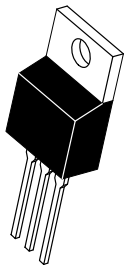


Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF8D5N10C

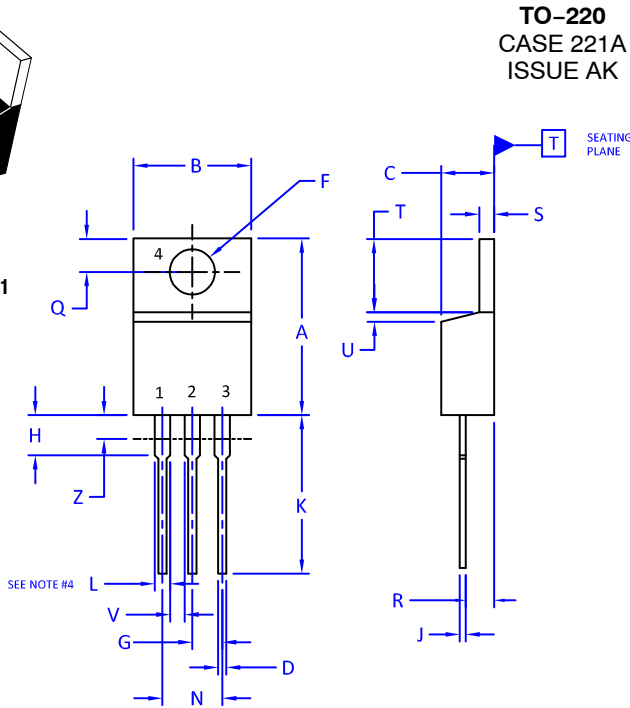
FDP8D5N10C, FDPF8D5N10C

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

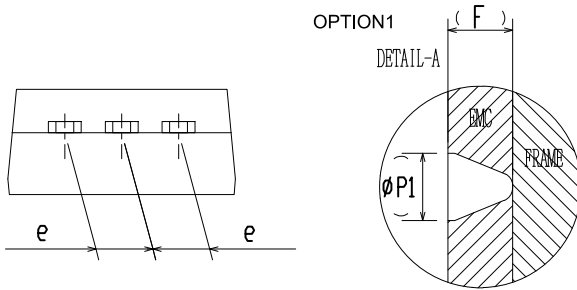
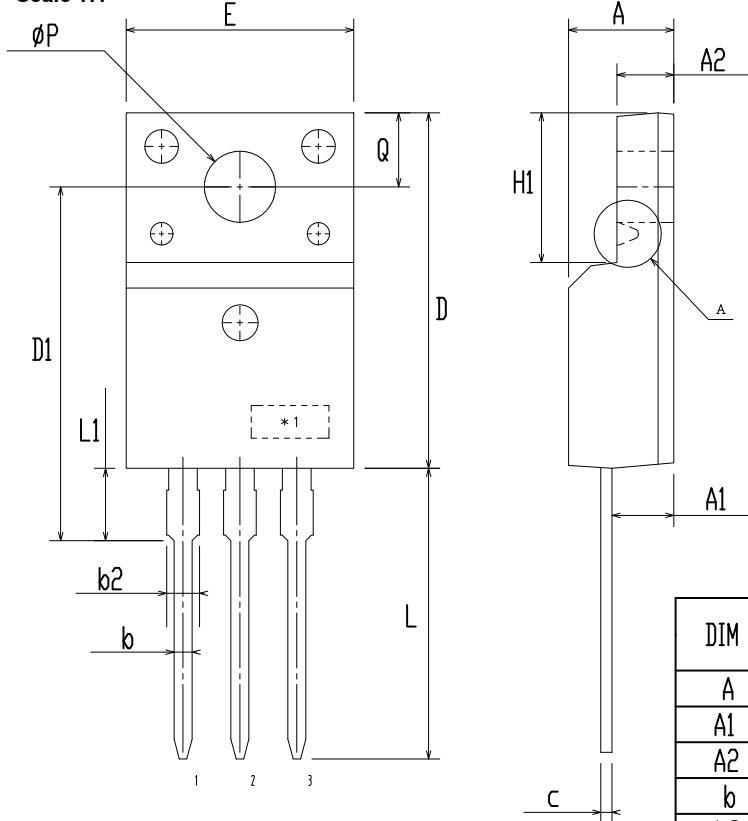


TO-220 Fullpack, 3-Lead / TO-220F-3SG CASE 221AT ISSUE B

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
phi P	2.98	3.18	3.38
phi P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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