

FDP20N50 / FDPF20N50 / FDPF20N50T

N-Channel UniFET™ MOSFET

500 V, 20 A, 230 mΩ

Features

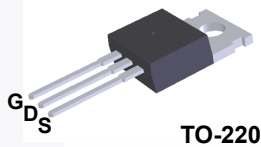
- $R_{DS(on)} = 200 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$
- Low Gate Charge (Typ. 45.6 nC)
- Low C_{rss} (Typ. 27 pF)
- 100% Avalanche Tested

Applications

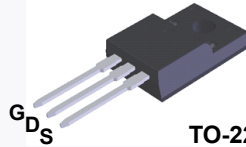
- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

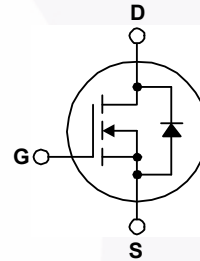
UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220



TO-220F



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP20N50	FDPF20N50 / FDPF20N50T	Unit
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	20	20 *	A
		12.9	12.9 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	80	80 *A	
V_{GSS}	Gate-Source voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1110		mJ
I_{AR}	Avalanche Current (Note 1)	20		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	25		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	250	38.5	W
		2.0	0.3	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FDP20N50	FDPF20N50/ FDPF20N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.5	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP20N50	FDP20N50	TO-220	Tube	N/A	N/A	50 units
FDPF20N50	FDPF20N50	TO-220F	Tube	N/A	N/A	50 units
FDPF20N50T	FDPF20N50	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C -	-	0.5	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	--	0.20	0.23	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 10\text{ A}$	--	24.6	--	S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2400	3120	pF
C_{OSS}	Output Capacitance		--	355	465	pF
C_{RSS}	Reverse Transfer Capacitance		--	27	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	--	95	200	ns
t_r	Turn-On Rise Time		--	375	760	ns
$t_{d(off)}$	Turn-Off Delay Time	(Note 4)	--	100	210	ns
t_f	Turn-Off Fall Time		--	105	220	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$	--	45.6	59.5	nC
Q_{gs}	Gate-Source Charge		--	14.8	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	21.6	--
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	80	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 20\text{ A},$ $di_f/dt = 100\text{ A}/\mu\text{s}$	--	507	--	ns
Q_{rr}	Reverse Recovery Charge		--	7.20	--	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 5.0\text{ mH}, I_{AS} = 20\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 20\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

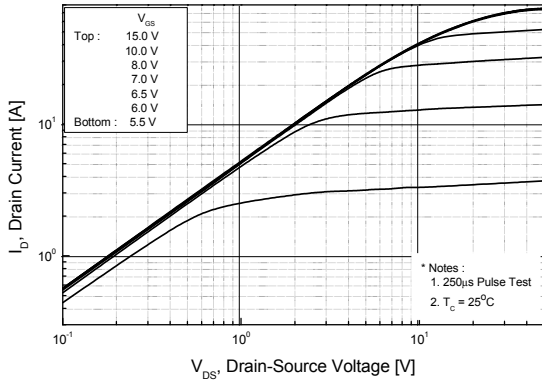


Figure 2. Transfer Characteristics

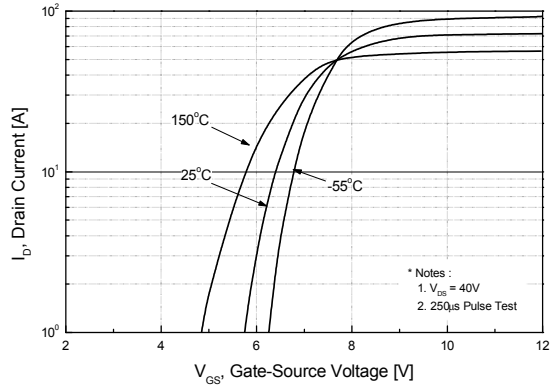


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

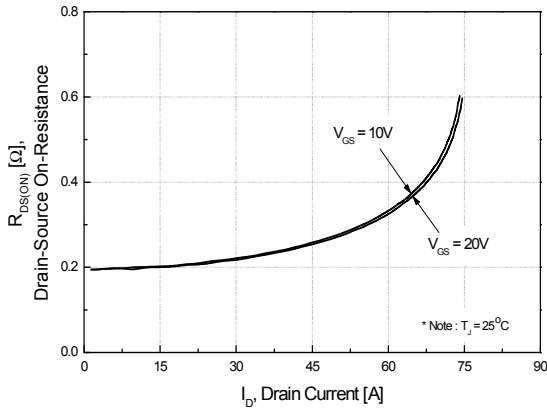


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

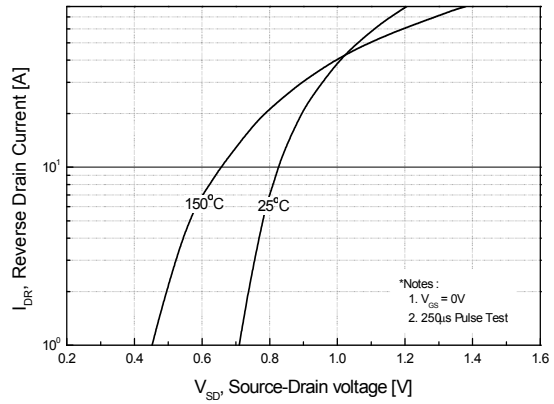


Figure 5. Capacitance Characteristics

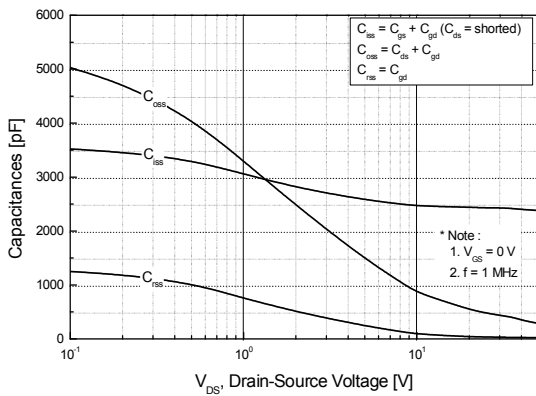
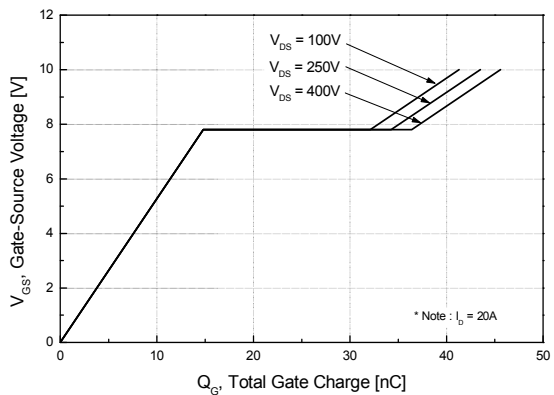


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

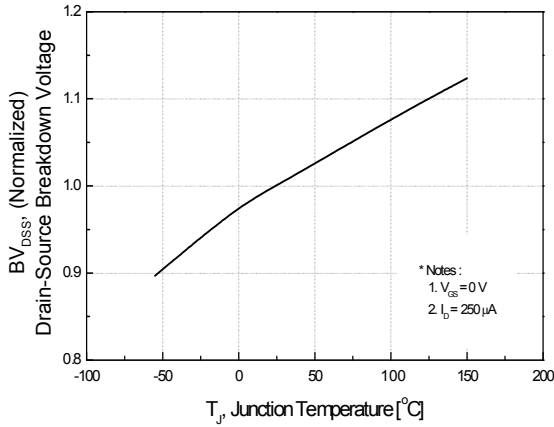


Figure 8. On-Resistance Variation vs. Temperature

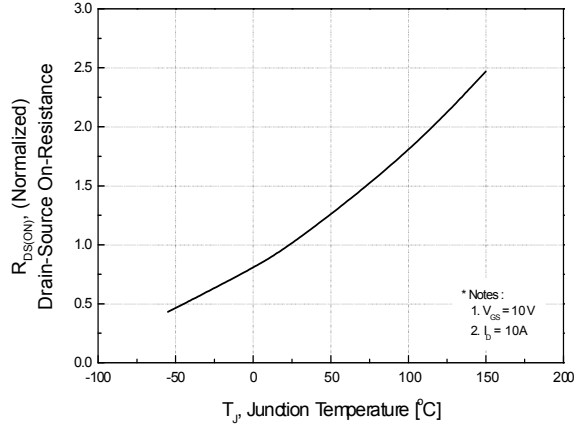


Figure 9-1. Maximum Safe Operating Area - FDP20N50

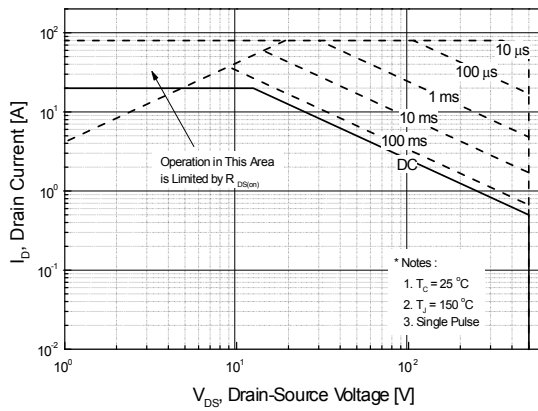


Figure 9-2. Maximum Safe Operating Area - FDPF20N50

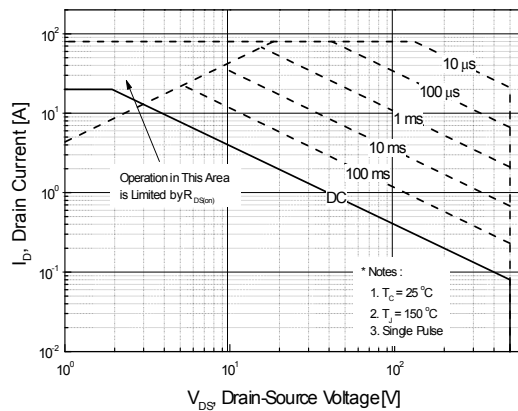
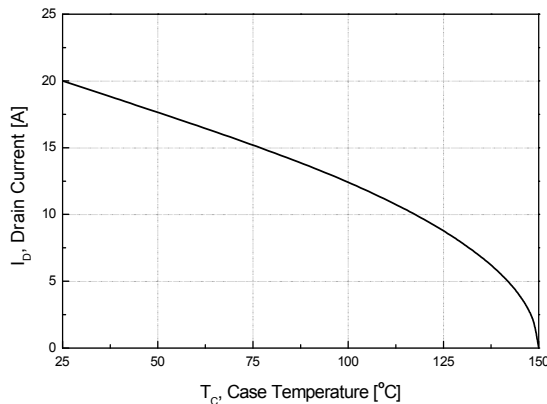


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve - FDP20N50

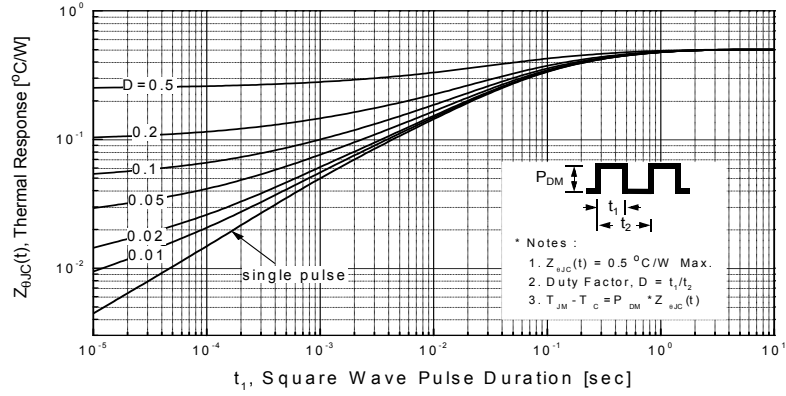
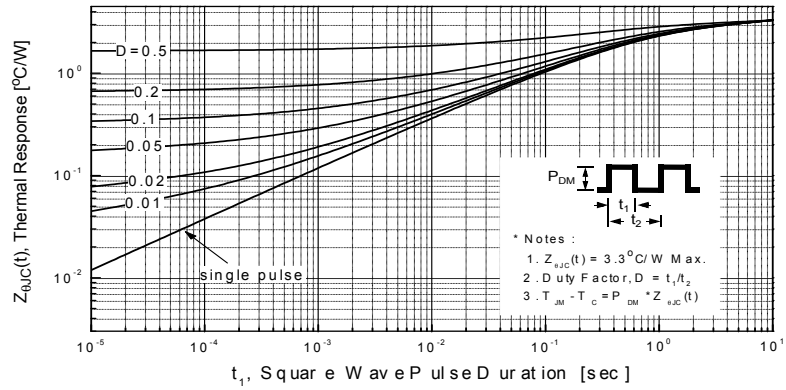


Figure 11-2. Transient Thermal Response Curve - FDPF20N50



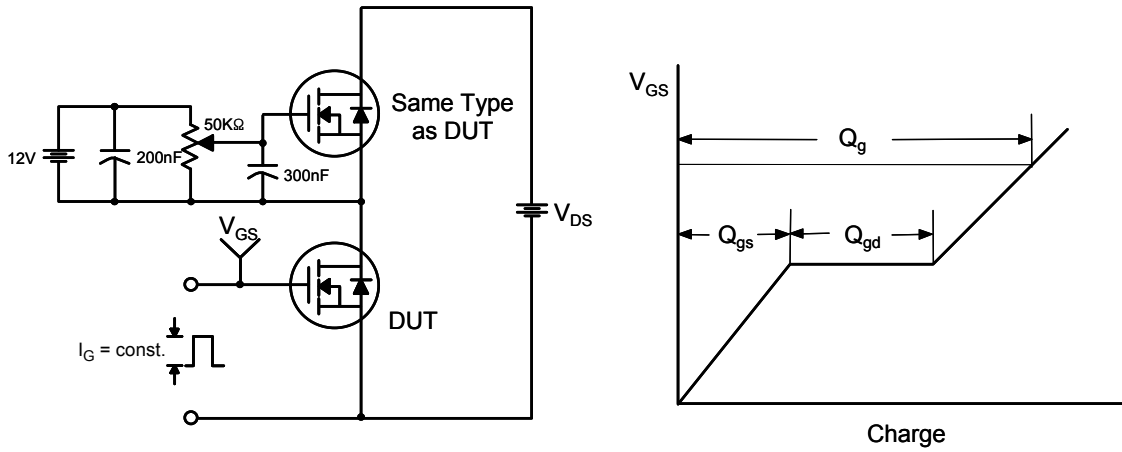


Figure 12. Gate Charge Test Circuit & Waveform

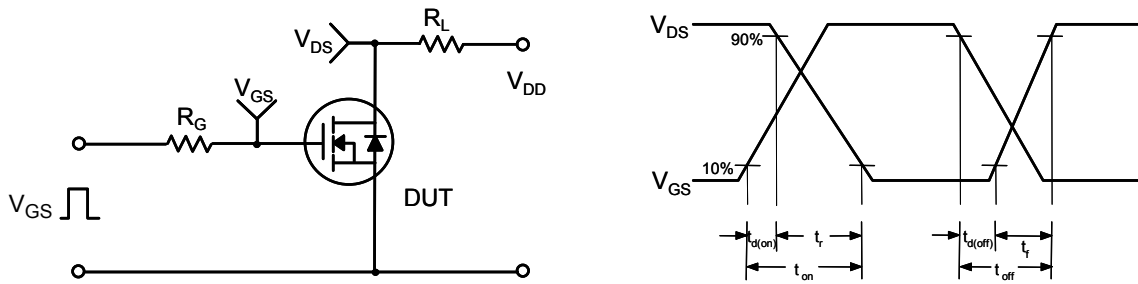


Figure 13. Resistive Switching Test Circuit & Waveforms

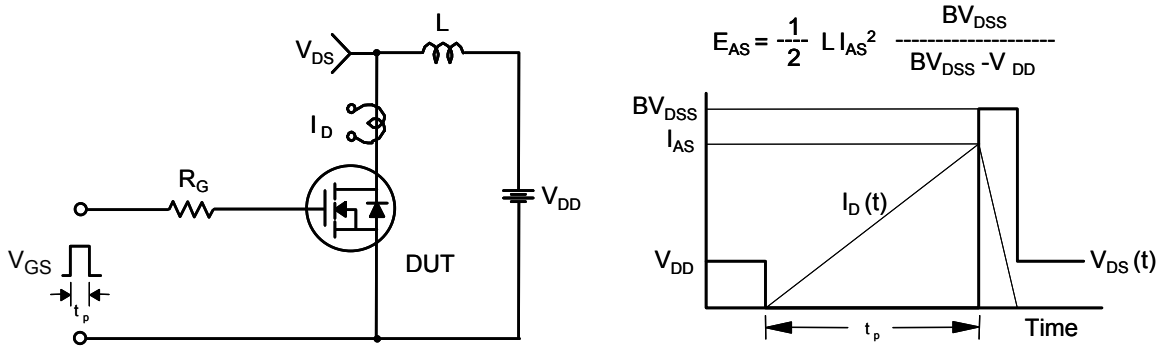


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

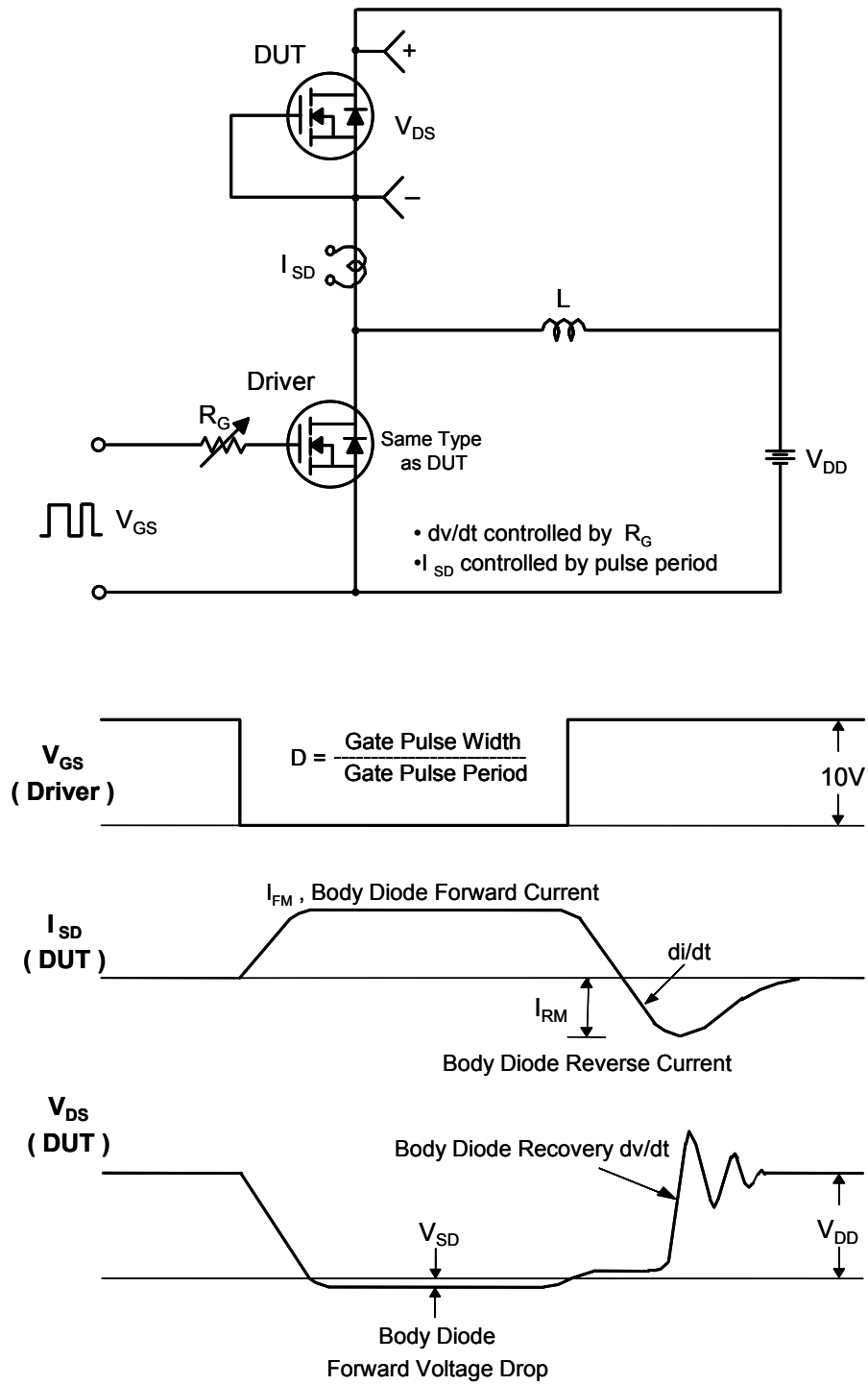
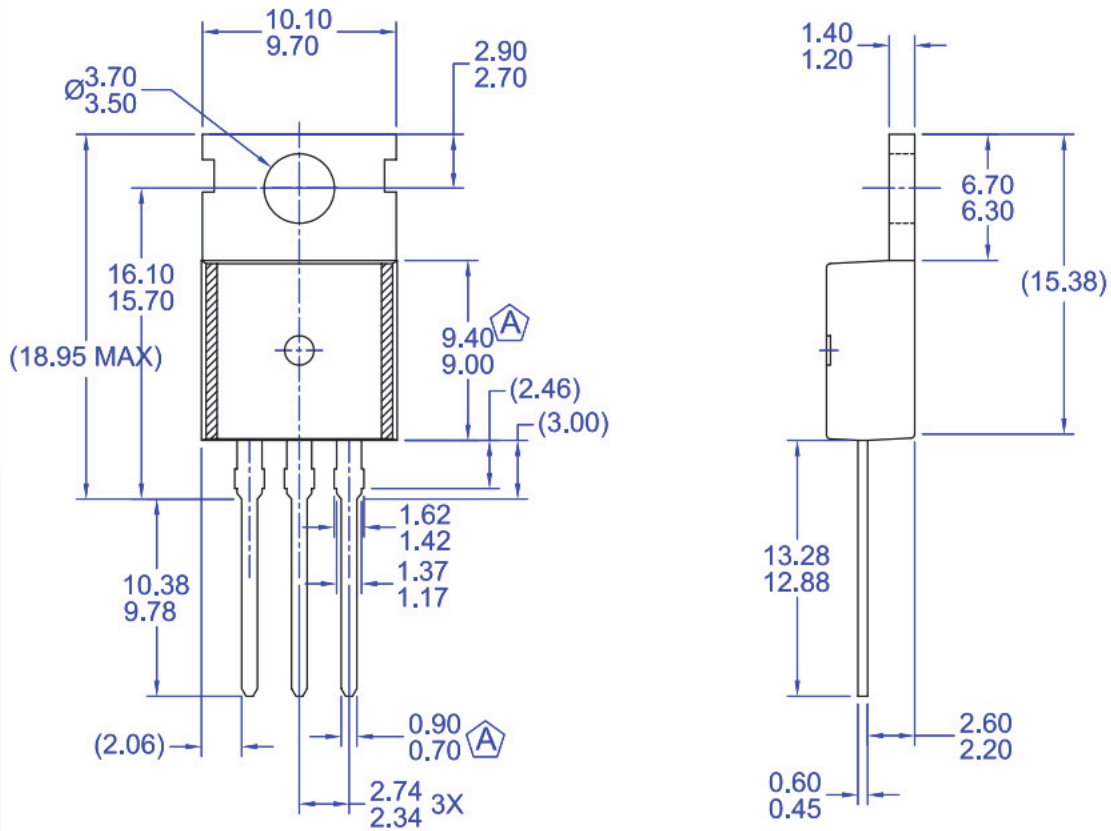


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- Ⓐ CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

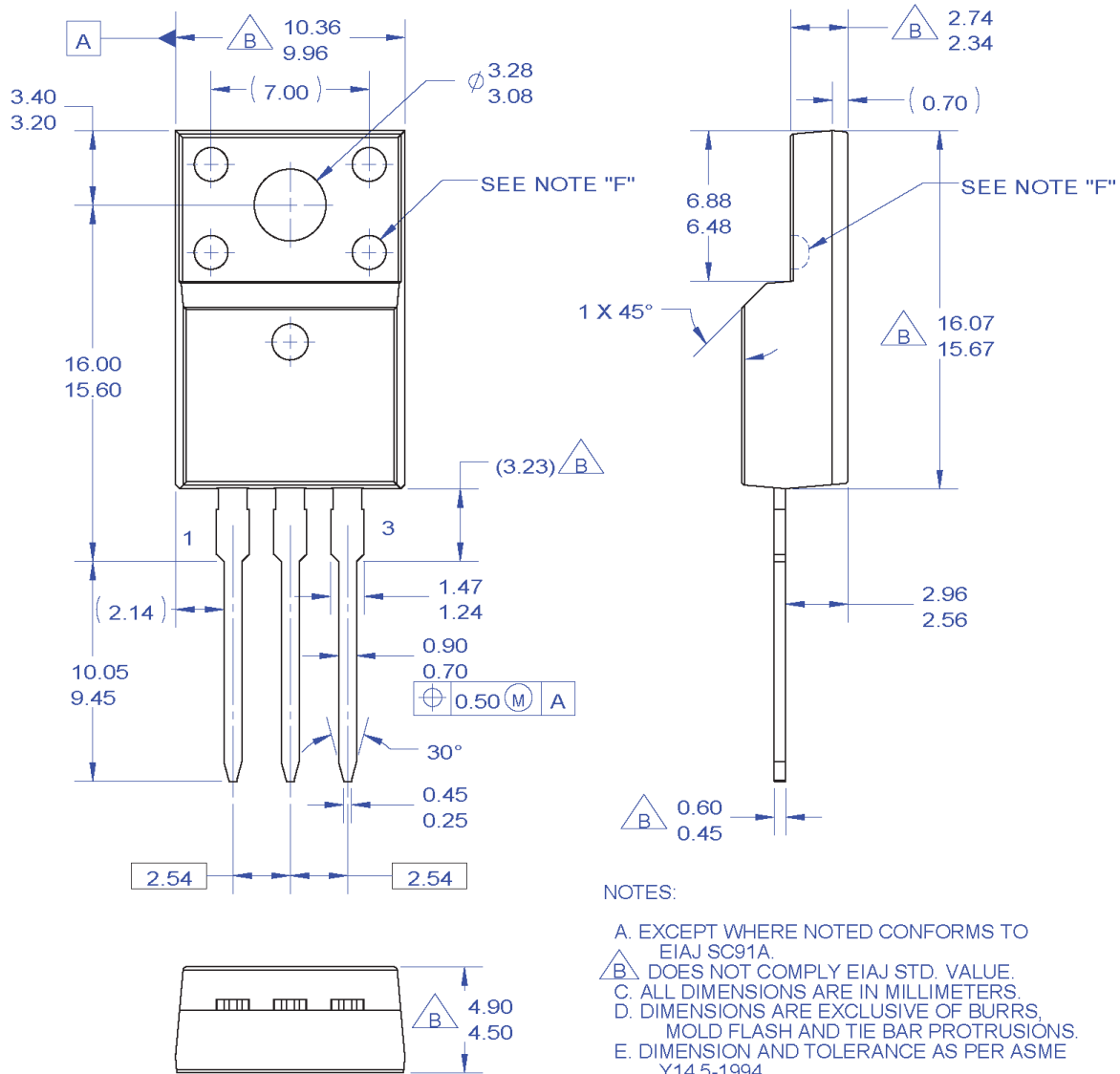
Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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Mechanical Dimensions



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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