

FDR840P

P-Channel 2.5V Specified PowerTrench® MOSFET

General Description

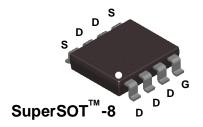
This P-Channel 2.5V specified MOSFET uses a rugged gate PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V-12V).

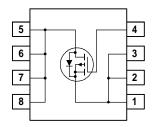
Applications

- · Power management
- · Load switch
- Battery protection

Features

- -10 A, -20 V. $R_{DS(ON)} = 0.011~\Omega$ @ $V_{GS} = -4.5~V$ $R_{DS(ON)} = 0.016~\Omega$ @ $V_{GS} = -2.5~V$
- Fast switching speed.
- High performance trench technology for extremely low $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability.





Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V_{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		± 12	V
I _D	Drain Current - Continuous	(Note 1a)	-10	А
	– Pulsed		-50	
P _D	Power Dissipation for Single Operation	(Note 1a)	1.8	W
		(Note 1b)	1.0	
		(Note 1c)	0.9	
T _J , T _{STG}	Operating and Storage Junction Tempera	ture Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

Package Marking and Ordering Information

Device Marking	Device Marking Device		Tape width	Quantity	
FDR840P	FDR840P	13"	12mm	2500 units	

Symbol	Parameter	Min	Тур	Max	Units	
Off Char	acteristics		· I			ı
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-20			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$,Referenced to 25°C		-12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I _{GSSF}	Gate-Body Leakage, Forward	V _{GS} = 12 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V}$ $V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.6	-0.8	-1.5	٧
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$\begin{split} V_{GS} = -4.5 \ V, & I_D = -10 \ A \\ V_{GS} = -2.5 \ V, & I_D = -8.4 \ A \\ V_{GS} = -4.5 \ V, I_D = -10A, \ T_J = 125^{\circ}C \end{split}$		9 12 12	11 16 17	mΩ
I _{D(on)}	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, \qquad V_{DS} = -5 \text{ V}$	-50			Α
g FS	Forward Transconductance	$V_{DS} = -10 \text{ V}, \qquad I_{D} = -10 \text{ A}$		49		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$		4481		pF
Coss	Output Capacitance	f = 1.0 MHz		1532		pF
C _{rss}	Reverse Transfer Capacitance			540		pF
Switchin	g Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -5 \text{ V}, \qquad I_{D} = -1 \text{ A},$		15	30	ns
t _r	Turn-On Rise Time	$V_{DD} = -5 \text{ V}, \qquad I_{D} = -1 \text{ A}, \\ V_{GS} = -4.5 \text{ V}, \qquad R_{GEN} = 6 \Omega$		15	30	ns
t _{d(off)}	Turn-Off Delay Time			120	240	ns
t _f	Turn-Off Fall Time			60	120	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, \qquad I_{D} = -10 \text{ A},$		41	60	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$		6.4		nC
Q _{gd}	Gate-Drain Charge			11.8		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Sourc	_			-1.5	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -1.5 \text{ A} \text{(Note 2)}$		-0.65	-1.2	V

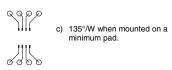
^{1.} R_{BJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 70°/W when mounted on a 1in² pad of 2 oz copper



b) 125°/W when mounted on a .04 in² pad of 2 oz copper



Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu s$, Duty Cycle < 2.0%

Typical Characteristics

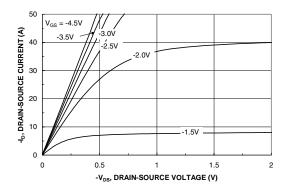


Figure 1. On-Region Characteristics.

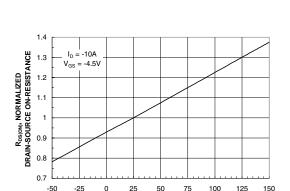


Figure 3. On-Resistance Variation with Temperature.

T_J, JUNCTION TEMPERATURE (°C)

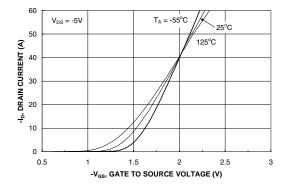


Figure 5. Transfer Characteristics.

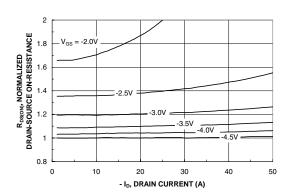


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

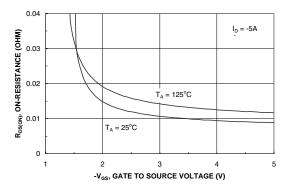


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

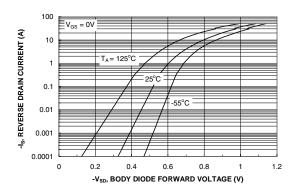
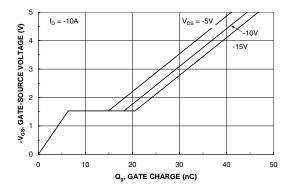


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



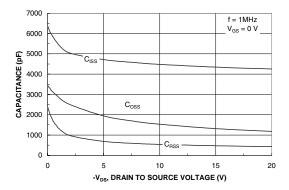


Figure 7. Gate Charge Characteristics.

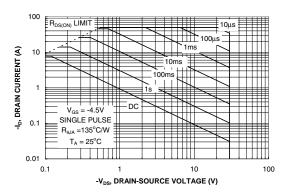


Figure 8. Capacitance Characteristics.

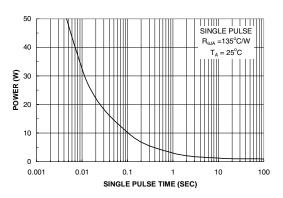


Figure 9. Maximum Safe Operating Area.



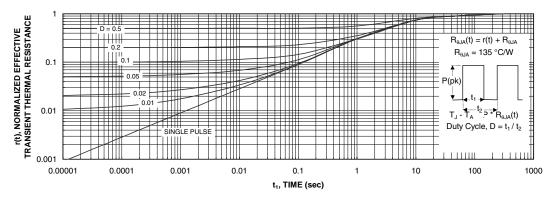
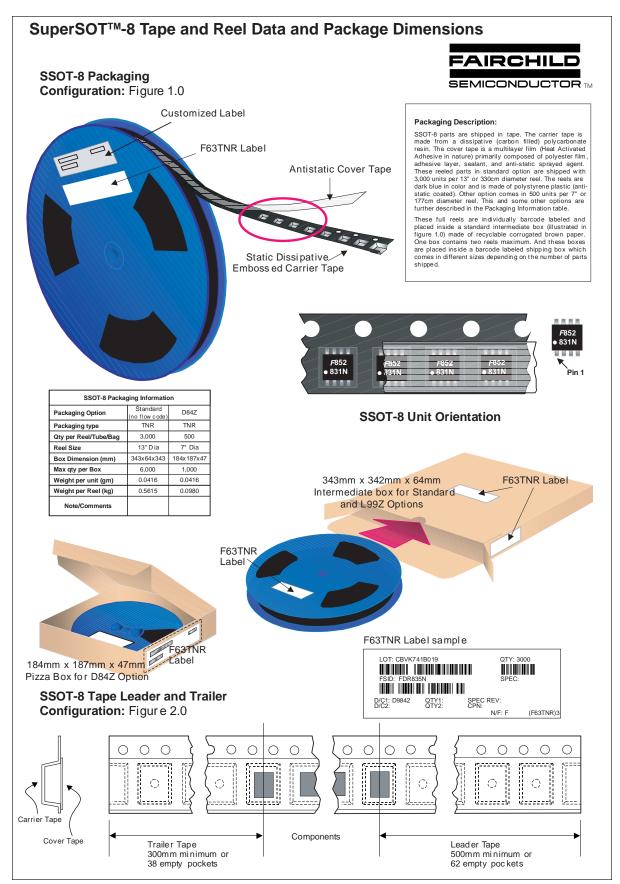
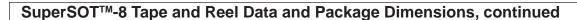


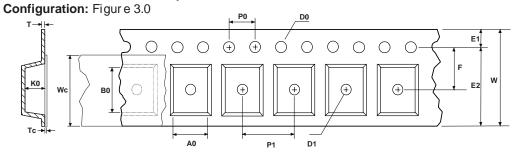
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.





SSOT-8 Embossed Carrier Tape



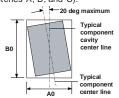


	Dimensions are in millimeter													
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
SSOT-8 (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

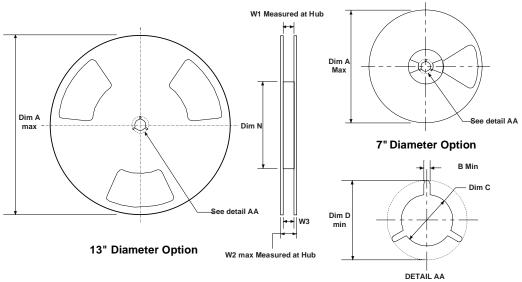


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

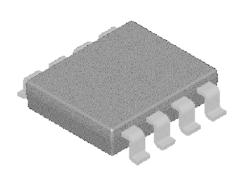
SSOT-8 Reel Configuration: Figur e 4.0

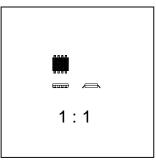


	Dimensions are in inches and millimeters								
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-8 (FS PKG Code 34, 35)

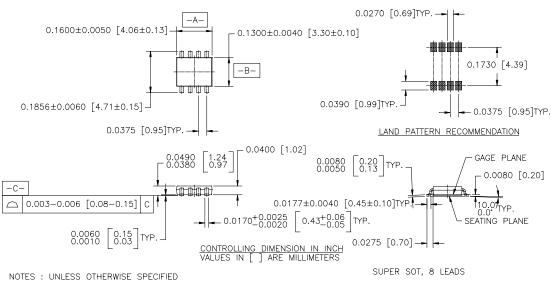




Scale 1:1 on letter size paper

Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 0.0416



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