

# FDS4410A

## Single N-Channel, Logic-Level, PowerTrench® MOSFET

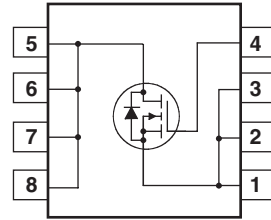
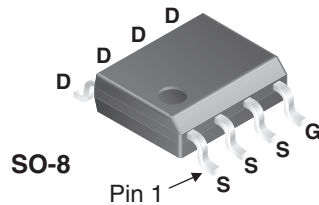
### Features

- 10 A, 30 V.  $R_{DS(ON)} = 13.5\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(ON)} = 20\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability

### General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	10	A
		50	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	2.5	W
		1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$
<b>Thermal Characteristics</b>			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	50	$^\circ\text{C/W}$
		125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	

### Package Marking and Ordering Information

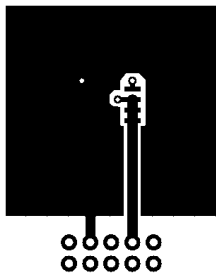
Device Marking	Device	Reel Size	Tape width	Quantity
FDS4410A	FDS4410A	13"	12mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		25		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		–5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		9.8	13.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		12.0	20	
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}, T_J = 125^\circ\text{C}$		13.7	23	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	50			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		48		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		1205		pF
$C_{oss}$	Output Capacitance			290		
$C_{rss}$	Reverse Transfer Capacitance			115		
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.4		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DS} = 15\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		9	19	ns
$t_r$	Turn–On Rise Time			5	10	
$t_{d(off)}$	Turn–Off Delay Time			28	44	
$t_f$	Turn–Off Fall Time			9	19	
$Q_g$	Total Gate Charge	$V_{DD} = 15\text{ V}, I_D = 10\text{ A}, V_{GS} = 5\text{ V}$		12	16	nC
$Q_{gs}$	Gate–Source Charge			3.4		
$Q_{gd}$	Gate–Drain Charge			4.0		
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.1	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.74	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 10\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$		24		nS
$Q_{rr}$	Diode Reverse Recovery Charge			27		

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

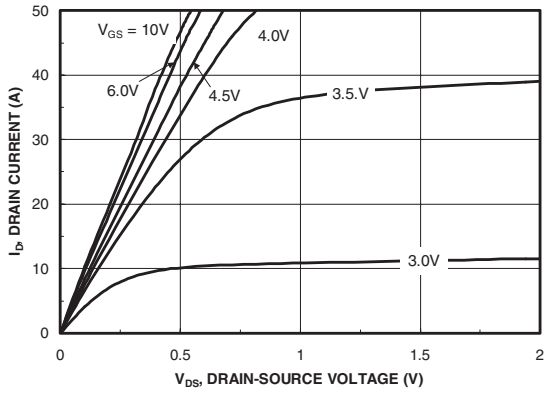


Figure 1. On-Region Characteristics.

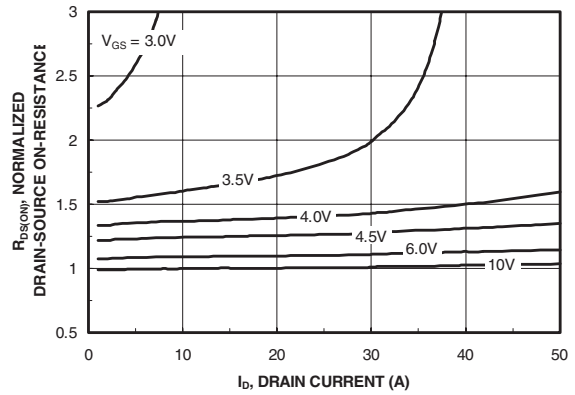


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

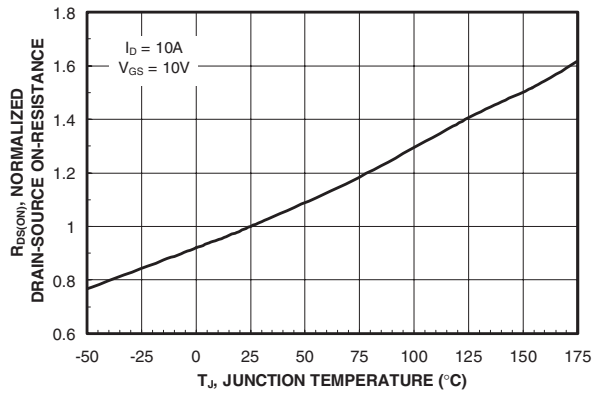


Figure 3. On-Resistance Variation with Temperature.

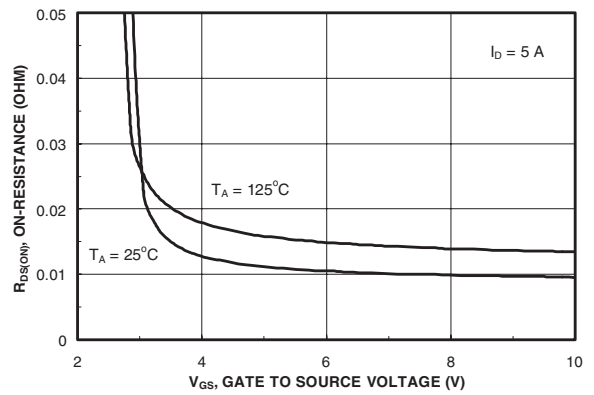


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

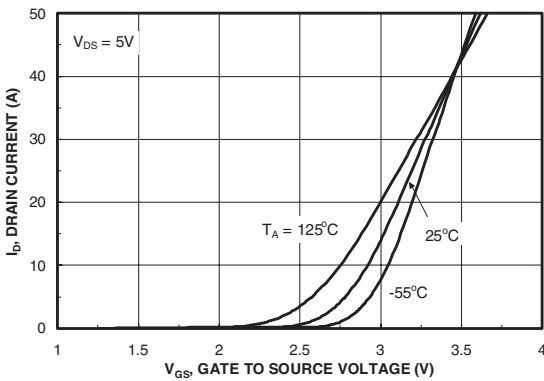


Figure 5. Transfer Characteristics.

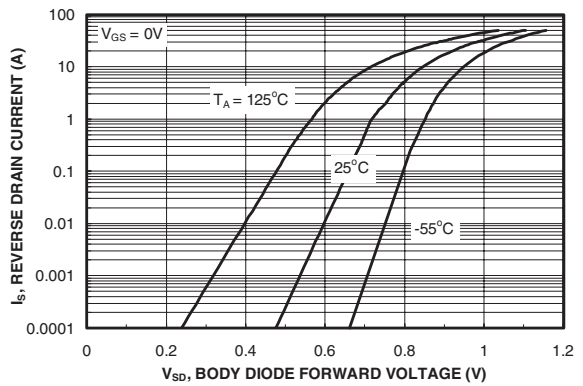
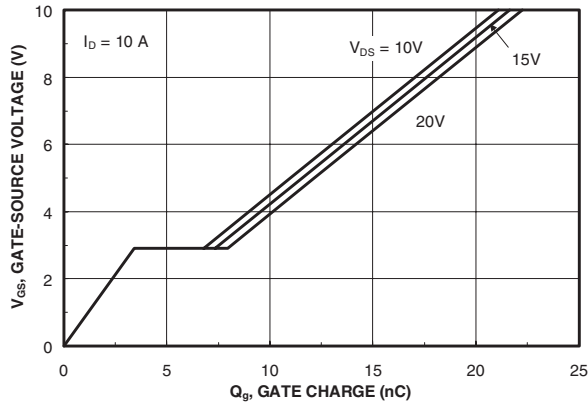
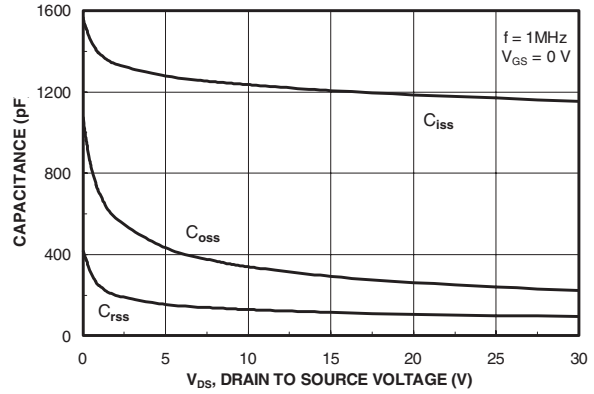


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

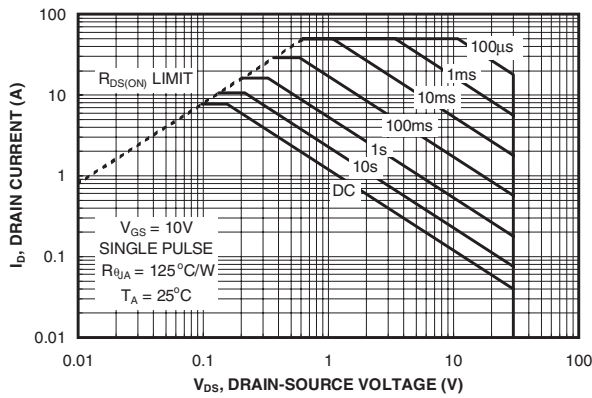
### Typical Characteristics



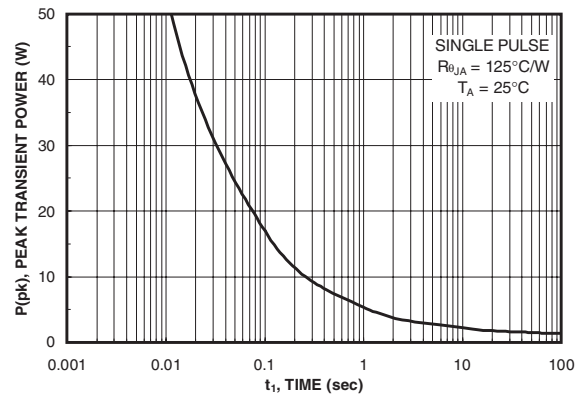
**Figure 7. Gate Charge Characteristics.**



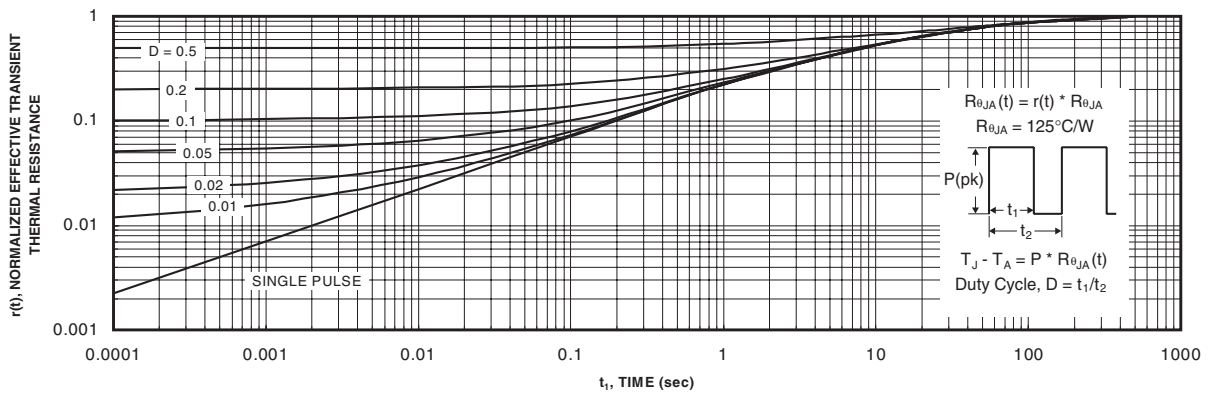
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

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