ON

oN Semiconductor® FDS4435BZ-F085

P-Channel PowerTrench[®] MOSFET -30V, -8.8A, 20m Ω

Features

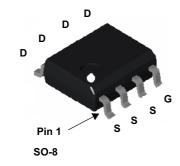
- Max $r_{DS(on)}$ = 20m Ω at V_{GS} = -10V, I_D = -8.8A
- Max $r_{DS(on)}$ = 35m Ω at V_{GS} = -4.5V, I_D = -6.7A
- Extended V_{GSS} range (-25V) for battery applications
- HBM ESD protection level of ±3.8KV typical (note 3)
- High performance trench technology for extremely low r_{DS(on)}
- High power and current handling capability

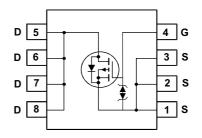
 Termination is Lead-free and RoHS compliant Qualified to AEC Q101



using ON Semiconductor's advanced PowerTrench[®] process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

This P-Channel MOSFET is produced





General Description

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

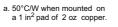
Symbol		Р	Ratings		Units			
V _{DS}	Drain to	Source Voltage	-30		V			
V _{GS}	Gate to	Gate to Source Voltage						V
I _D	Drain C	T _A = 2	T _A = 25°C (Note 1a)		-8.8			
		-Pulsed				-50		A
P _D	Power Dissipation T			25°C	(Note 1a)	2.5		- w
	Power I	Dissipation	T _A = 25°C (Note 1b) 1.0					
E _{AS}	Single Pulse Avalanche Energy (Note 4)					24		mJ
T _J , T _{STG}	Operating and Storage Junction Temperature Range					-55 to +150		°C
Thermal Cł _{R_{өjc}}		istics Il Resistance, Junction to C	ase			25		
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)					50		°C/W
[•] ackage M	arking a	and Ordering Informa	ition					
Device Marking		Device	Package	Re	eel Size	Tape Width	Qua	ntity
FDS4435BZ		FDS4435BZ-F085	SO-8		13"	12mm	2500	Ounits

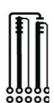
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Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-30			V
ΔBV _{DSS} ΔTJ	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu$ A, referenced to 25°C		-21		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V			1	μA
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$			±10	μA
On Chara	cteristics				<u>.</u>	
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-1	-2.1	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$, referenced to $25^{\circ}C$		6		mV/°C
r _{DS(on)}		V _{GS} = -10V, I _D = -8.8A		16	20	
	Static Drain to Source On Resistance	V _{GS} = -4.5V, I _D = -6.7A		26	35	mΩ
		V _{GS} = -10V, I _D = -8.8A, T _J = 125°C		22	28	1
9 _{FS}	Forward Transconductance	V _{DS} = -5V, I _D = -8.8A		24		S
C _{iss} C _{oss}	Characteristics Input Capacitance Output Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1MHz		1385 275	1845 365	pF pF
C _{rss}	Reverse Transfer Capacitance	t = 1MHz		230	345	pF
R _g	Gate Resistance	f = 1MHz		4.5		Ω
-	g Characteristics					
t _{d(on)}	Turn-On Delay Time			10	20	ns
t _r	Rise Time	$V_{DD} = -15V, I_D = -8.8A,$		6	12	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = -10V, R_{GEN} = 6 Ω		30	48	ns
t _f	Fall Time			12	22	ns
Qg	Total Gate Charge	$\frac{V_{GS} = 0V \text{ to } -10V}{V_{GS} = 0V \text{ to } -5V} V_{DD} = -15V, I_D = -8.8A$		28	40	nC
Q _g	Total Gate Charge	$V_{GS} = 0V \text{ to } -5V$ $V_{DD} = -15V,$		16	23	nC
Q _{gs}	Gate to Source Charge	I _D 0.0A		5.2		nC
Q _{gd}	Gate to Drain "Miller" Charge			7.4		nC
Drain-Sou	urce Diode Characteristics					
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0V, I _S = -8.8A (Note 2)		-0.9	-1.2	V
t _{rr}	Reverse Recovery Time			29	44	ns
Q _{rr}	Reverse Recovery Charge	— I _F = -8.8A, di/dt = 100A/μs		23	35	nC

the user's board design.







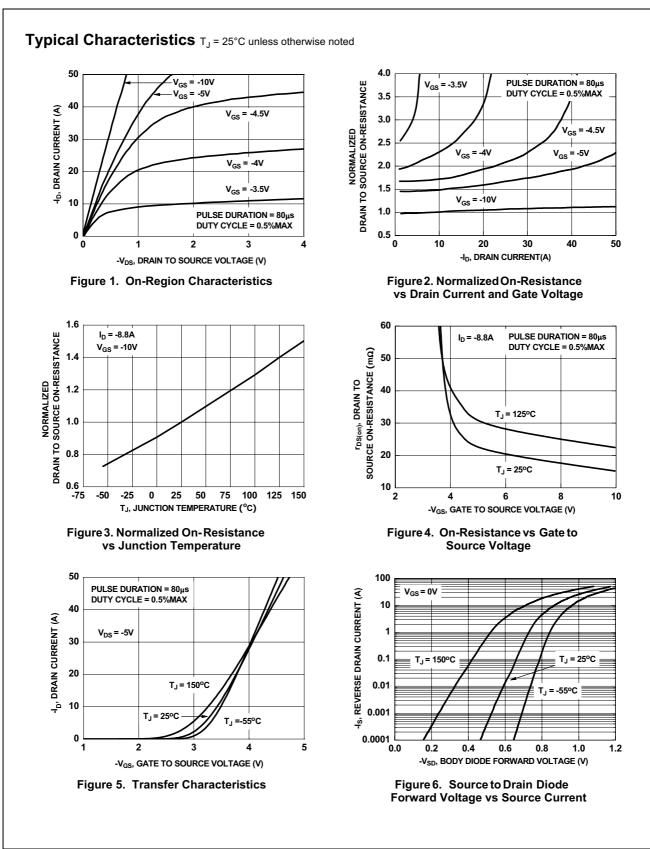
b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μ s, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

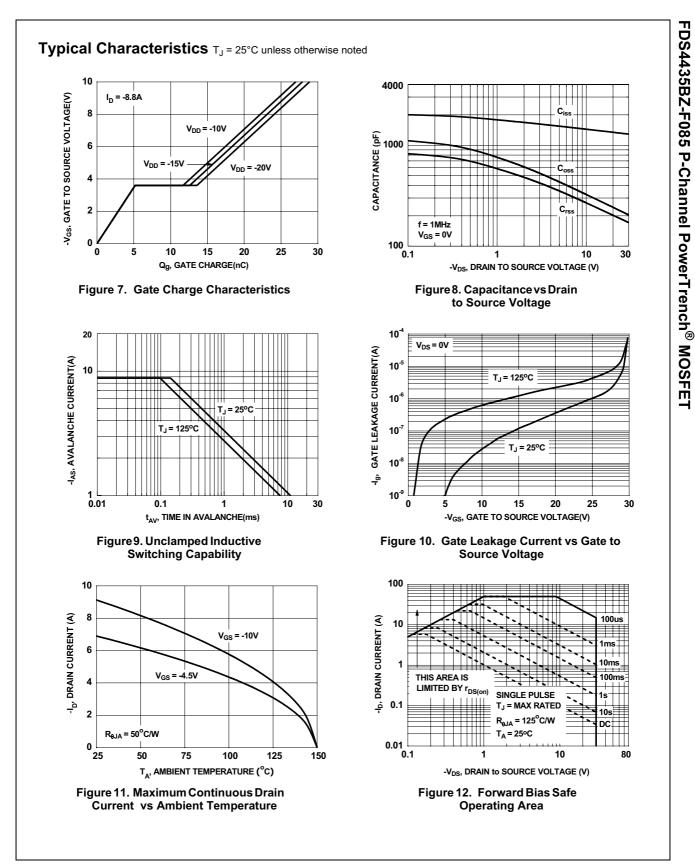
4. Starting T_J = 25°C, L = 1mH, I_{AS} = -7A, V_{DD} = -30V, V_{GS} = -10V

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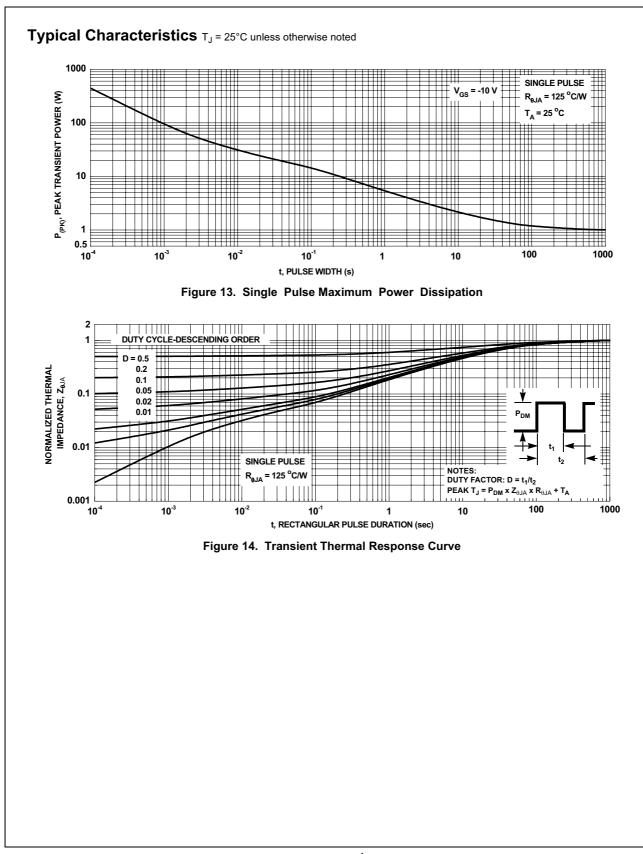


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