FAIRCHILD SEMICONDUCTOR™

May 2008

# FDS6984AS

## Dual Notebook Power Supply N-Channel PowerTrench® SyncFET™

### General Description

The FDS6 984AS is designed t o replace t wo single SO-8 MOS FETs and Schottk y diode in s ynchronous DC:DC p ower supplies that prov ide various perip heral voltages for not ebook computer s and oth er battery powered electro nic devices . FDS6984AS contains tw o unique 30V, N-channel, logic level, PowerT rench MOSFETs designed to maximi ze pow er conversion efficiency.

The high-side sw itch ( Q1) is designed w ith sp ecific emphasis on reducing sw itching losse s w hile th e low-side sw itch (Q2 ) is optimized t o reduce condu ction losses. Q2 also includes a pate nted combination of a MOSFET mono lithically integrat ed w ith a Schottk y diode.

### Features

- **Q2**: Optimized to minimize conduction losses Includes SyncFET Schottky diode

  8.5A, 30V $R_{DS(on)}$ max= 20 mΩ @ $V_{GS}$ = 10V

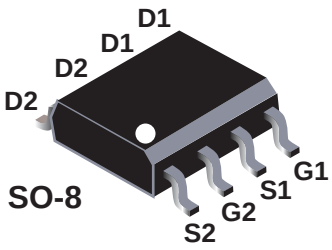
  $R_{DS(on)}$ max= 28 mΩ @ $V_{GS}$ = 4.5V

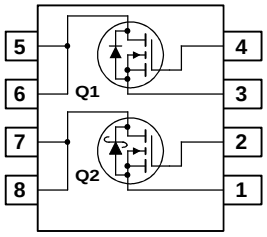
- **Q1**: Optimized for low switching losses Low gate charge (8nC typical)

  5.5A, 30V $R_{DS(on)}$ max= 31 mΩ @ $V_{GS}$ = 10V

  $R_{DS(on)}$ max= 40 mΩ @ $V_{GS}$ = 4.5V

- RoHS Compliant




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Q2 | Q1 | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 8.5 | 5.5 | A |
| | - Pulsed | | 30 | 20 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2 | | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | | |
| | | (Note 1b) | 1 | | |
| | | (Note 1c) | 0.9 | | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS6984AS | FDS6984AS | 13” | 12mm | 2500 units |

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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter Test | Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA<br>$V_{GS}$ = 0 V, $I_D$ = 250 µA | Q2<br>Q1 | 30<br>30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | Q2<br>Q1 | | | 500<br>1 | µA |
| | | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V, $T_J$ = 125°C | Q2 | | 2.3 | | mA |
| | | | Q1 | 79 | | | nA |
| $I_{GSS}$ Gate-B | ody Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | All | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA<br>$V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | Q2<br>Q1 | 1<br>1 | 1.7<br>1.8 | 3<br>3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 1 mA, Referenced to 25°C<br>$I_D$ = 250 uA, Referenced to 25°C | Q2<br>Q1 | –3 | <br>–4 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 8.5 A<br>$V_{GS}$ = 10 V, $I_D$ = 8.5 A, $T_J$ = 125°C<br>$V_{GS}$ = 4.5 V, $I_D$ = 7 A | Q2 | 17 | <br>24<br>21 | 20<br>32<br>28 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 5.5 A<br>$V_{GS}$ = 10 V, $I_D$ = 5.5 A, $T_J$ = 125°C<br>$V_{GS}$ = 4.5 V, $I_D$ = 4.6 A | Q1 | | 26<br>34<br>32 | 31<br>43<br>40 | |
| $I_{D(on)}$ On-Stat | e Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | Q2<br>Q1 | 30<br>20 | | | A |
| $g_{FS}$ For | ward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 8.5 A<br>$V_{DS}$ = 5 V, $I_D$ = 5.5 A | Q2<br>Q1 | 25 | <br>18 | S | |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ Input | Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | Q2<br>Q1 | 530 | <br>420 | pF | |
| $C_{oss}$ Output | Capacitance | | Q2<br>Q1 | 170 | <br>120 | pF | |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q2<br>Q1 | 60 | <br>50 | pF | |
| $R_G$ Gate | Resistance | $V_{GS}$ = 15mV, f = 1.0 MHz | Q2<br>Q1 | 3.1 | <br>2.2 | | Ω |

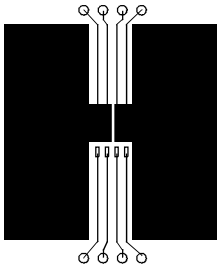
## Electrical Characteristics (continued)

$T_A$ = 25°C unless otherwise noted

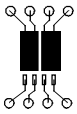
| Symbol | Parameter Test | Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Switching Characteristics** (Note 2) | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10V, $R_{GEN}$ = 6 Ω | Q2 | 8 | | 16 | ns |
| | | | Q1 | | 9 | 18 | |
| $t_r$ Turn | -On Rise Time | | Q2 | 5 | | 10 | ns |
| | | | Q1 | | 6 | 12 | |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q2 | 23 | | 37 | ns |
| | | | Q1 | | 22 | 35 | |
| $t_f$ Turn | -Off Fall Time | | Q2 | 4 | | 8 | ns |
| | | | Q1 | | 2 | 4 | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 4.5V, $R_{GEN}$ = 6 Ω | Q2 | 9 | | 18 | ns |
| | | | Q1 | | 10 | 19 | |
| $t_r$ Turn | -On Rise Time | | Q2 | 7 | | 14 | ns |
| | | | Q1 | | 11 | 20 | |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q2 | 13 | | 24 | ns |
| | | | Q1 | | 13 | 24 | |
| $t_f$ Turn | -Off Fall Time | | Q2 | 4 | | 8 | ns |
| | | | Q1 | | 3 | 6 | |
| $Q_{g(TOT)}$ | Total Gate Charge, Vgs = 10V | Q2: $V_{DS}$ = 15 V, $I_D$ = 8.5 A; Q1: $V_{DS}$ = 15 V, $I_D$ = 5.5 A | Q2 | 10 | | 14 | nC |
| | | | Q1 | | 8 | 11 | |
| $Q_g$ | Total Gate Charge, Vgs = 5V | | Q2 | 5 | | 8 | nC |
| | | | Q1 | | 4 | 6 | |
| $Q_{gs}$ Gate-S | ource Charge | | Q2 | 1.5 | | nC | |
| | | | Q1 | | 1.3 | | |
| $Q_{gd}$ Gate- | Drain Charge | | Q2 | 1.9 | | nC | |
| | | | Q1 | | 1.5 | | |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | Q2 | | | 3.0 | A |
| | | | Q1 | | | 1.3 | |
| $t_{rr}$ Rever | se Recovery Time | $I_F$ = 10A, $dI_F/dt$ = 300 A/µs (Note 3) | Q2 | | 13 | ns | |
| $Q_{rr}$ | Reverse Recovery Charge | | | | 6 | | nC |
| $t_{rr}$ Rever | se Recovery Time | $I_F$ = 5.5A, $dI_F/dt$ = 100 A/µs (Note 3) | Q1 | | 17 | ns | |
| $Q_{rr}$ | Reverse Recovery Charge | | | | 6 | | nC |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.3 A (Note 2) | Q2 | 0.6 | | 0.7 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2) | Q1 | | 0.8 | 1.2 | |

**Notes:**

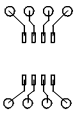
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C /W when mounted on a 0.5in$^2$ pad of 2 oz copper



b) 125°C /W when mounted on a 0.02 in$^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** See "SyncFET Schottky body diode characteristics" below.

**3.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics: Q2

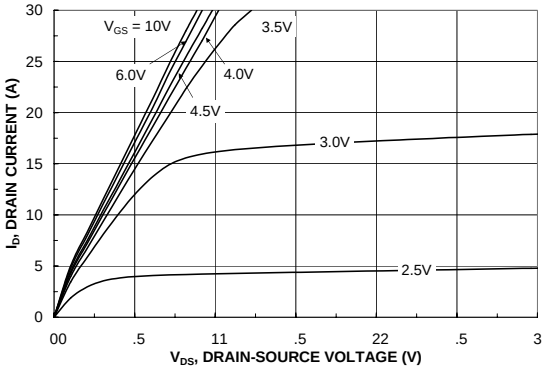



**Figure 1. On-Region Characteristics.**

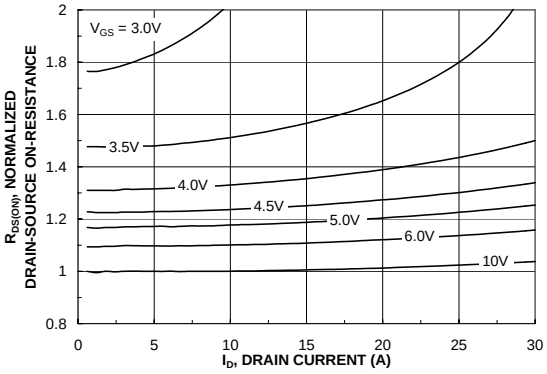



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

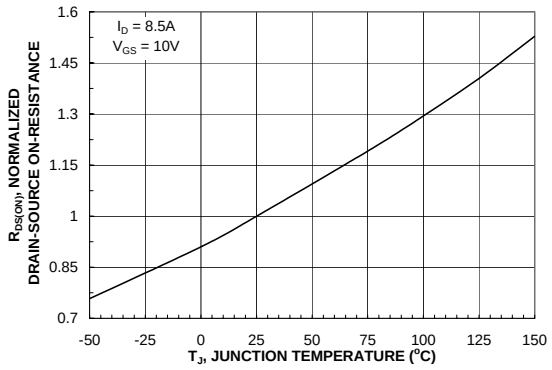



**Figure 3. On-Resistance Variation with Temperature.**

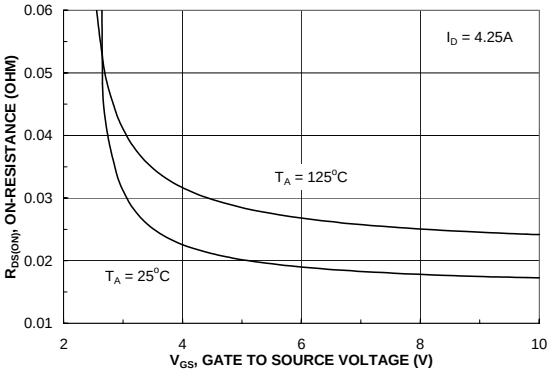



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

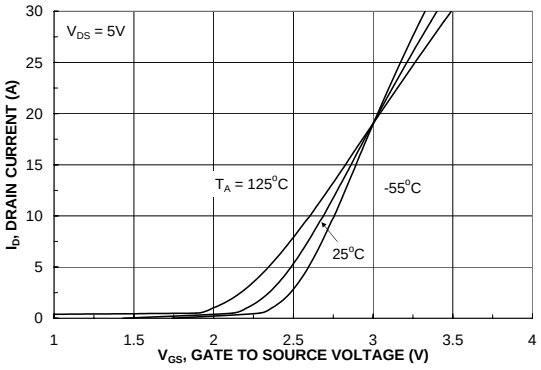



**Figure 5. Transfer Characteristics.**

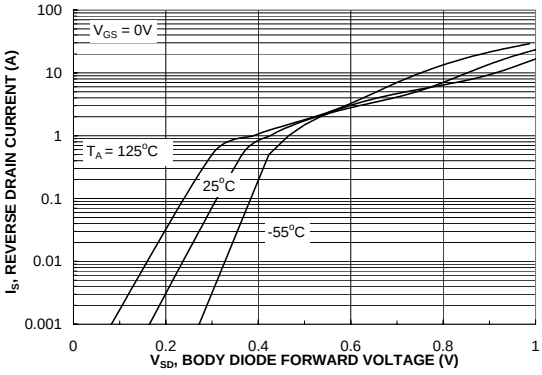



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: Q2

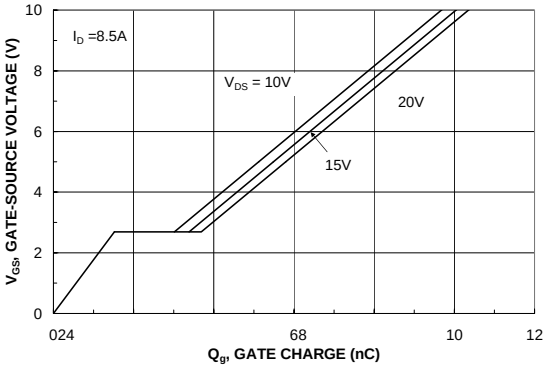



**Figure 7. Gate Charge Characteristics.**

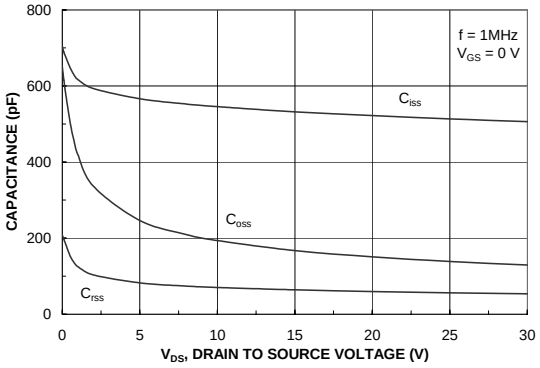



**Figure 8. Capacitance Characteristics.**

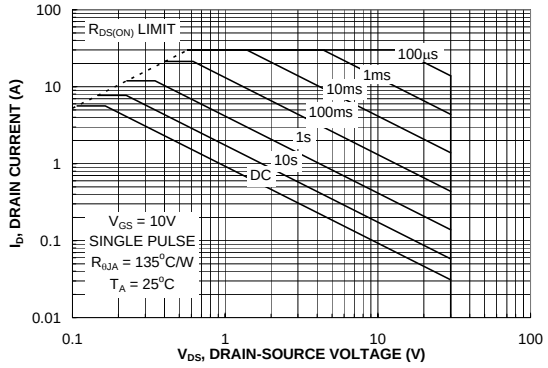



**Figure 9. Maximum Safe Operating Area.**

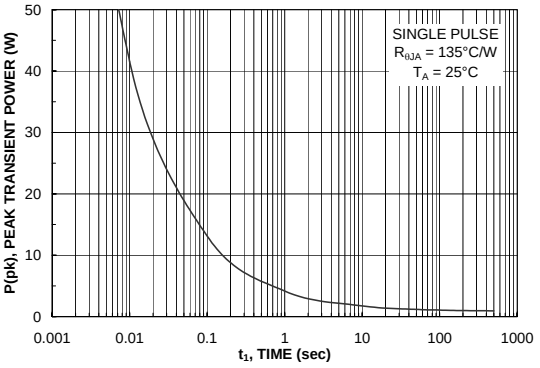



**Figure 10. Single Pulse Maximum Power Dissipation.**

## Typical Characteristics Q1

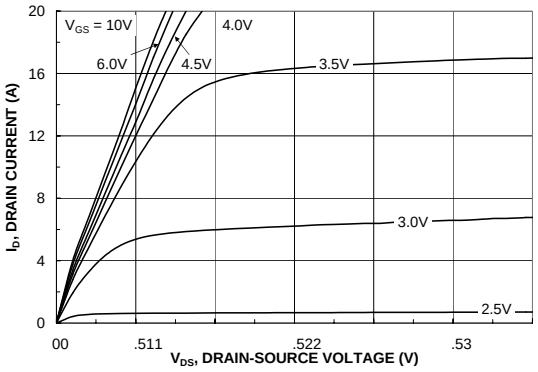



**Figure 11. On-Region Characteristics.**

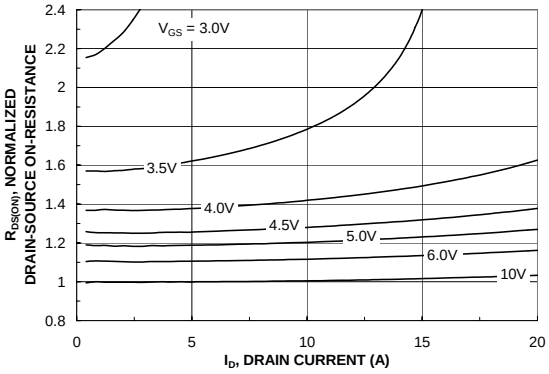



**Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.**

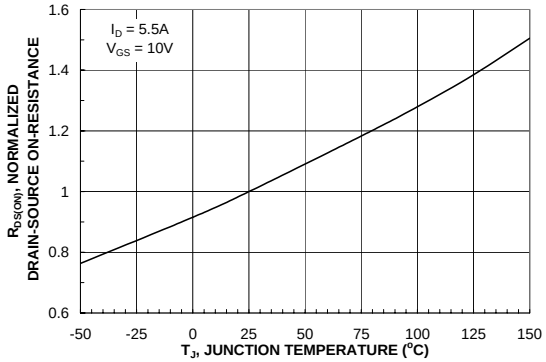



**Figure 13. On-Resistance Variation with Temperature.**

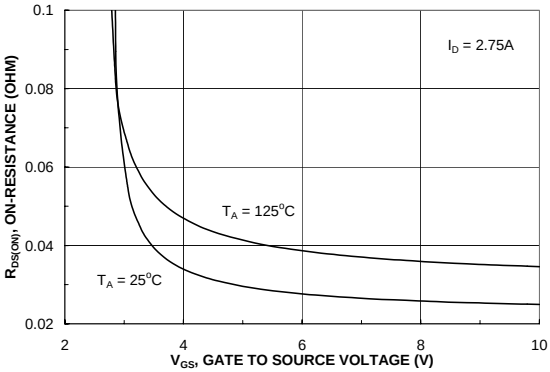



**Figure 14. On-Resistance Variation with Gate-to-Source Voltage.**

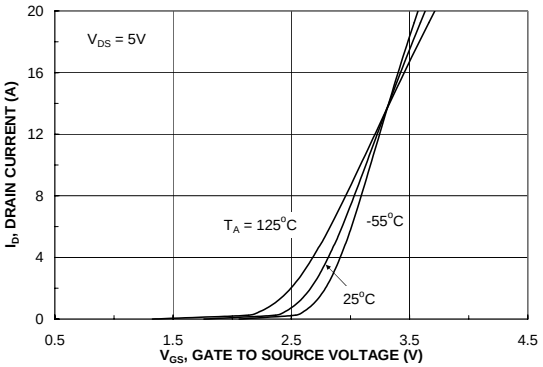



**Figure 15. Transfer Characteristics.**

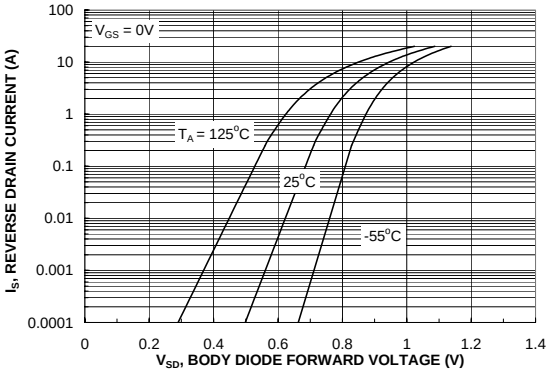



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics Q1

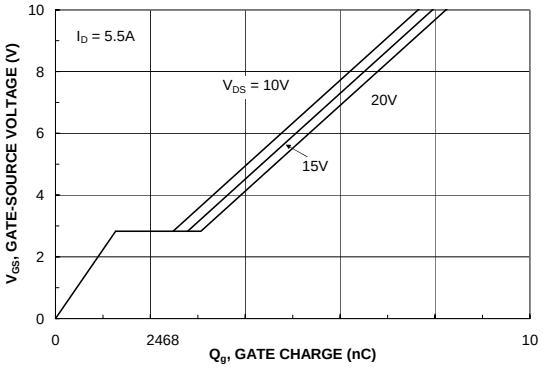



**Figure 17. Gate Charge Characteristics.**

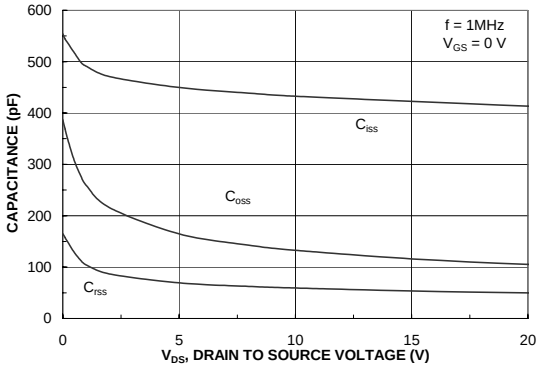



**Figure 18. Capacitance Characteristics.**

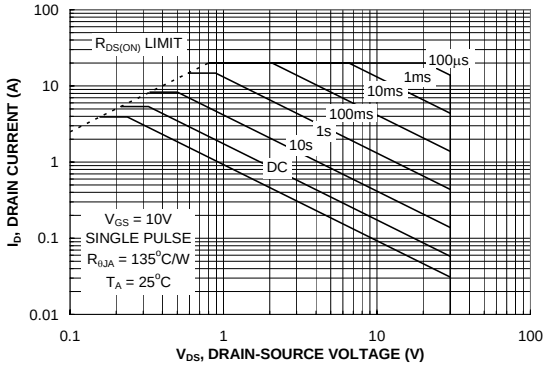



**Figure 19. Maximum Safe Operating Area.**

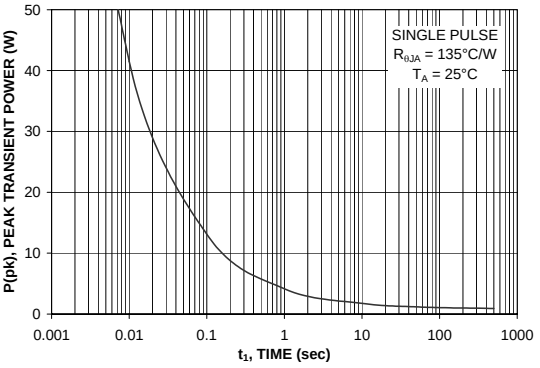



**Figure 20. Single Pulse Maximum Power Dissipation.**

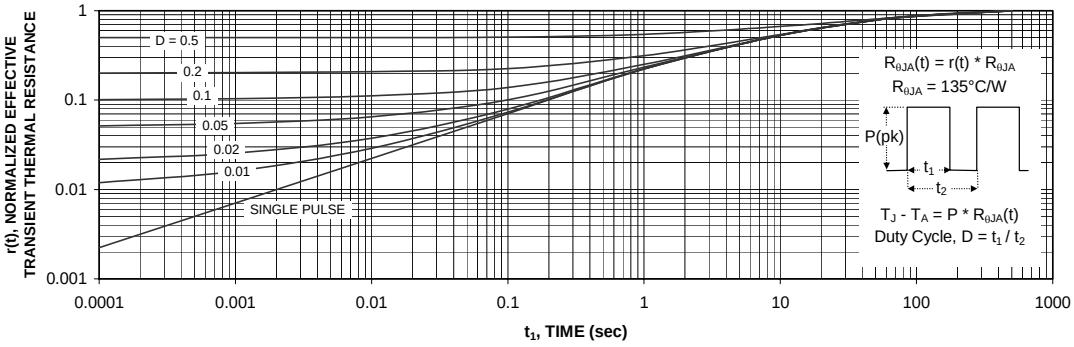



**Figure 21. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

## Typical Characteristics (continued)

### SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 22 shows the reverse recovery characteristic of the FDS6984AS.

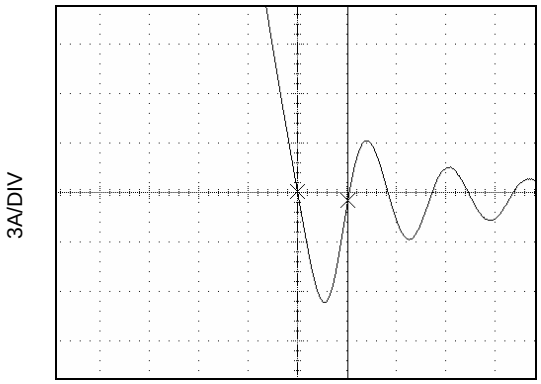



**Figure 22. FDS6984AS SyncFET body diode reverse recovery characteristic.**

For comparison purposes, Figure 23 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6984A).

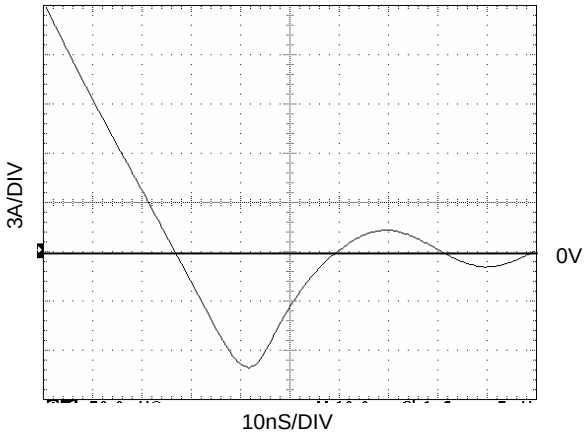



**Figure 23. Non-SyncFET (FDS6984A) body diode reverse recovery characteristic.**

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

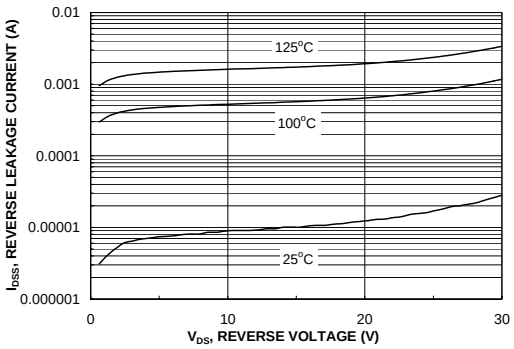



**Figure 24. SyncFET body diode reverse leakage versus drain-source voltage and temperature.**

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GTO™
IntelliMAX™
ISOPLANAR™
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MillerDrive™
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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

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