

May 2013

# **FDS8813NZ**

# N-Channel PowerTrench® MOSFET 30V, 18.5A, 4.5m $\Omega$

### **Features**

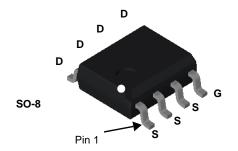
- Max  $r_{DS(on)} = 4.5 \text{m}\Omega$  at  $V_{GS} = 10 \text{V}$ ,  $I_D = 18.5 \text{A}$
- Max  $r_{DS(on)} = 6.0 m\Omega$  at  $V_{GS} = 4.5 V$ ,  $I_D = 16 A$
- HBM ESD protection level of 5.6KV typical (note 3)
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability
- RoHS compliant

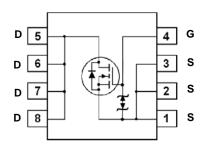


# **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.





# **MOSFET Maximum Ratings** $T_A = 25$ °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DS</sub>	Drain to Source Voltage		30	V
$V_{GS}$	Gate to Source Voltage		±20	V
	Drain Current -Continuous	(Note 1a)	18.5	^
I <sub>D</sub>	-Pulsed		74	A
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 4)	337	mJ
D	Power Dissipation (No		2.5	W
$P_{D}$	Power Dissipation	(Note 1b)	1.0	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	25	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	125	

# **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS8813NZ	FDS8813NZ	13" 12mm		2500 units

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to 25°C		20		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24V,  V_{GS} = 0V$			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			±10	μΑ

# On Characteristics (Note 2)

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$ , referenced to 25°C		-6		mV/°C
	$V_{GS} = 10V, I_D = 18.5A$		3.8	4.5		
rno( )	Static Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 16A$		4.7	6.0	mΩ
r <sub>DS(on)</sub> Static Drain to Source On Resistance		$V_{GS} = 10V$ , $I_D = 18.5A$ , $T_J = 125$ °C		5.1	6.6	11122
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5V, I_{D} = 18.5A$		74		S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	45)/ )/ 0)/		3115	4145	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1MHz$		580	775	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 11/11/2		345	520	pF
$R_g$	Gate Resistance	f = 1MHz	0.1	1.8	5.6	Ω

# **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time				13	24	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 15V, I_D = 18$	$V_{DD} = 15V, I_{D} = 18.5A$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		8	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	v <sub>GS</sub> = 10V, R <sub>GEN</sub>			39	63	ns
t <sub>f</sub>	Fall Time				7	14	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0V \text{ to } 10V$	V <sub>DD</sub> = 15V		55	76	nC
Qg	Total Gate Charge	$V_{GS} = 0V \text{ to } 5V$	$I_D = 18.5A$		28	40	nC
$Q_{gs}$	Gate to Source Gate Charge		_		9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				10		nC

# **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 2.1A$ (Note 2)		0.7	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 18.5A, di/dt = 100A/μs		32	47	ns
Q <sub>rr</sub>	Reverse Recovery Charge			27	41	nC

1. R<sub>BJA</sub> is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BJC</sub> is guaranteed by design while R<sub>BJA</sub> is determined by the user's board design.



a) 50°C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a

- 2. Pulse Test: Pulse Width < 300 us, Duty Cycle < 2%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
   Starting T<sub>J</sub> = 25°C, L = 3mH, I<sub>AS</sub> = 15A, V<sub>DD</sub> = 30V, V<sub>GS</sub> = 10V.

# Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

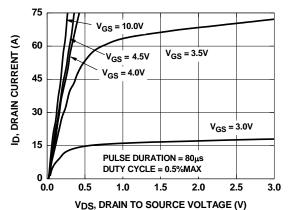


Figure 1. On-Region Characteristics

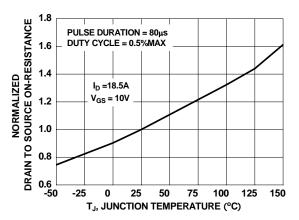


Figure 3. Normalized On-Resistance vs Junction Temperature

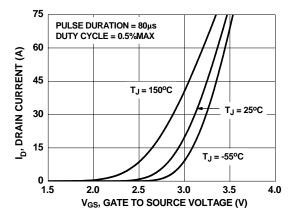


Figure 5. Transfer Characteristics

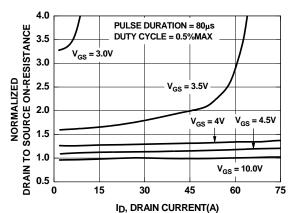


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

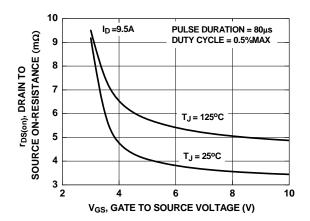


Figure 4. On-Resistance vs Gate to Source Voltage

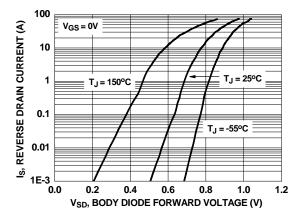


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

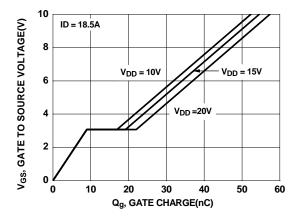


Figure 7. Gate Charge Characteristics

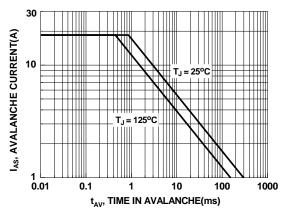


Figure 9. Unclamped Inductive Switching Capability

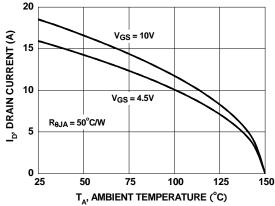


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

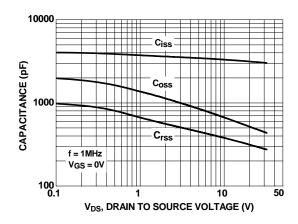


Figure 8. Capacitance vs Drain to Source Voltage

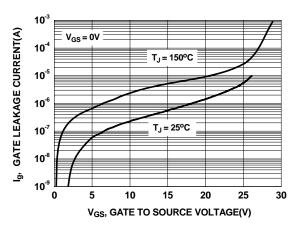


Figure 10. Gate Leakage Current vs Gate to Source Voltage

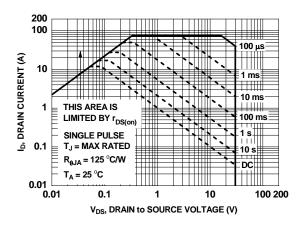


Figure 12. Forward Bias Safe Operating Area

# Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

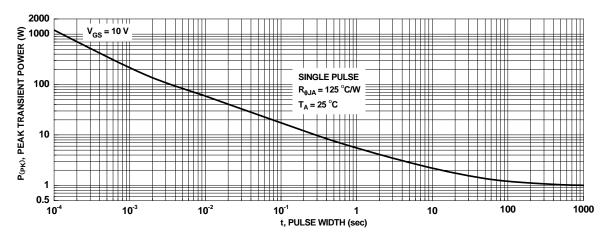


Figure 13. Single Pulse Maximum Power Dissipation

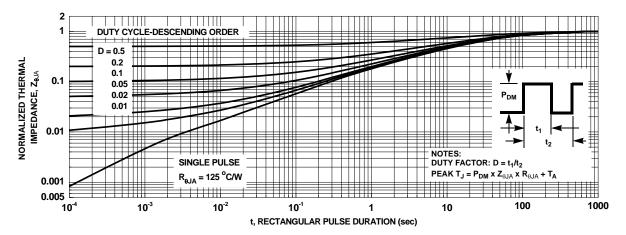


Figure 14. Junction-to-Ambient Transient Thermal Response Curve





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