



ON Semiconductor®

FDS8858CZ

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 30V, 8.6A, 17.0mΩ P-Channel: -30V, -7.3A, 20.5mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 17mΩ at $V_{GS} = 10V$, $I_D = 8.6A$
- Max $r_{DS(on)}$ = 20mΩ at $V_{GS} = 4.5V$, $I_D = 7.3A$

Q2: P-Channel

- Max $r_{DS(on)}$ = 20.5mΩ at $V_{GS} = -10V$, $I_D = -7.3A$
- Max $r_{DS(on)}$ = 34.5mΩ at $V_{GS} = -4.5V$, $I_D = -5.6A$
- High power and handling capability in a widely used surface mount package
- Fast switching speed



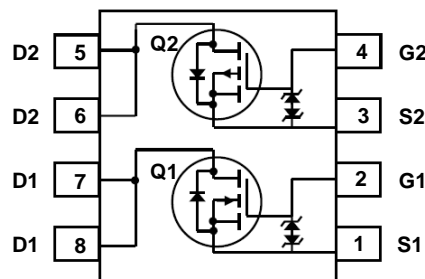
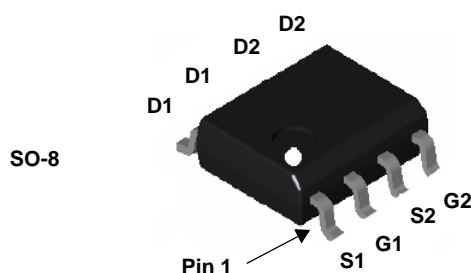
General Description

These dual N and P-Channel enhancement mode power MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications

- Inverter
- Synchronous Buck



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	-30	V
V_{GS}	Gate to Source Voltage	± 20	± 25	V
I_D	Drain Current - Continuous	8.6	-7.3	A
	- Pulsed	20	-20	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	50	11	mJ
P_D	Power Dissipation for Dual Operation	2.0		W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$ (Note 1a)	1.6	
		$T_A = 25^\circ\text{C}$ (Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8858CZ	FDS8858CZ	SO-8	13"	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		22 -22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$ $V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$	Q1 Q2			± 10 ± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q1 Q2	1 -1	1.6 -2.1	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		-5.4 6.0		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 8.6\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 7.3\text{A}$ $V_{GS} = 10\text{V}, I_D = 8.6\text{A}, T_J = 125^\circ\text{C}$	Q1		12.4 15.2 17.7	17.0 20.0 24.3	m Ω
		$V_{GS} = -10\text{V}, I_D = -7.3\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -5.6\text{A}$ $V_{GS} = -10\text{V}, I_D = -7.3\text{A}, T_J = 125^\circ\text{C}$	Q2		17.1 26.5 24.0	20.5 34.5 28.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 8.6\text{A}$ $V_{DS} = -5\text{V}, I_D = -7.3\text{A}$	Q1 Q2		27 21		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1		905	1205	pF
			Q2		1675	2230	
C_{oss}	Output Capacitance	Q2 $V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1		180	240	pF
			Q2		290	390	
C_{riss}	Reverse Transfer Capacitance	Q1 $V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1		110	165	pF
			Q2		260	390	
R_g	Gate Resistance	$f = 1\text{MHz}$	Q1		1.3		Ω
			Q2		4.4		

Switching Characteristics

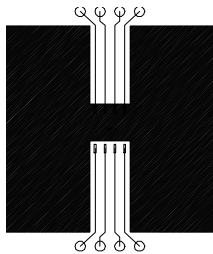
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 15\text{V}, I_D = 8.6\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	Q1		7	14	ns
			Q2		9	18	
t_r	Rise Time	Q2 $V_{DD} = -15\text{V}, I_D = -7.3\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	Q1		3	10	ns
			Q2		10	20	
$t_{d(off)}$	Turn-Off Delay Time	Q1 $V_{DD} = 15\text{V}, I_D = 8.6\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	Q1		19	35	ns
			Q2		33	53	
t_f	Fall Time	Q2 $V_{DD} = -15\text{V}, I_D = -7.3\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	Q1		3	10	ns
			Q2		16	29	
$Q_{g(TOT)}$	Total Gate Charge	Q1 $V_{GS} = 10\text{V}, V_{DD} = 15\text{V}, I_D = 8.6\text{A}$	Q1		17	24	nC
			Q2		33	46	
Q_{gs}	Gate to Source Charge	Q2 $V_{GS} = -10\text{V}, V_{DD} = -15\text{V}, I_D = -7.3\text{A}$	Q1		2.7		nC
			Q2		6.1		
Q_{gd}	Gate to Drain "Miller" Charge	Q1 $V_{GS} = -10\text{V}, V_{DD} = -15\text{V}, I_D = -7.3\text{A}$	Q1		3.4		nC
			Q2		8.5		

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

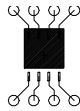
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 8.6A$ (Note 2) $V_{GS} = 0V, I_S = -7.3A$ (Note 2)	Q1 Q2		0.8 0.9	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 8.6A, di/dt = 100A/s$	Q1 Q2		25 28	38 42	ns
Q_{rr}	Reverse Recovery Charge	$I_F = -7.3A, di/dt = 100A/s$	Q1 Q2		19 22	29 33	nC

Notes:

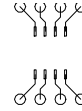
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.
- Starting $T_J = 25^\circ\text{C}$, N-ch: $L = 1\text{mH}, I_{AS} = 10A, V_{DD} = 27V, V_{GS} = 10V$; P-ch: $L = 1\text{mH}, I_{AS} = -4.7A, V_{DD} = -27V, V_{GS} = -10V$.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

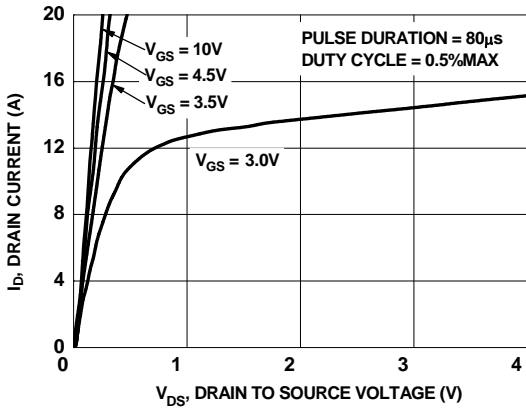


Figure 1. On-Region Characteristics

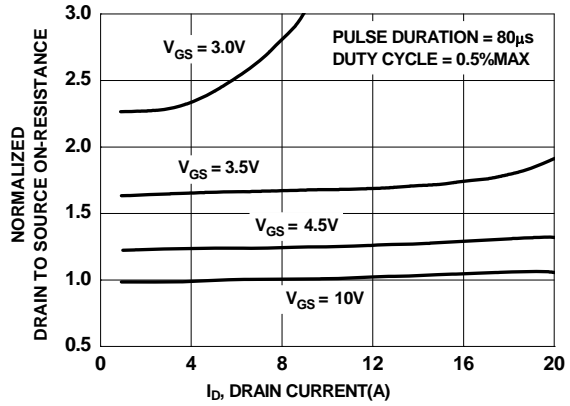


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

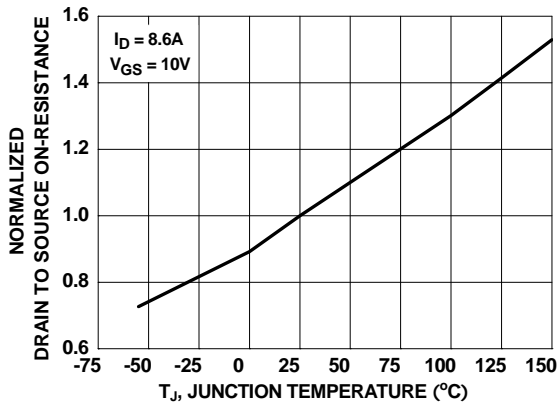


Figure 3. Normalized On-Resistance vs Junction Temperature

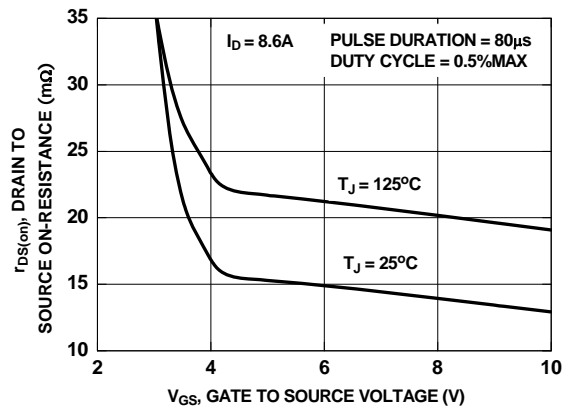


Figure 4. On-Resistance vs Gate to Source Voltage

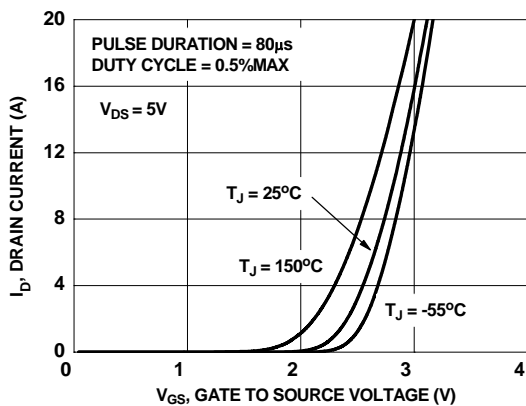


Figure 5. Transfer Characteristics

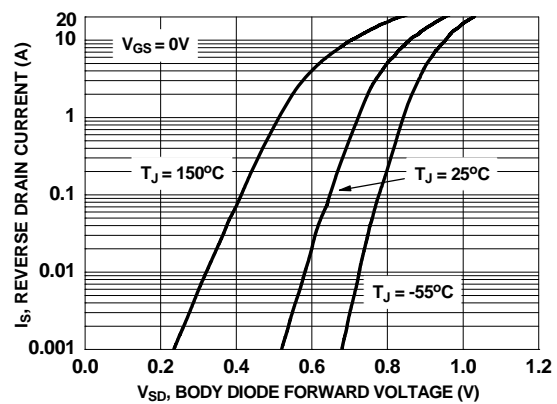


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

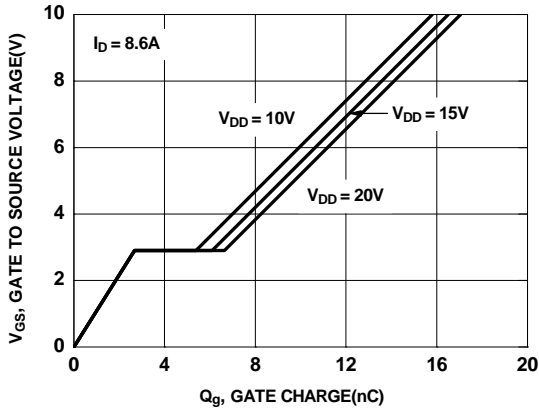


Figure 7. Gate Charge Characteristics

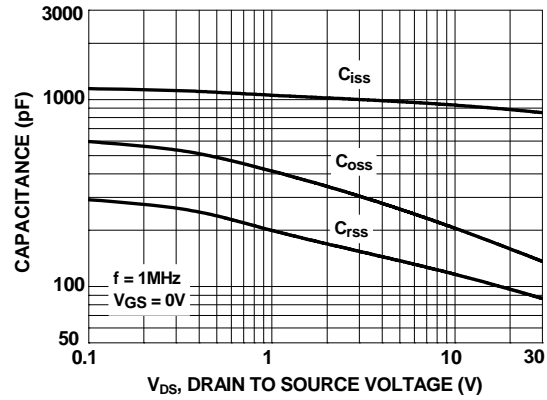


Figure 8. Capacitance vs Drain to Source Voltage

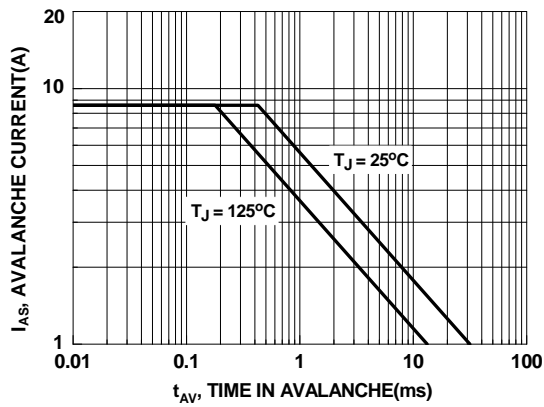


Figure 9. Unclamped Inductive Switching Capability

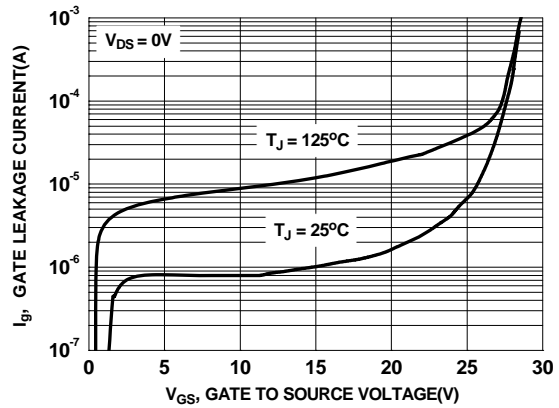


Figure 10. Gate Leakage Current vs Gate to Source Voltage

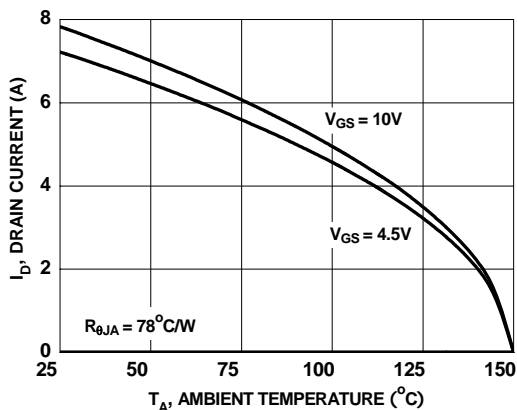


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

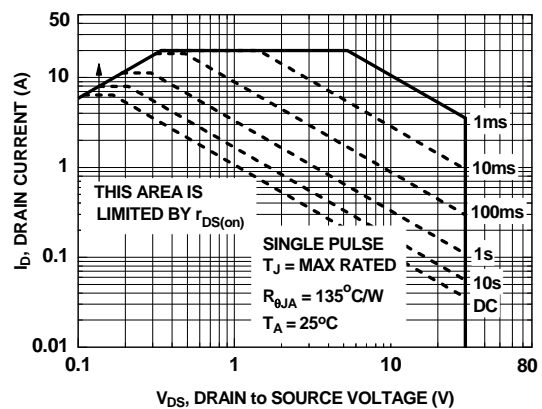


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

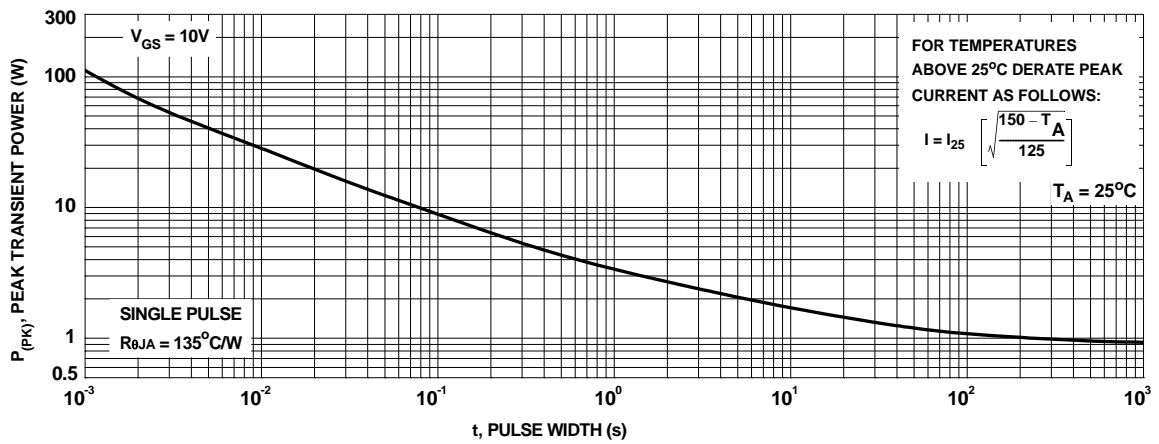


Figure 13. Single Pulse Maximum Power Dissipation

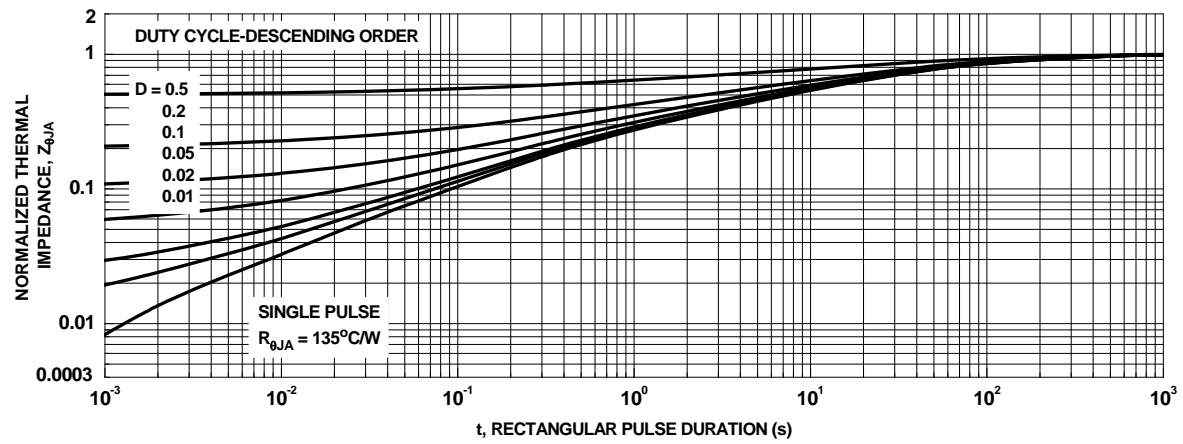


Figure 14. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

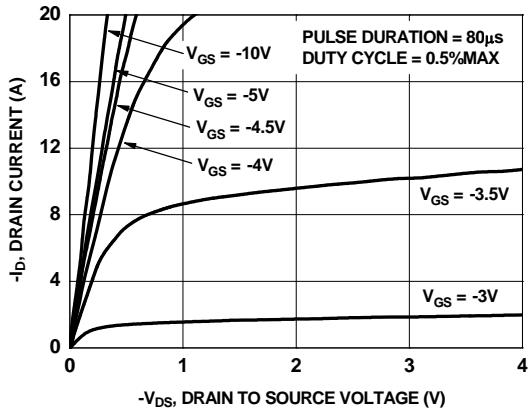


Figure 15. On-Region Characteristics

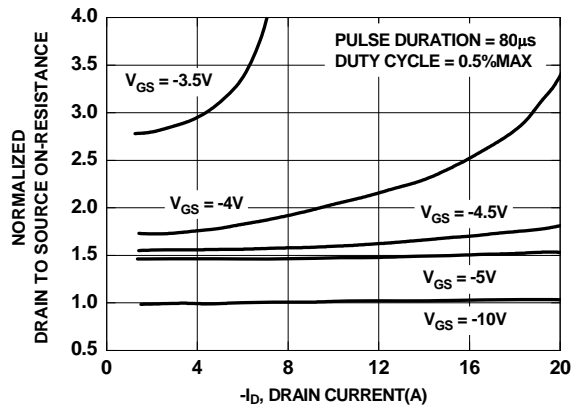


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

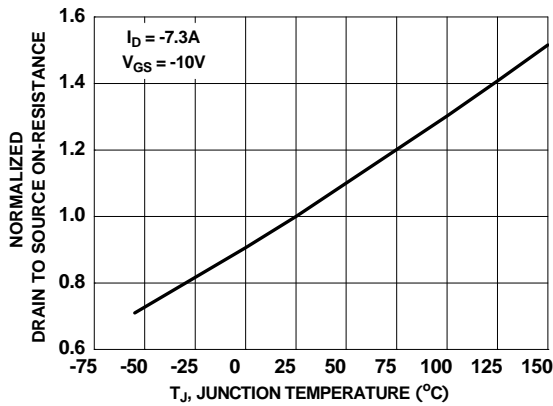


Figure 17. Normalized On-Resistance vs Junction Temperature

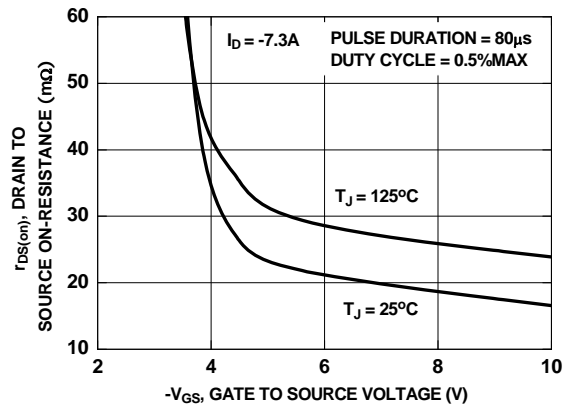


Figure 18. On-Resistance vs Gate to Source Voltage

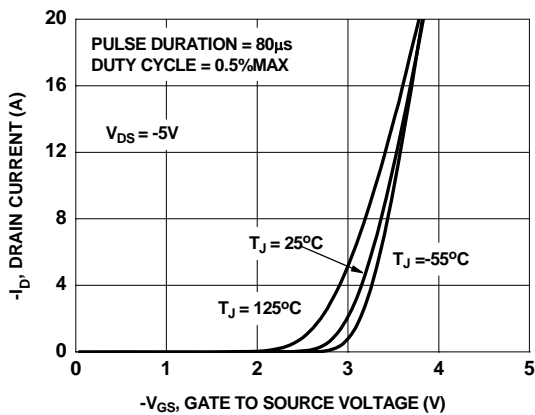


Figure 19. Transfer Characteristics

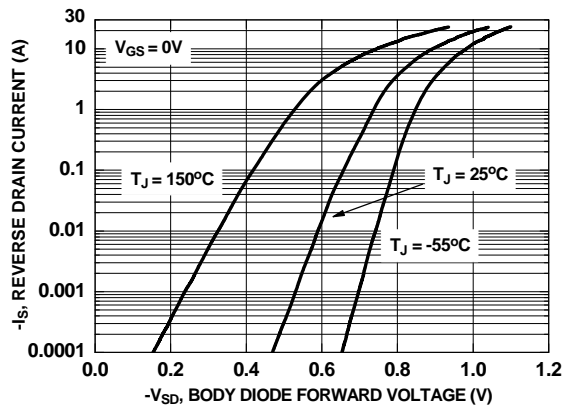


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics(Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

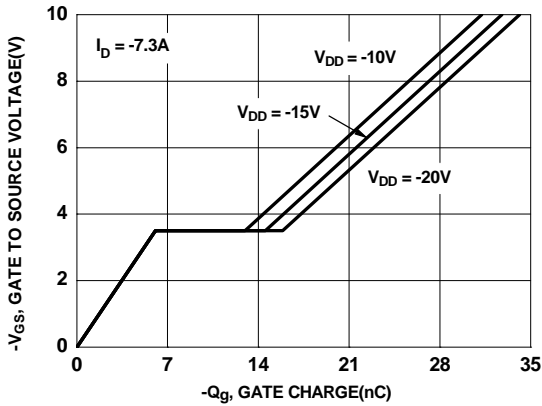


Figure 21. Gate Charge Characteristics

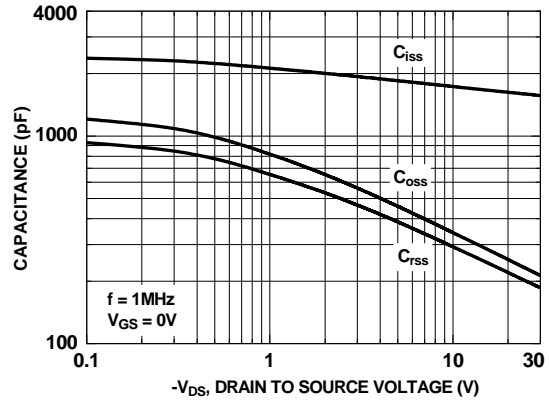


Figure 22. Capacitance vs Drain to Source Voltage

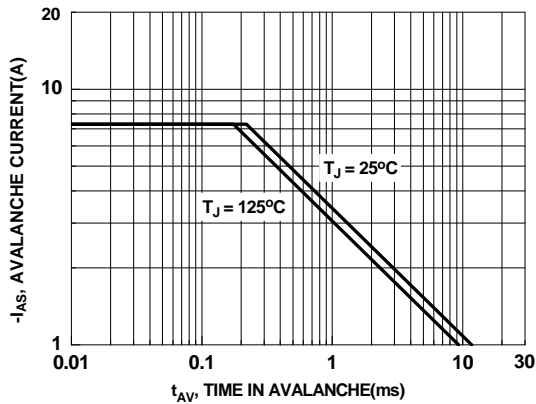


Figure 23. Unclamped Inductive Switching Capability

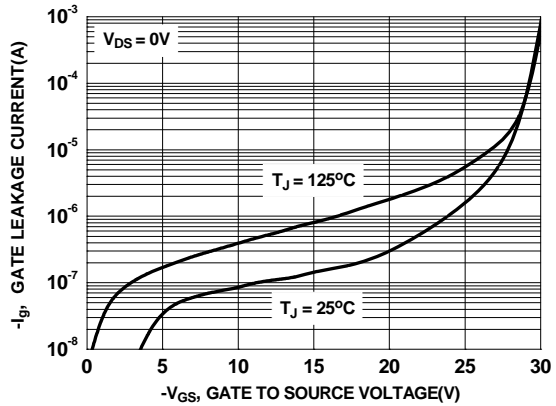


Figure 24. Gate Leakage Current vs Gate to Source Voltage

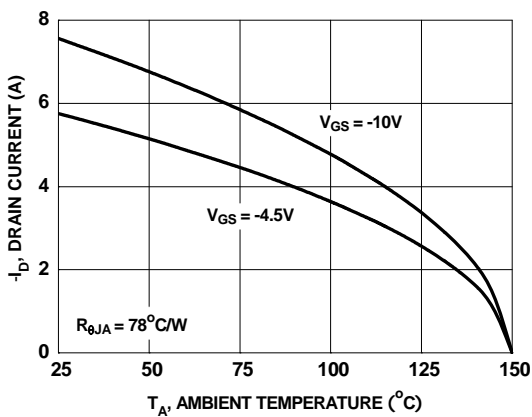


Figure 25. Maximum Continuous Drain Current vs Ambient Temperature

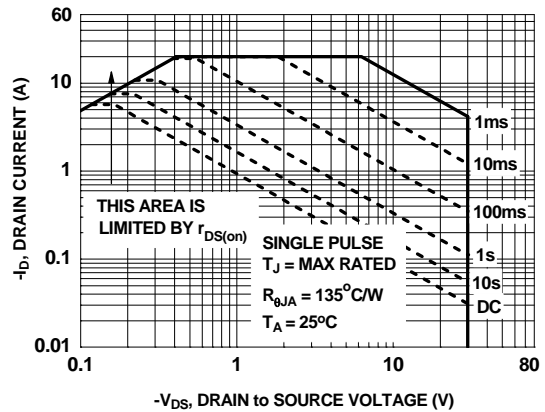


Figure 26. Forward Bias Safe Operating Area

Typical Characteristics(Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

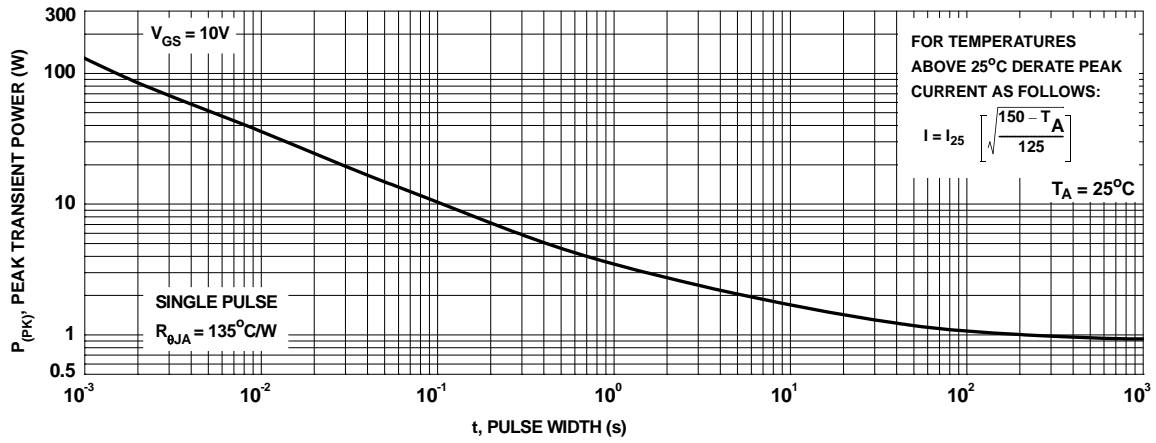


Figure 27. Single Pulse Maximum Power Dissipation

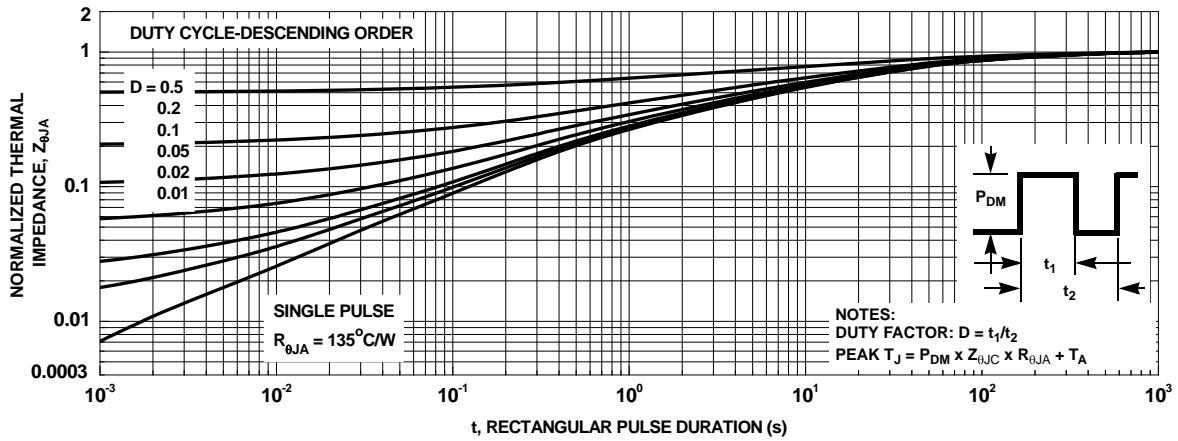



Figure 28. Transient Thermal Response Curve

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative