

# FDS89141-VB Datasheet Dual N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
100	0.0360 at V <sub>GS</sub> = 10 V	6.4	23 nC			
	0.0375 at V <sub>GS</sub> = 8 V	5.5	23110			

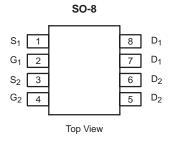
#### **FEATURES**

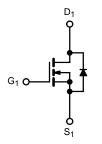
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q<sub>gd</sub> for Switching Losses
- 100 % R<sub>g</sub> Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC

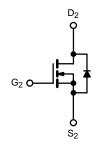


#### **APPLICATIONS**

· Primary Side Switch







N-Channel MOSFET

N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	100	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
	T <sub>C</sub> = 25 °C		6.4		
Continuous Drain Current (T. 150 °C)	T <sub>C</sub> = 70 °C	1 ,	5.1		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	5.5 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		4.5 <sup>b, c</sup>	Α	
Pulsed Drain Current	I <sub>DM</sub>	26	^		
Continuous Course Drain Diade Current	T <sub>C</sub> = 25 °C		4.5		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.6 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20		
Single Pulse Avalanche Energy		E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		5.9		
Maximum Davies Dissination	T <sub>C</sub> = 70 °C		3.8	W	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.1 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C		2 <sup>b, c</sup>		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>sta</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS								
Parameter		Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, †</sup>	t ≤ 10 s	R <sub>thJA</sub>	33	40	°C/W			
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	17	21	7 0/1			

#### Notes

- a. Based on  $T_C$  = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 80 °C/W.



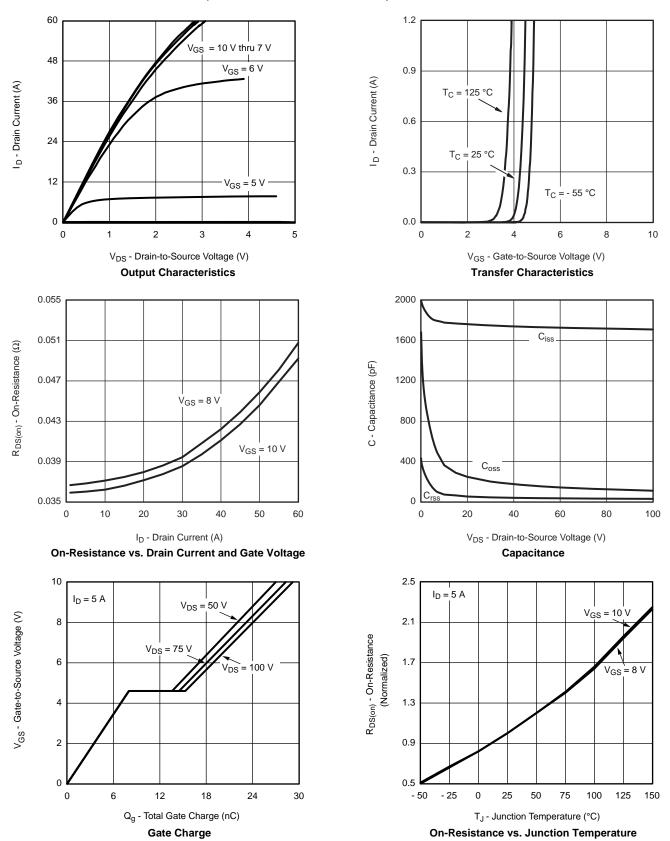
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		172		~~\//°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu\text{A}$		- 10		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu\text{A}$	2.5		4.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Valtana Busin Oamant	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain Course On Chata Desistance	_ ` ′	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	0.0360				
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 8 \text{ V}, I_{D} = 5 \text{ A}$		0.0375		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A		23		S	
Dynamic <sup>b</sup>			•	•			
Input Capacitance	C <sub>iss</sub>			1735			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		160		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			37			
Total Gate Charge	Q <sub>g</sub> V <sub>D</sub>	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		28.5 43	43	nC	
				23	35		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 75 \text{ V}, V_{GS} = 8 \text{ V}, I_{D} = 5 \text{ A}$		8			
Gate-Drain Charge	Q <sub>gd</sub>			6.5			
Gate Resistance	R <sub>g</sub>	f = 1 MHz		0.85	1.3	Ω	
Turn-on Delay Time	t <sub>d(on)</sub>			14	21		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 10 $\Omega$		12	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	33		
Fall Time	t <sub>f</sub>			6	10	no	
Turn-On Delay Time	t <sub>d(on)</sub>			16	24	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 10 $\Omega$		12	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t <sub>f</sub>			7	12	1	
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			7.7	Α	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50	_ ^	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.6 A		0.77	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			63	95	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L = 5 A dl/dt = 100 A/us T = 25 °C		110	165	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		49		20	
Reverse Recovery Rise Time		t <sub>b</sub>		14		ns	

#### Notes:

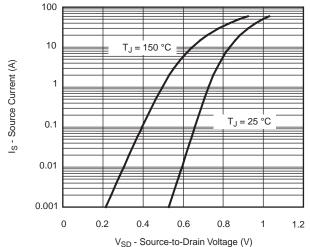
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- a. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

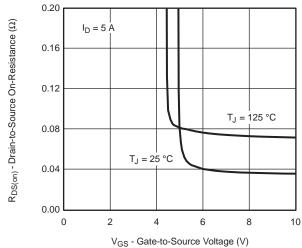




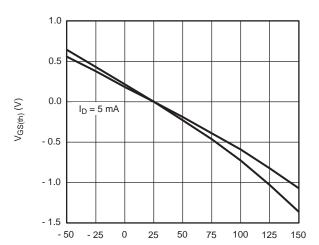








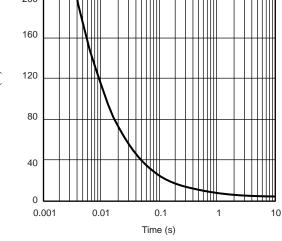
On-Resistance vs. Gate-to-Source Voltage



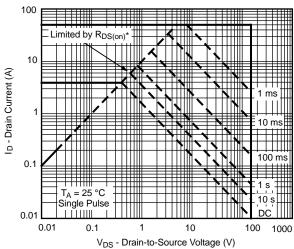
T<sub>J</sub> - Temperature (°C) **Threshold Voltage** 

Source-Drain Diode Forward Voltage





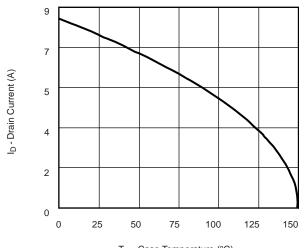
Single Pulse Power, Junction-to-Ambient



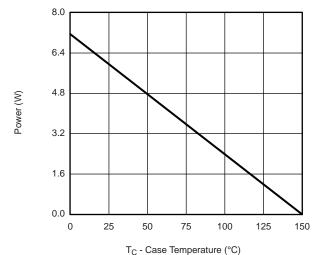
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

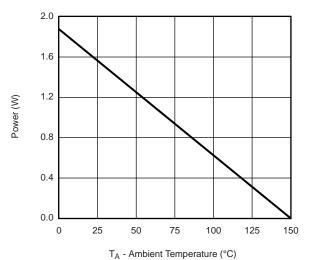




T<sub>C</sub> - Case Temperature (°C) **Current Derating\*** 



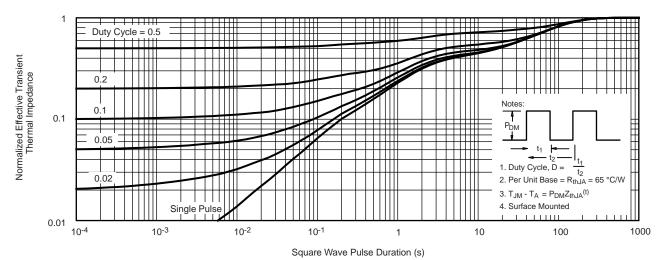
Power, Junction-to-Case



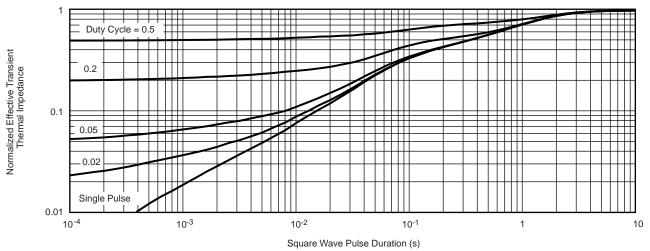
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





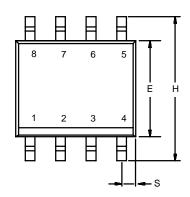
Normalized Thermal Transient Impedance, Junction-to-Ambient

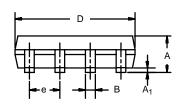


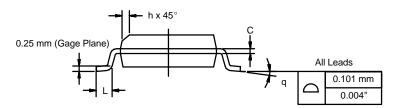
Normalized Thermal Transient Impedance, Junction-to-Foot



**SOIC (NARROW): 8-LEAD**JEDEC Part Number: MS-012







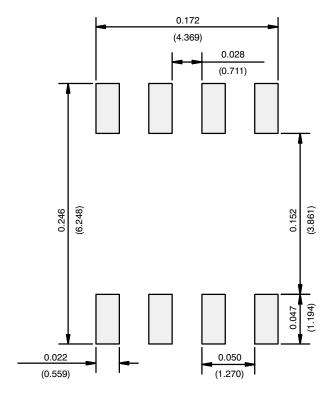
	MILLIM	IETERS	INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sen-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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