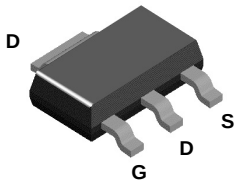
MOSFET – N-Channel, POWERTRENCH®

100 V, 5.6 A, 160 mΩ

FDT1600N10ALZ



SOT−223
CASE 318H

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been tailored to minimize the on−state resistance and maintain superior switching performance.

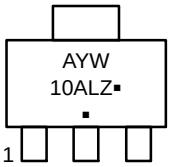
Features

- $R_{DS(on)}$ = 121 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 2.8 A
- $R_{DS(on)}$ = 156 mΩ (Typ.) @ V_{GS} = 5 V, I_D = 1.8 A
- Low Gate Charge (Typ. 2.9 nC)
- Low C_{rss} (Typ. 2.04 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Protection Level: HBM > 5.2 kV, MM > 400 V, CDM > 1.5 kV
- RoHS Compliant

Applications

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter

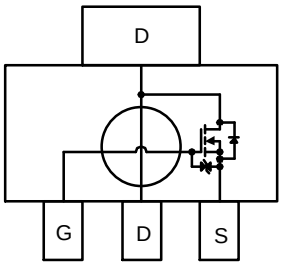
MARKING DIAGRAM



A	= Assembly Location
Y	= Year
W	= Work Week
10ALZ	= Specific Device Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDT1600N10ALZ	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	− Continuous (T_C = 25°C)	5.6	A
		− Continuous (T_C = 100°C)	3.5	
I_{DM}	Drain Current	− Pulsed (Note 2)	11.2	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)		9.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 4)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	10.42	W
		− Derate Above 25°C	0.083	°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering,1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDT1600N10ALZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

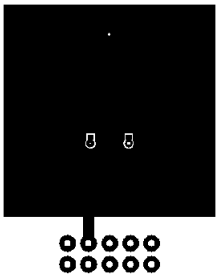
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		100	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		−	0.1	−	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V		−	−	1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_C = 125°C		−	−	500	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V		−	−	±10	μA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.4	−	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.8 A		−	121	160	mΩ
		V_{GS} = 5 V, I_D = 1.8 A		−	156	375	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.6 A		−	26.1	−	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		−	169	225	pF
C_{oss}	Output Capacitance			−	43	55	pF
C_{rss}	Reverse Transfer Capacitance			−	2.04	−	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		−	85	−	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{GS} = 10 V	V_{DD} = 50 V, I_D = 5.6 A (Note 5)	−	2.9	3.77	nC
$Q_{g(tot)}$	Total Gate Charge at 5 V	V_{GS} = 5 V		−	1.6	2.08	nC
Q_{gs}	Gate to Source Gate Charge			−	0.7	−	nC
Q_{gd}	Gate to Drain “Miller” Charge			−	0.64	−	nC
$V_{plateau}$	Gate Plateau Volatge			−	3.81	−	V
Q_{sync}	Total Gate Charge Sync.	V_{DS} = 0 V, I_D = 2.8 A		−	2.45	−	nC
Q_{oss}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		−	5.2	−	nC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

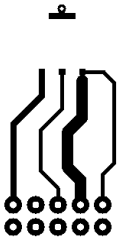
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistance (G−S)	f = 1 MHz	−	2.1	−	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 5.6 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 5)	−	7.4	24.8	ns
t_r	Rise Time		−	2.5	15	ns
$t_{d(off)}$	Turn−Off Delay Time		−	13.5	37	ns
t_f	Turn−Off Fall Time		−	2.4	14.8	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continous Drain to Source Diode Forward Current		−	−	5.6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		−	−	11.2	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 5.6 A	−	−	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 5.6 A, V_{DD} = 50 V dI_F/dt = 100 A/μs	−	34.1	−	ns
Q_{rr}	Reverse Recovery Charge		−	32.7	−	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 118°C/W when mounted on a minimum pad of 2 oz copper

2. Repetitive rating: pulse−width limited by maximum junction temperature.
3. Starting T_J = 25°C, L = 3 mH, I_{AS} = 2.47 A.
4. I_SD ≤ 5.6 A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
5. Essentially independent of operating temperature typical characteristics.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping†
FDT1600N10ALZ	10ALZ	SOT−223	13”	12 mm	4000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

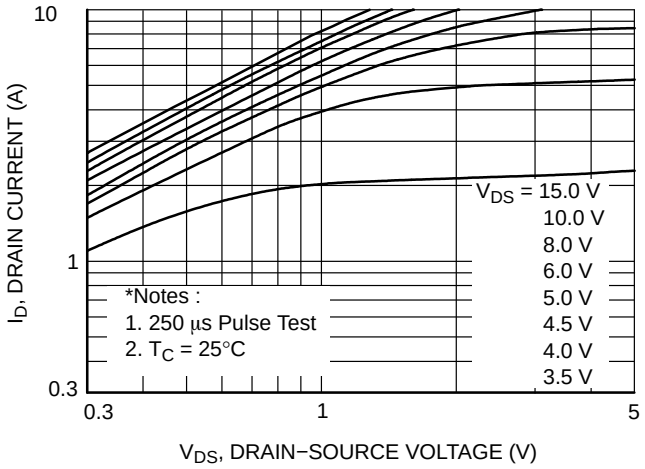


Figure 1. On−Region Characteristics

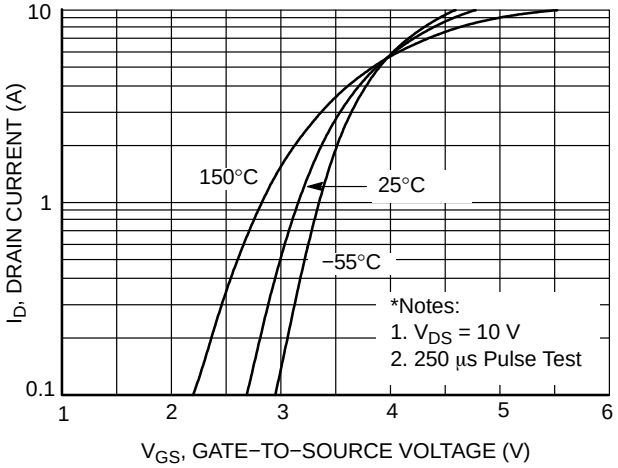


Figure 2. Transfer Characteristics

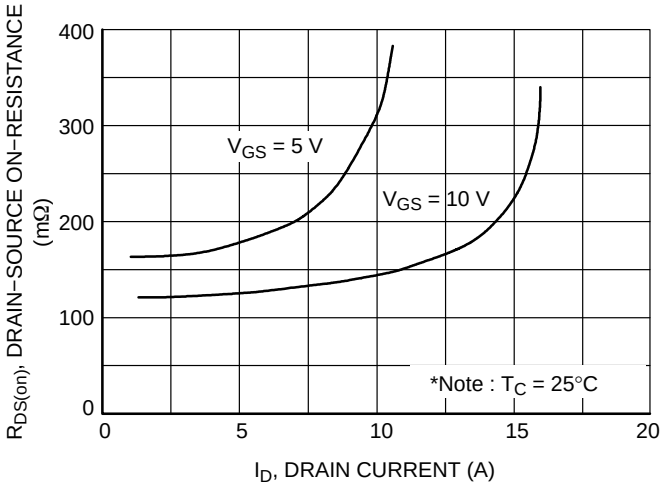


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

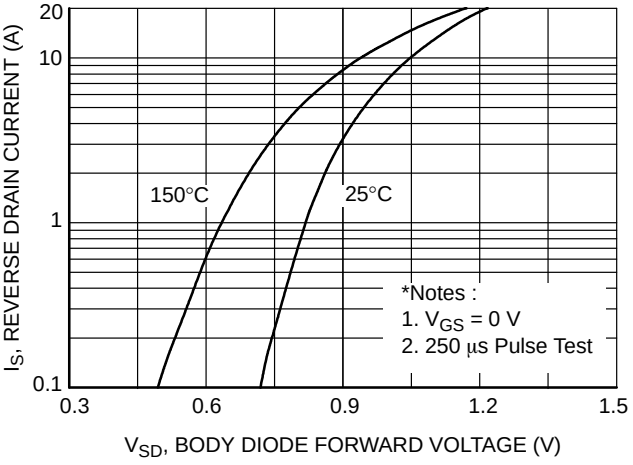


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

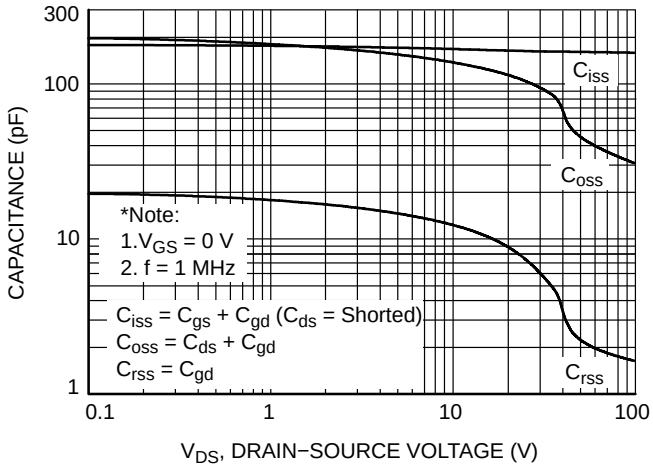


Figure 5. Capacitance Characteristics

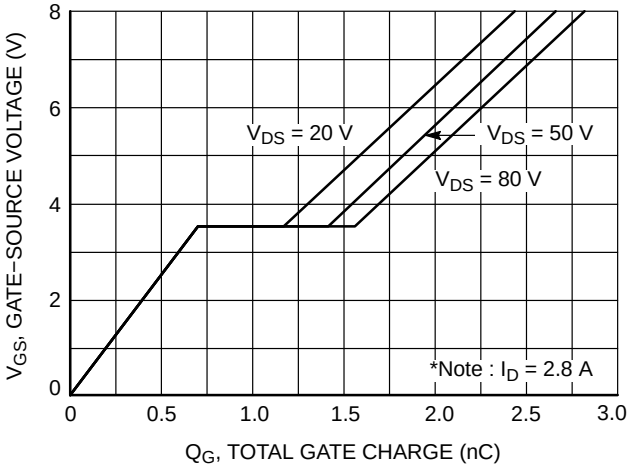


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

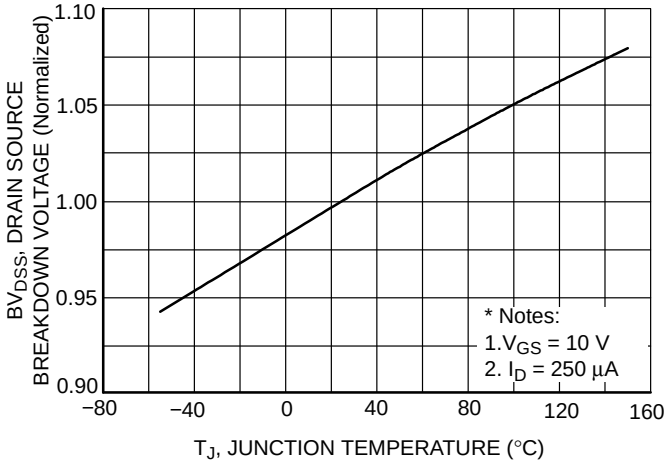


Figure 7. Breakdown Voltage Variation vs. Temperature

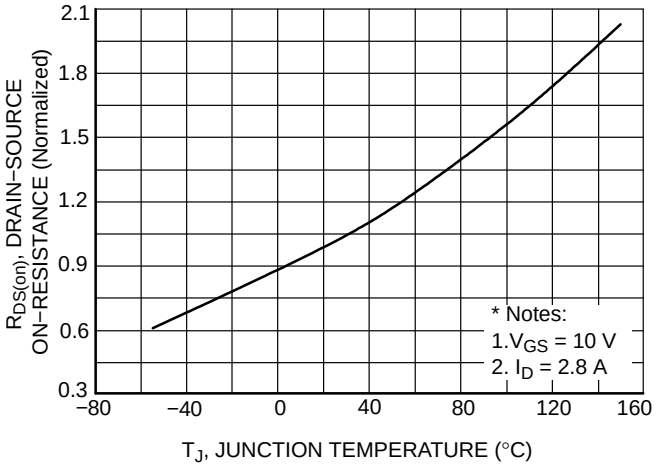


Figure 8. On−Resistance Variation vs. Temperature

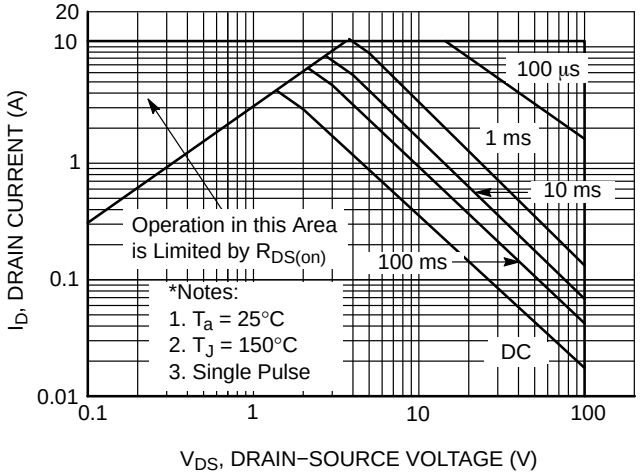


Figure 9. Maximum Safe Operating Area

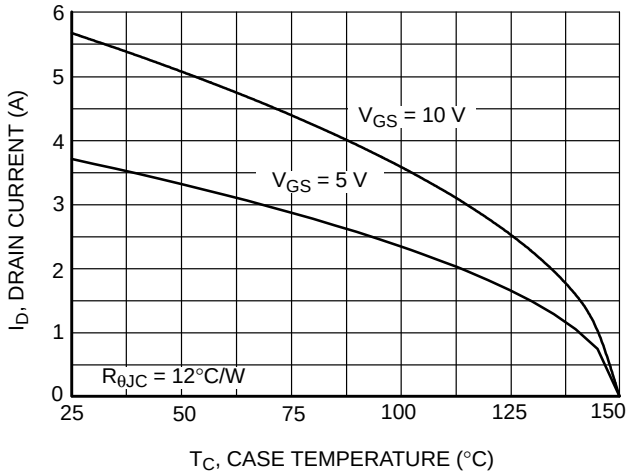


Figure 10. Maximum Drain Current vs. Case Temperature

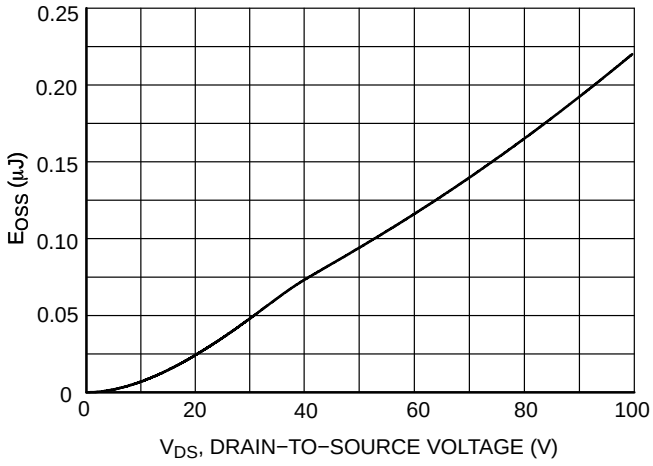


Figure 11. E_{OSS} vs. Drain−to−Source Voltage

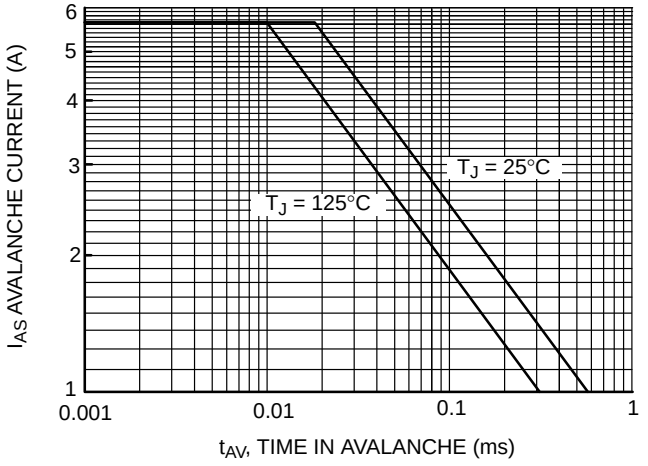


Figure 12. Unclamped Inductive Switching Capability

TYPICAL CHARACTERISTICS (continued)

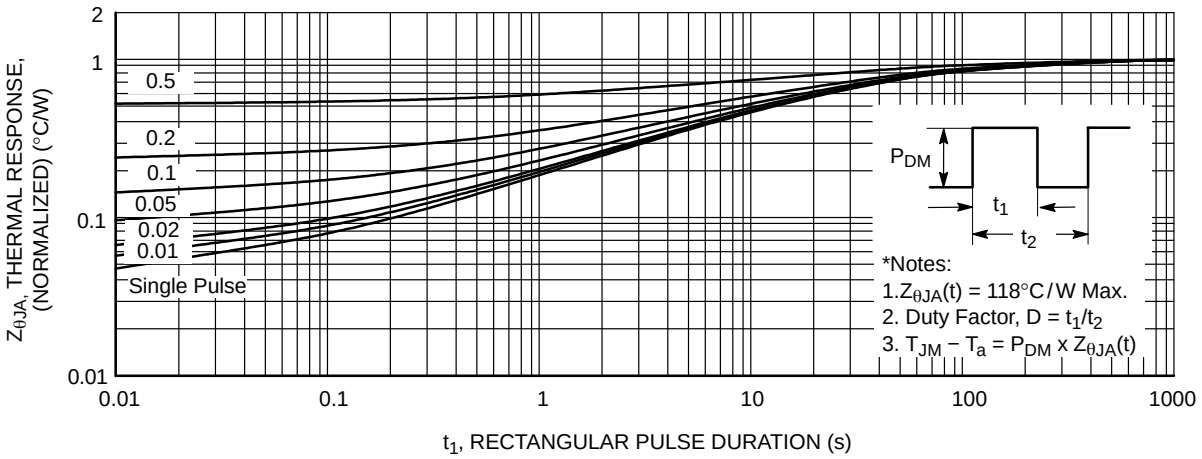


Figure 13. Transient Thermal Response Curve

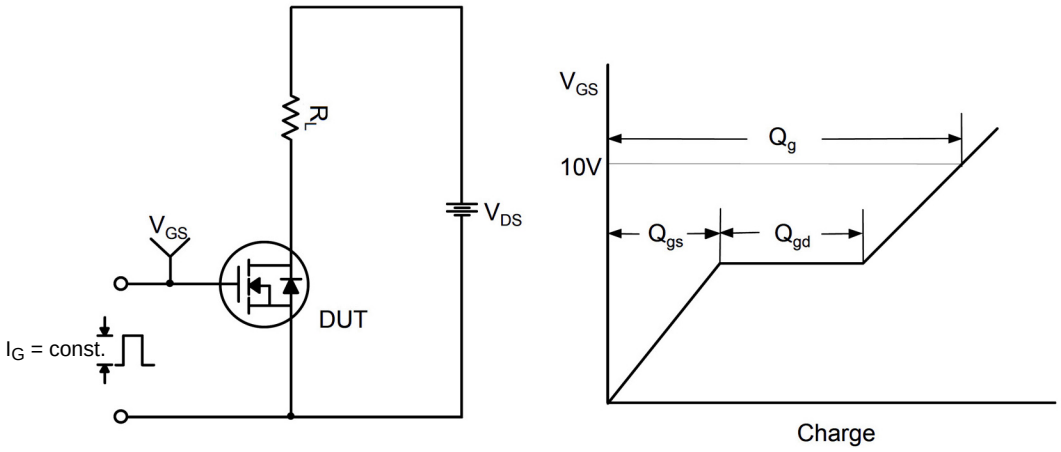


Figure 14. Gate Charge Test Circuit & Waveform

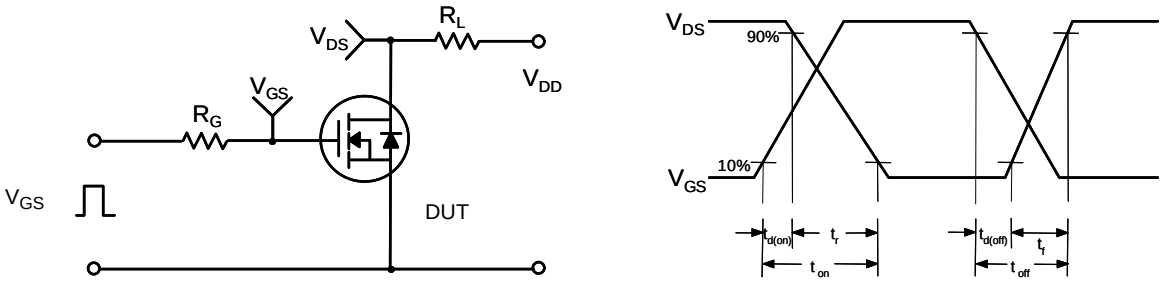


Figure 15. Resistive Switching Test Circuit & Waveforms

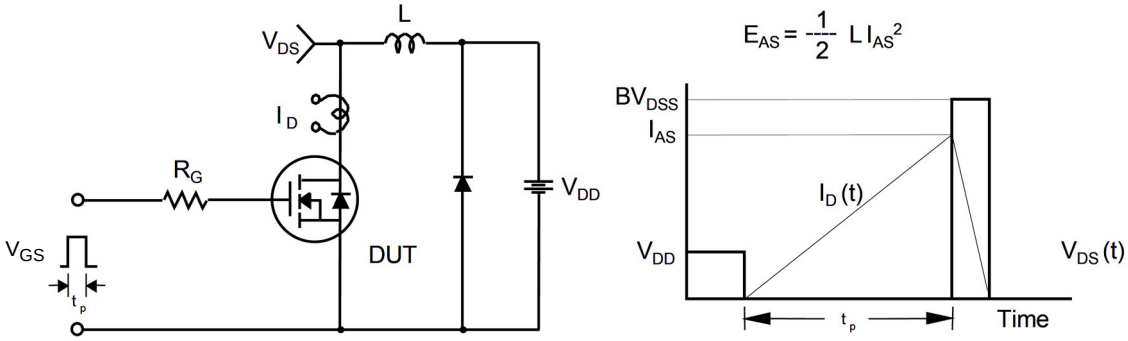


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

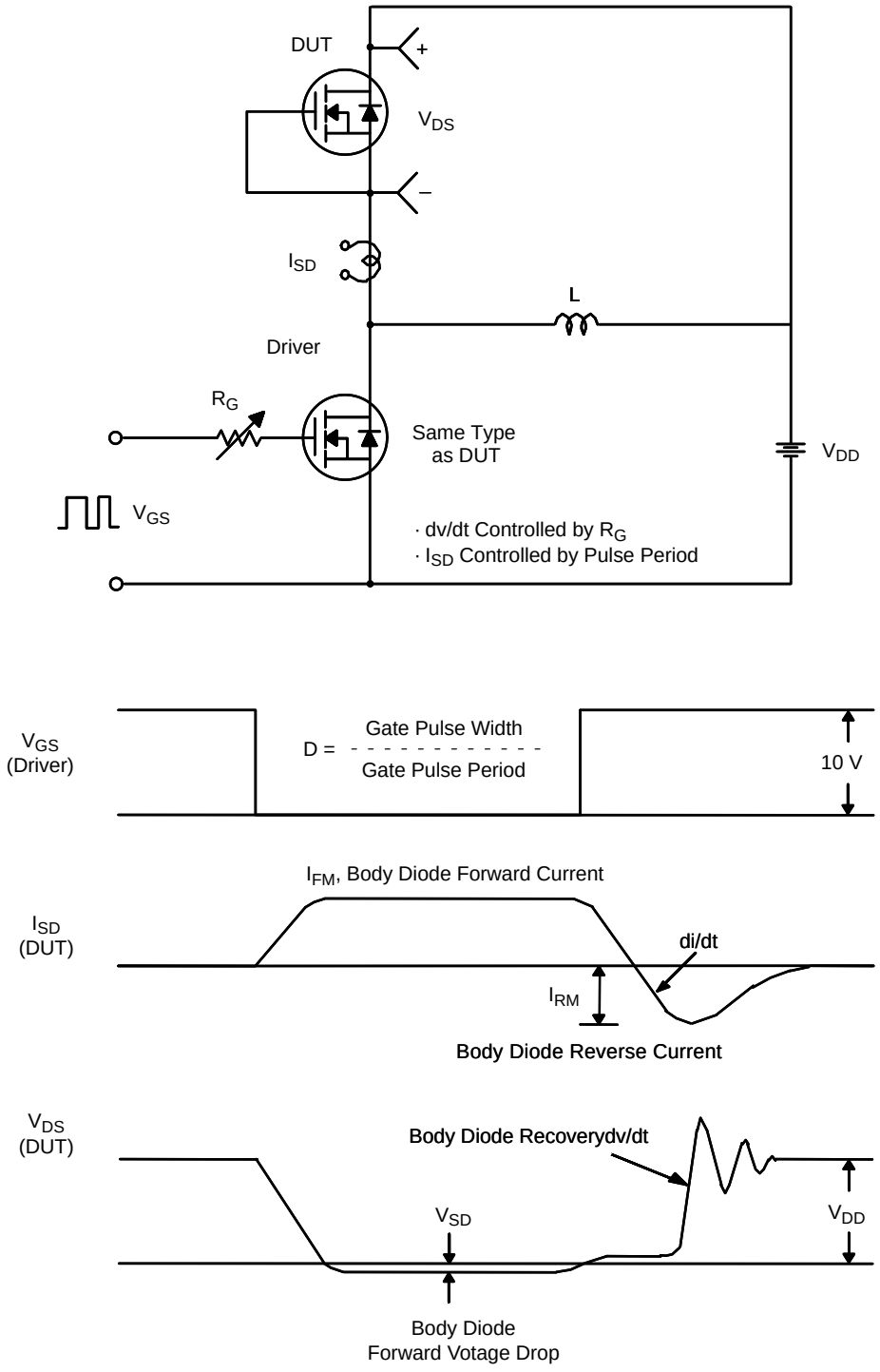
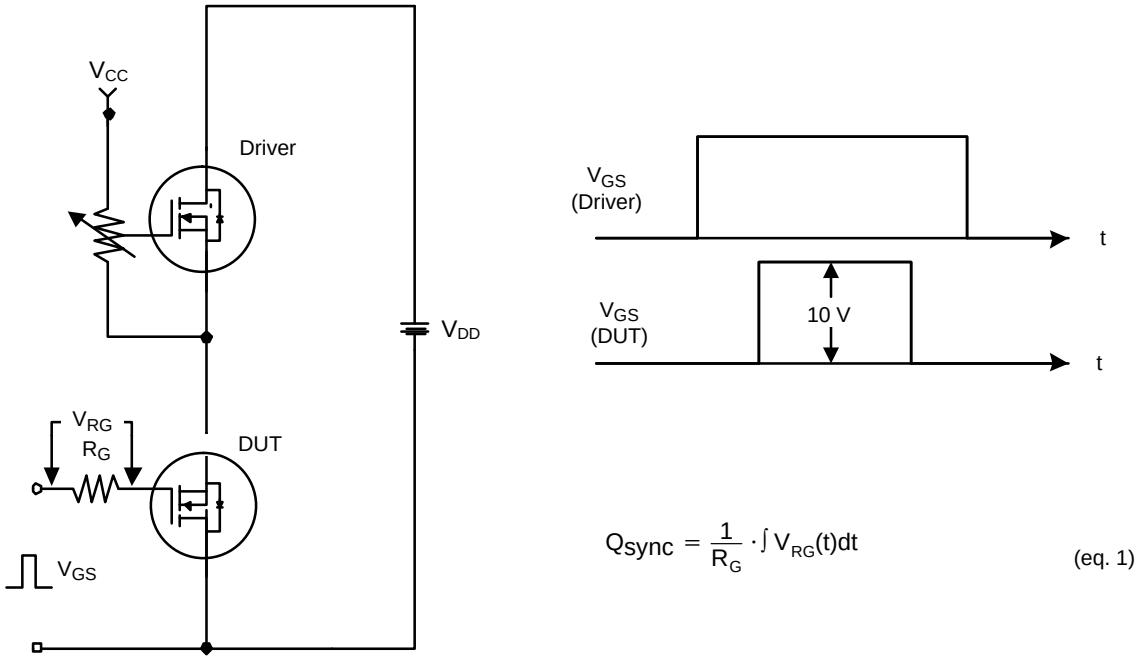
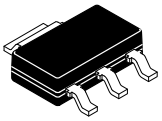


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms



$$Q_{sync} = \frac{1}{R_G} \cdot \int V_{RG}(t)dt \qquad \text{(eq. 1)}$$

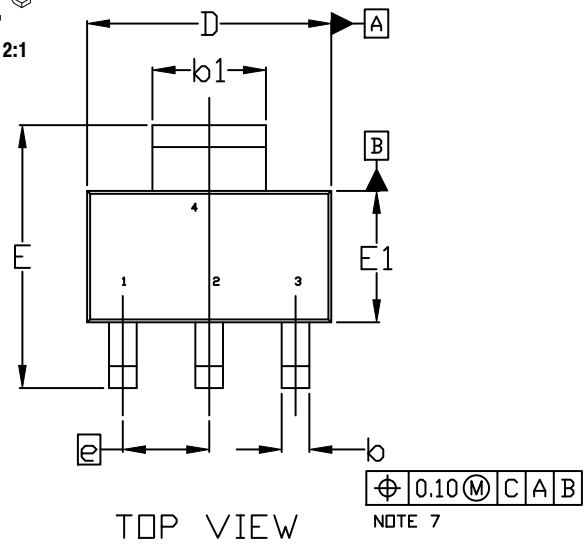
Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

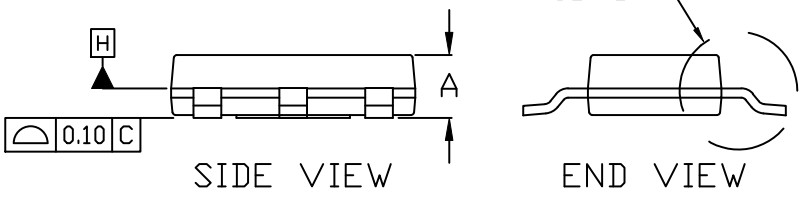


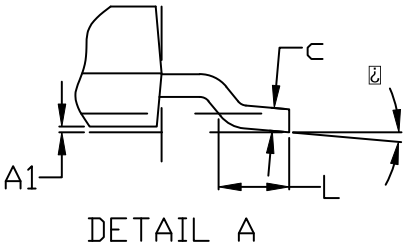
SCALE 2:1

SOT−223
CASE 318H
ISSUE B

DATE 13 MAY 2020

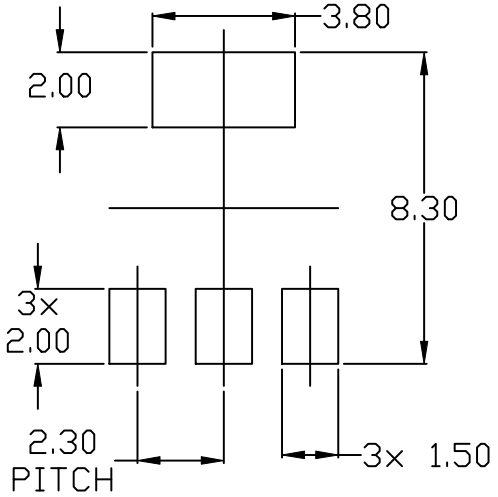






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

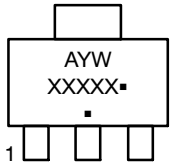
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70634A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOT−223**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales