

Transistor, N-Channel, Field Effect, Enhancement Mode

FDT457N

General Description

These N-Channel enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance. These products are well suited to low voltage, low current applications such as notebook computer power management, battery powered circuits, and DC motor control.

Features

- 5 A, 30 V
 $R_{DS(on)} = 0.06 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(on)} = 0.090 \Omega @ V_{GS} = 4.5 \text{ V}$
- High Density Cell Design for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This Device is Pb-Free

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

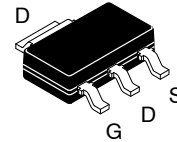
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
I_D	Maximum Drain Current	- Continuous (Note 1a)	5
		- Pulsed	16
P_D	Maximum Power Dissipation	(Note 1a)	3
		(Note 1b)	1.3
		(Note 1c)	1.1
T_J, T_{stg}	Operating and Storage Temperature Range	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

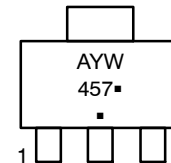
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

V_{DSS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	0.06 $\Omega @ 10 \text{ V}$	5 A
	0.090 $\Omega @ 4.5 \text{ V}$	



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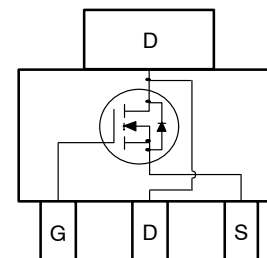
MARKING DIAGRAM



- A = Specific Device Code
- Y = Date Code
- W = Work Week
- 457 = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
FDT457N	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	35	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55°C	–	–	10	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–4.2	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 5 A	–	0.043	0.06	Ω
		V _{GS} = 10 V, I _D = 5 A, T _J = 125°C	–	0.065	0.1	
		V _{GS} = 4.5 V, I _D = 3.8 A	–	0.071	0.09	
I _{D(on)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	5	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 5 A	–	5	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	235	–	pF
C _{oss}	Output Capacitance		–	145	–	pF
C _{rss}	Reverse Transfer Capacitance		–	50	–	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	5	10	ns
t _r	Turn–On Rise Time		–	12	22	ns
t _{d(off)}	Turn–Off Delay Time		–	12	22	ns
t _f	Turn–Off Fall Time		–	3	8	ns
Q _g	Total Gate Charge	V _{DS} = 10 V, I _D = 5 A, V _{GS} = 5 V	–	4.2	5.9	nC
Q _{gs}	Gate–Source Charge		–	1.3	–	nC
Q _{gd}	Gate–Drain Charge		–	1.7	–	nC

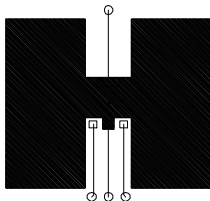
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current	–	–	2.5	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.5 A (Note 2)	–	0.85	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

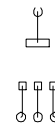
- R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 42°C/W when mounted on a 1 in² pad of 2oz Cu.



b. 95°C/W when mounted on a 0.066 in² pad of 2oz Cu.



c. 110°C/W when mounted on a 0.00123 in² pad of 2oz Cu.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0 %.

TYPICAL CHARACTERISTICS

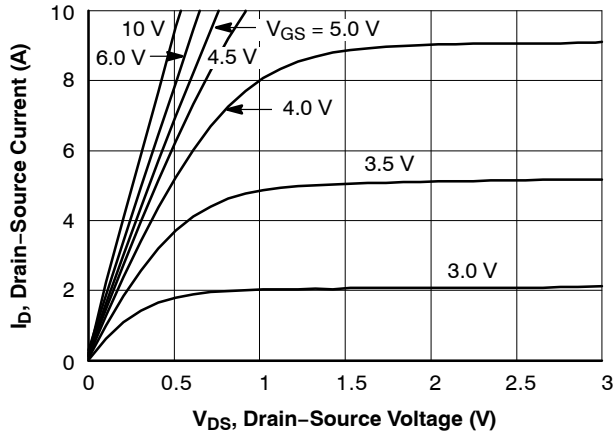


Figure 1. On-Region Characteristics

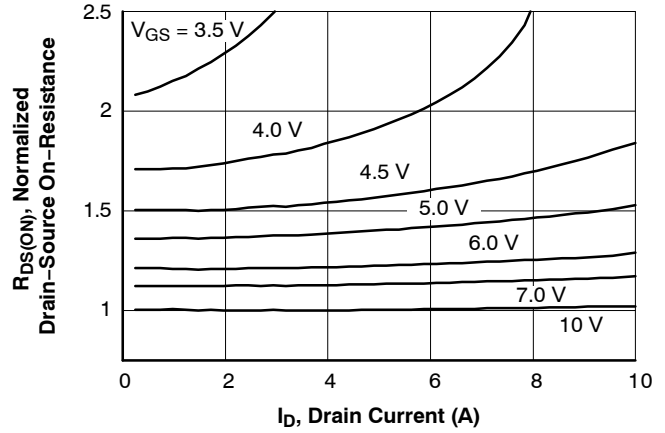


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

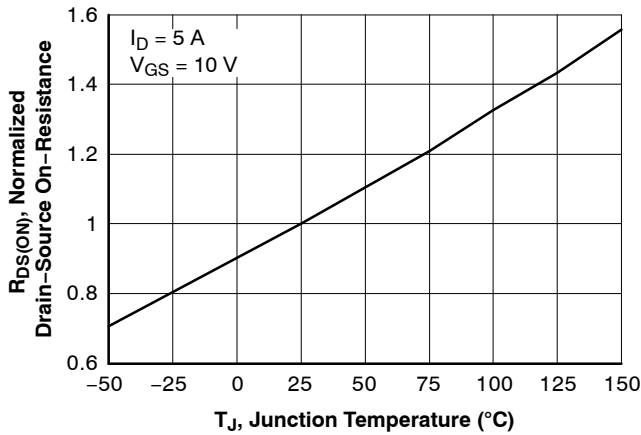


Figure 3. On-Resistance Variation with Temperature

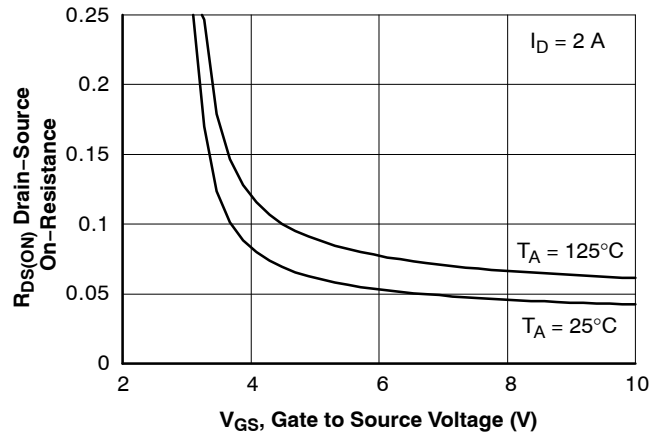


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

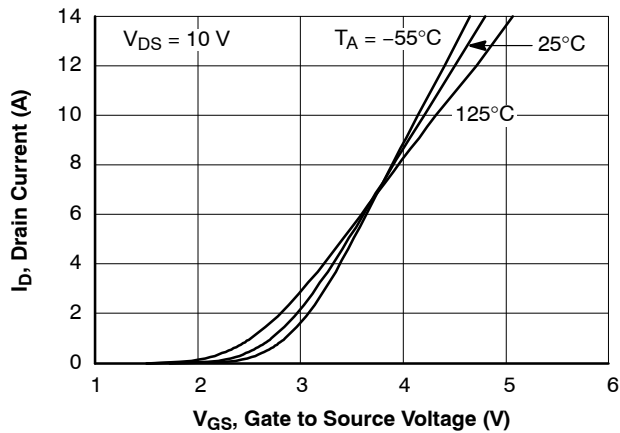


Figure 5. Transfer Characteristics

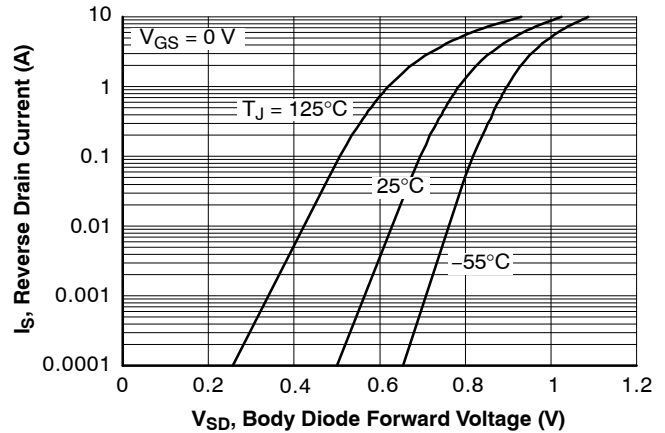


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

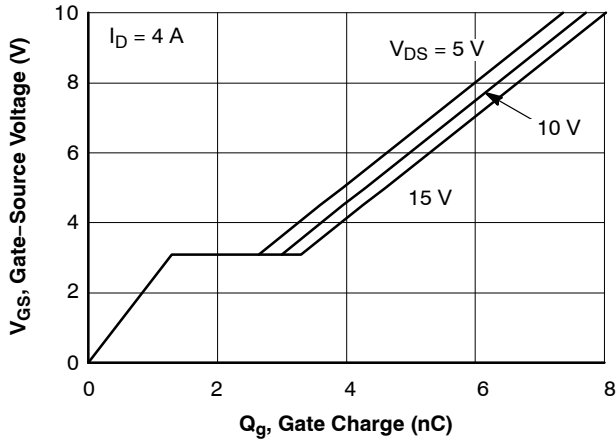


Figure 7. Gate Charge Characteristics

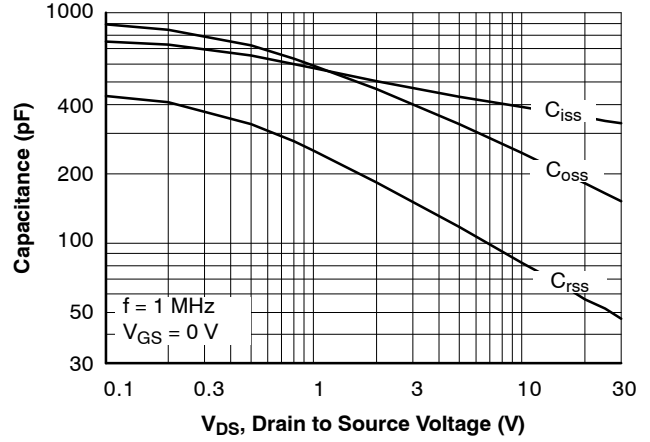


Figure 8. Capacitance Characteristics

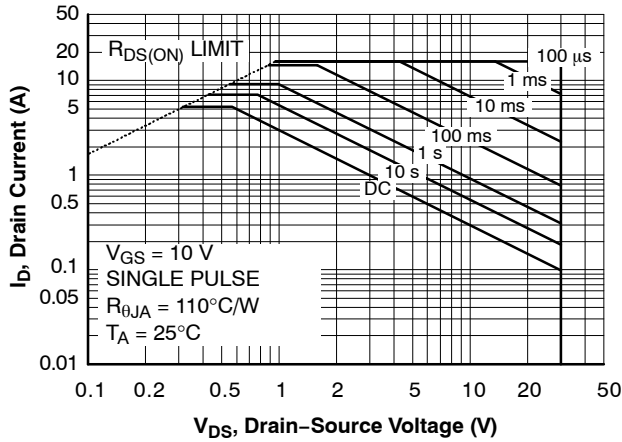


Figure 9. Maximum Safe Operating Area

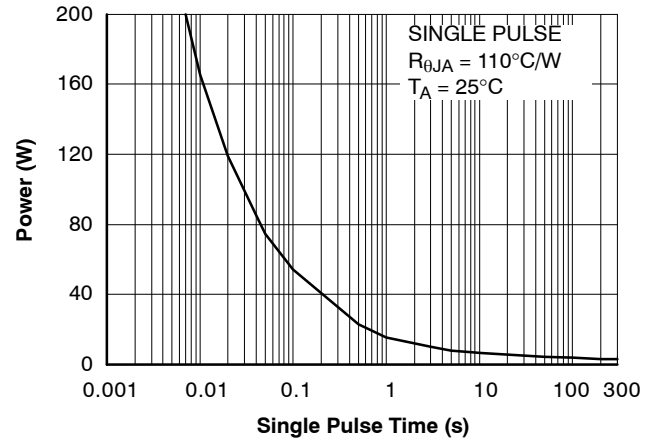


Figure 10. Single Pulse Maximum Power Dissipation

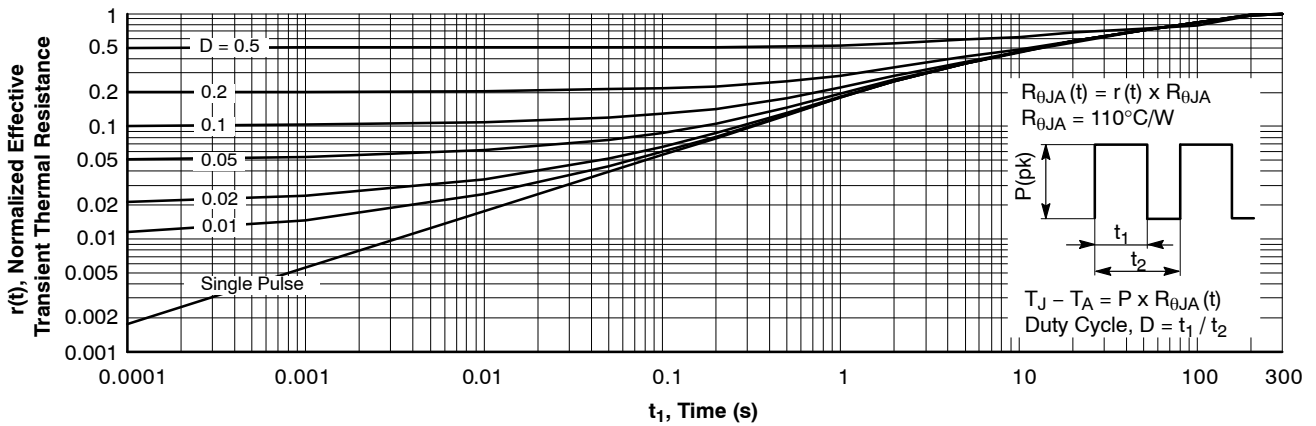


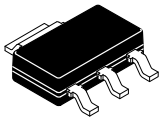
Figure 11. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

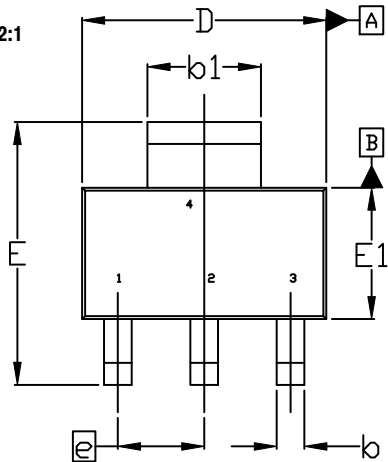
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ISSUE B

DATE 13 MAY 2020

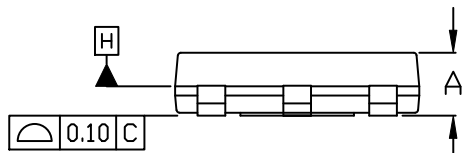
SCALE 2:1



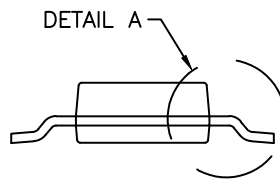
TOP VIEW

$\text{Ø} 0.10 \text{ (M) C A B}$

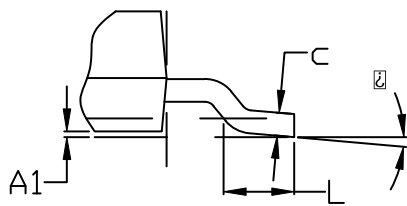
NOTE 7



SIDE VIEW



END VIEW

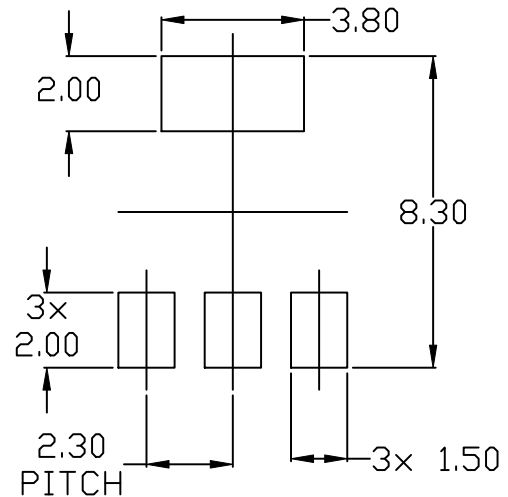


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

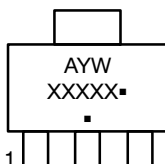
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
Ø	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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