FAIRCHILD SEMICONDUCTOR®

August 2011

# FDT86256

## N-Channel PowerTrench® MOSFET
### 150 V, 1.2 A, 845 mΩ

## Features

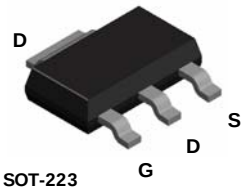
- Max $r_{DS(on)}$ = 845 mΩ at $V_{GS}$ = 10 V, $I_D$ = 1.2 A
- Max $r_{DS(on)}$ = 1280 mΩ at $V_{GS}$ = 6.0 V, $I_D$ = 1.0 A
- Very low Qg and Qgd compared to competing trench technologies
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

## General Description

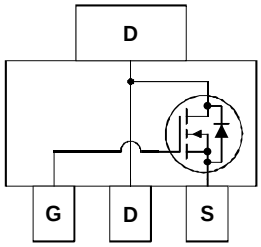
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

## Applications

- DC-DC conversion
- Inverter
- Synchronous Rectifier



SOT-223




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 150 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous (Package limited) | $T_C$ = 25 °C | | 3 | A |
| | -Continuous (Silicon limited) | $T_C$ = 25 °C | | 2.5 | |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | 1.2 | |
| | -Pulsed | | | 2 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 1 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 10 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.3 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 12 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 55 | |

### Package Marking and Ordering Information

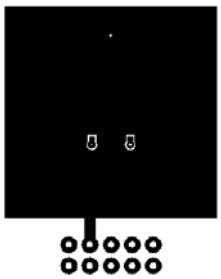
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 86256 | FDT86256 | SOT-223 | 13 ” | 12 mm | 2500 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

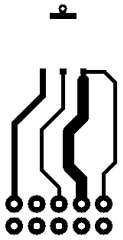
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 150 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 100 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 120 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2 | 3.5 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -8 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.2 A | | 695 | 845 | mΩ |
| | | $V_{GS}$ = 6 V, $I_D$ = 1.0 A | | 912 | 1280 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 1.2 A, $T_J$ = 125 °C | | 1298 | 1367 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 1.2 A | | 0.3 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 75 V, $V_{GS}$ = 0 V, f = 1MHz | | 55 | 73 | pF |
| $C_{oss}$ | Output Capacitance | | | 8 | 11 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 1 | 1.4 | pF |
| $R_g$ | Gate Resistance | | | 1.3 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 75 V, $I_D$ = 1.2 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 2.7 | 10 | ns |
| $t_r$ | Rise Time | | | 1.7 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 4.8 | 10 | ns |
| $t_f$ | Fall Time | | | 2.6 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 75 V, $I_D$ = 1.2 A | | 1.2 | 2.0 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 6 V; $V_{DD}$ = 75 V, $I_D$ = 1.2 A | | 0.8 | 1.0 | |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 75 V, $I_D$ = 1.2 A | | 0.4 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 0.3 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.2 A (Note 2) | | 0.9 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 1.0 A (Note 2) | | 0.8 | 1.3 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 1.2 A, di/dt = 100 A/μs | | 47 | 75 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 24 | 38 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 55 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper



b) 118 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Starting $T_J$ = 25 °C, L = 3 mH, $I_{AS}$ = 1 A, $V_{DD}$ = 150 V, $V_{GS}$ = 10 V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

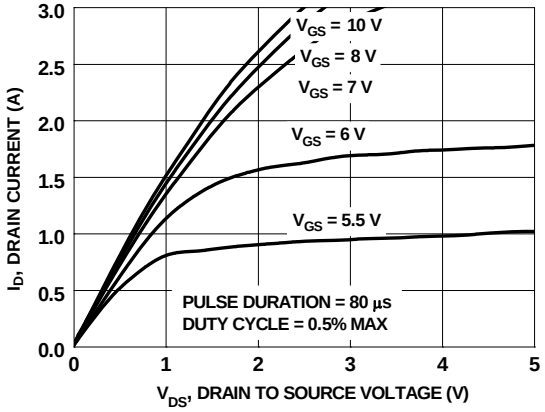



**Figure 1. On-Region Characteristics**

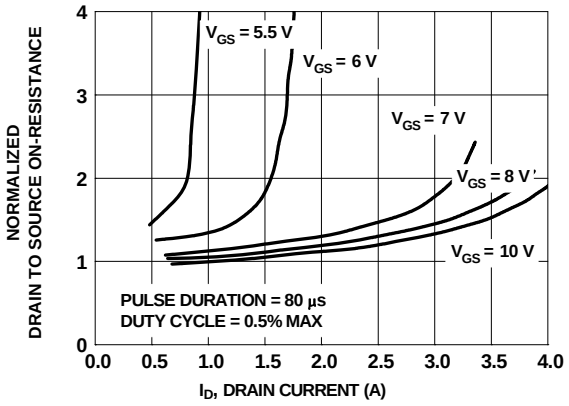



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

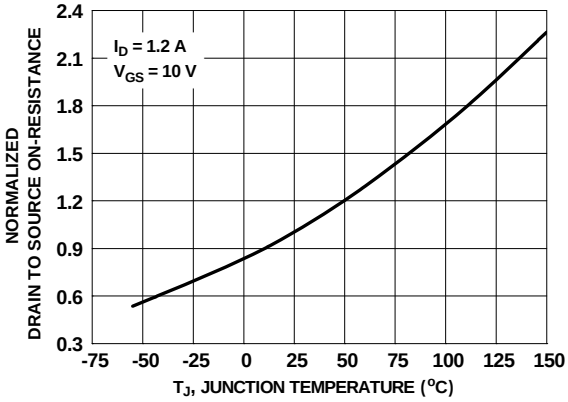



**Figure 3. Normalized On-Resistance vs Junction Temperature**

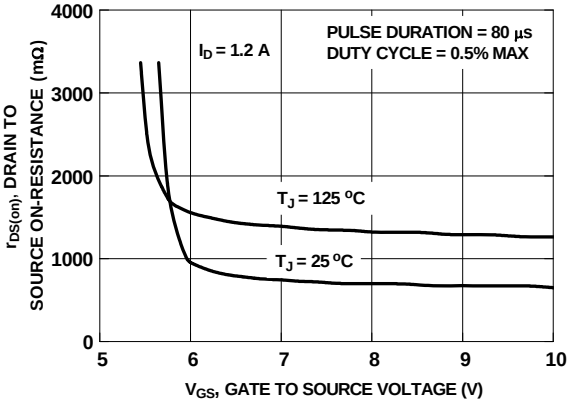



**Figure 4. On-Resistance vs Gate to Source Voltage**

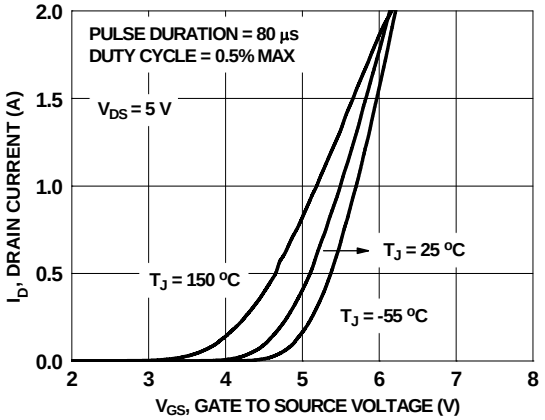



**Figure 5. Transfer Characteristics**

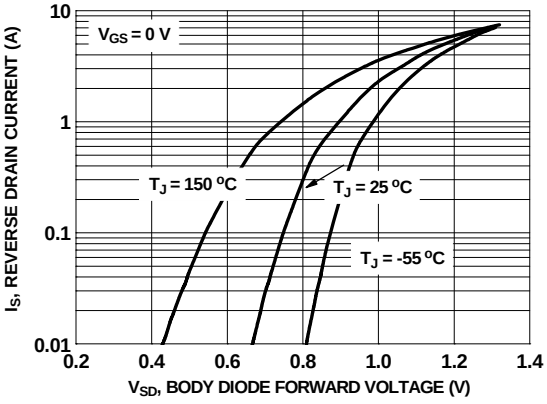



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

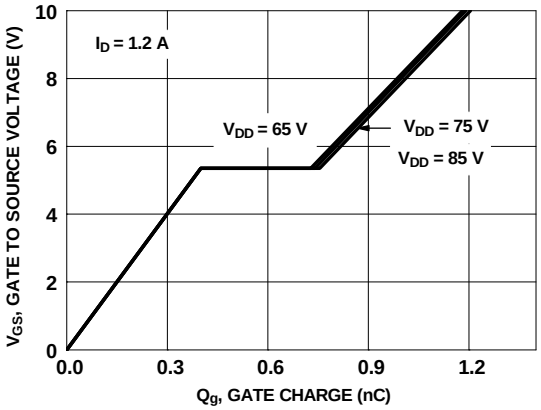



**Figure 7. Gate Charge Characteristics**

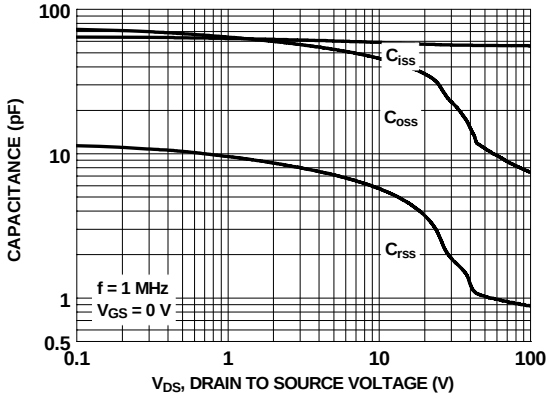



**Figure 8. Capacitance vs Drain to Source Voltage**

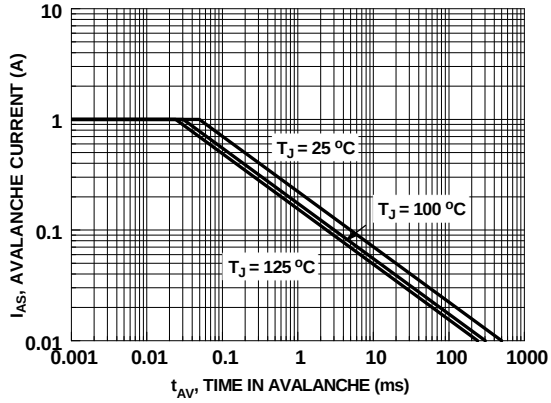



**Figure 9. Unclamped Inductive Switching Capability**

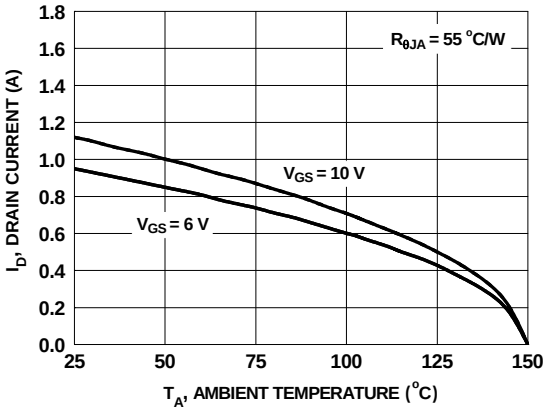



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

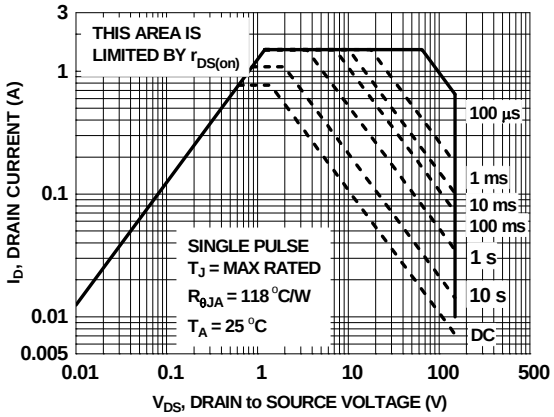



**Figure 11. Forward Bias Safe Operating Area**

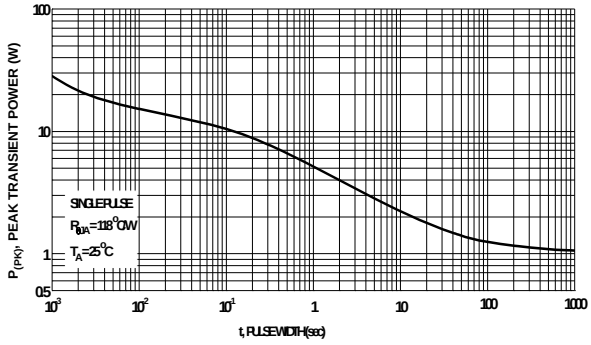



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

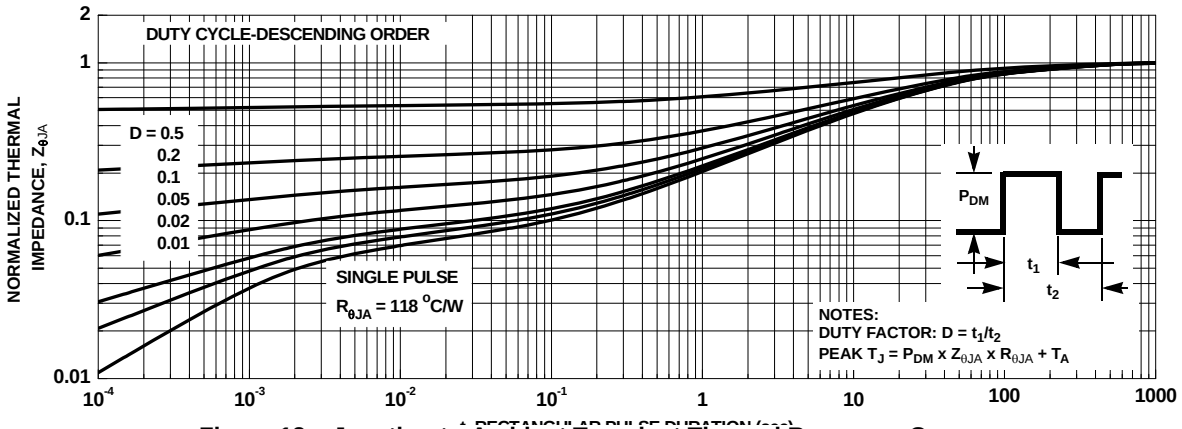
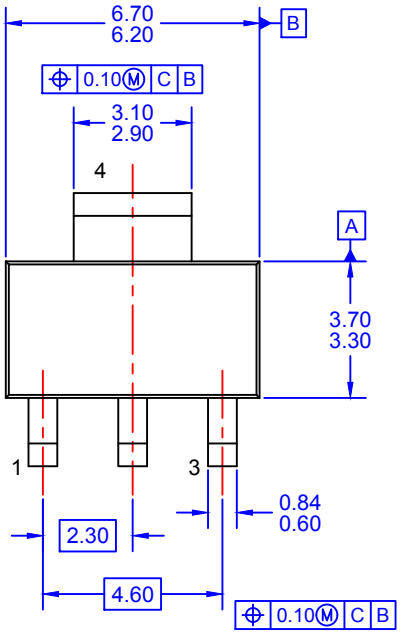
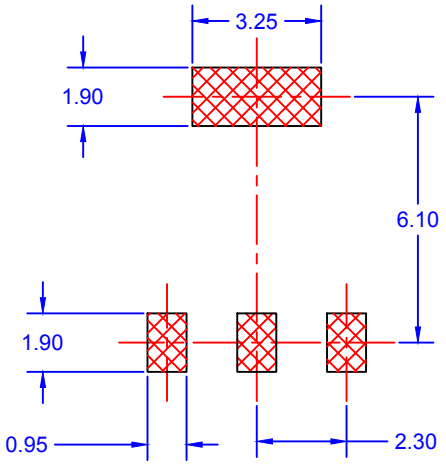
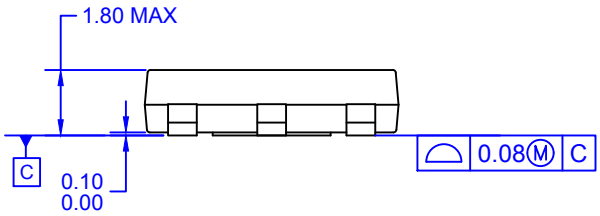


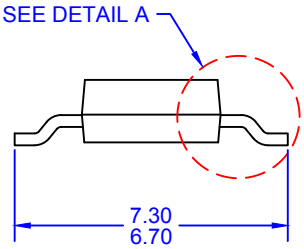

**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



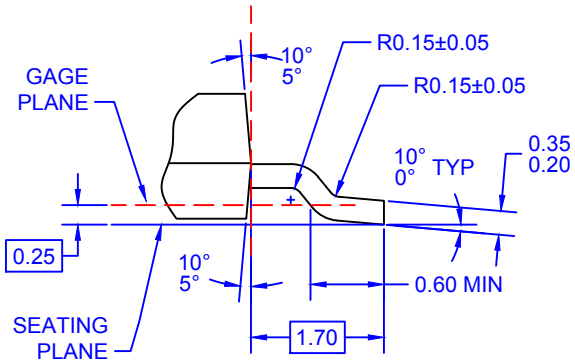




LAND PATTERN RECOMMENDATION




NOTES: UNLESS OTHERWISE SPECIFIED
A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) LANDPATTERN NAME: SOT230P700X180-4BN
F) DRAWING FILENAME: MKT-MA04AREV3




DETAIL A
SCALE: 2:1

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