FAIRCHILD
SEMICONDUCTOR®

November 2013

FDD3N40 / FDU3N40

N-Channel UniFET^{TM} MOSFET

400 V, 2 A, 3.4 Ω

Features

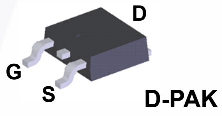
- $R_{DS(on)}$ = 3.4 Ω (Typ.) @ V_{GS} = 10 V, I_D = 1 A
- Low Gate Charge (Typ. 4.5 nC)
- Low C_{rss} (Typ. 3.7 pF)
- 100% Avalanche Tested

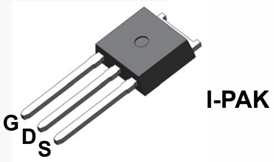
Applications

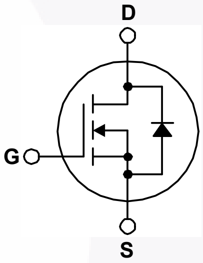
- LED TV
- Consumer Appliances
- Lighting
- Uninterruptible Power Supply

Description

UniFET^{TM} MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDD3N40TM / FDU3N40TU	Unit
V_{DSS}	Drain-Source Voltage		400	V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)	2.0 1.25	A A
I_{DM}	Drain Current	- Pulsed (Note 1)	8.0	A
V_{GSS}	Gate-Source voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	46	mJ
I_{AR}	Avalanche Current	(Note 1)	2	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C) - Derate Above 25°C	30 0.24	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FDD3N40TM / FDU3N40TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD3N40TM	FDD3N40	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FDU3N40TU	FDU3N40	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	400	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.4	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 400 V, V_{GS} = 0 V V_{DS} = 320 V, T_C = 125°C	-- --	-- --	1 10	µA µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1 A	--	2.8	3.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 1 A	--	2	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	--	173	225	pF
C_{oss}	Output Capacitance		--	30	40	pF
C_{rss}	Reverse Transfer Capacitance		--	3.7	6	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 200 V, I_D = 3 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	--	10	30	ns
t_r	Turn-On Rise Time		--	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		--	10	30	ns
t_f	Turn-Off Fall Time		--	25	60	ns
Q_g	Total Gate Charge	V_{DS} = 320 V, I_D = 3 A, V_{GS} = 10 V (Note 4)	--	4.5	6	nC
Q_{gs}	Gate-Source Charge		--	1.2	--	nC
Q_{gd}	Gate-Drain Charge		--	2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 3 A, dI_F/dt =100 A/µs	--	210	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.75	--	µC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 20 mH, I_{AS} = 2 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq 2$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

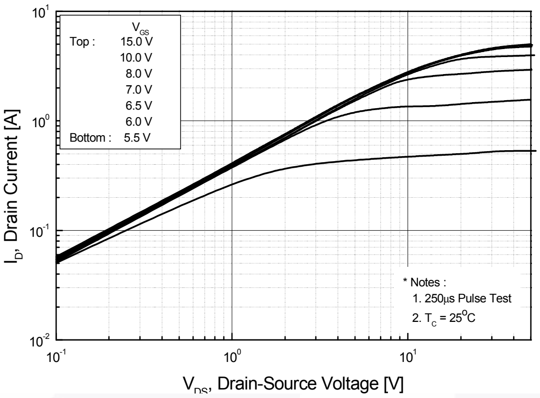


Figure 2. Transfer Characteristics

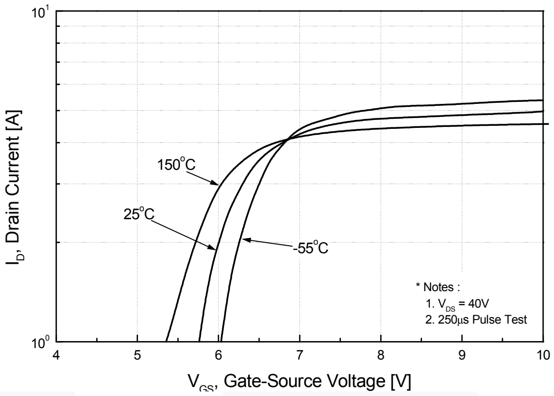


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

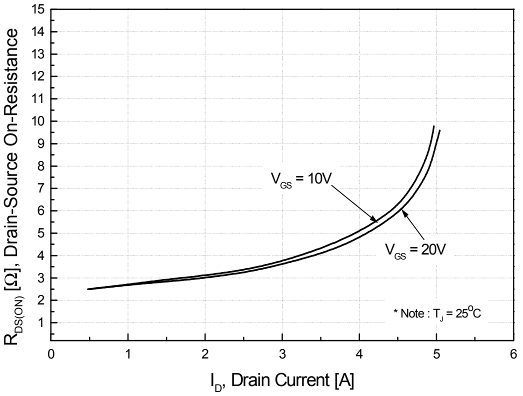


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

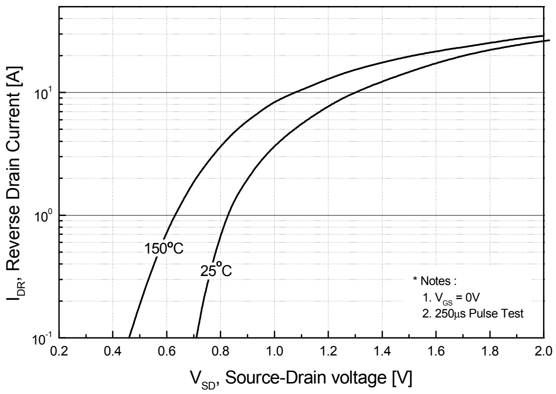


Figure 5. Capacitance Characteristics

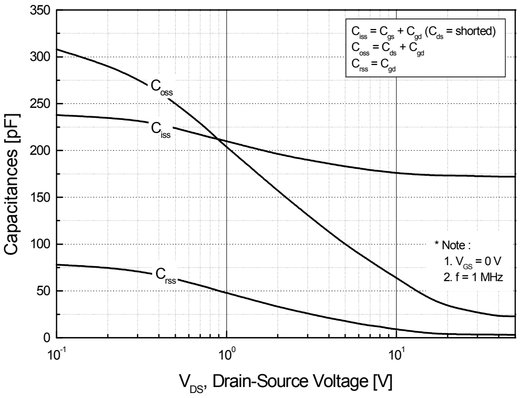
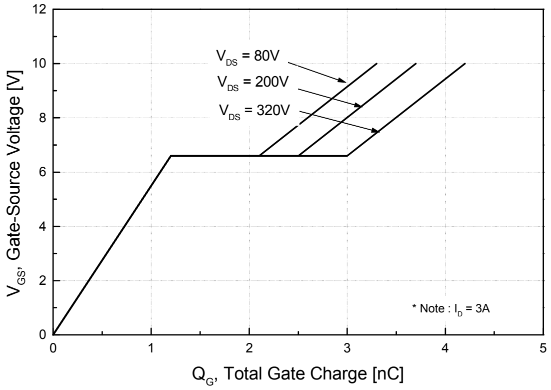


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

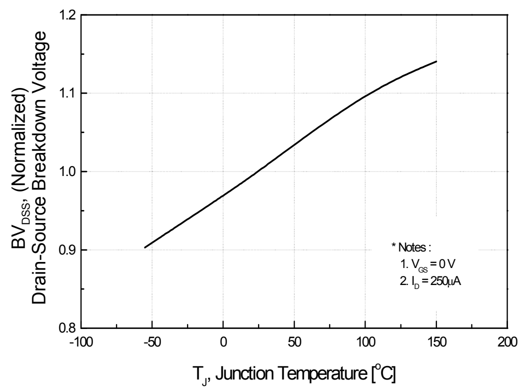


Figure 8. On-Resistance Variation vs. Temperature

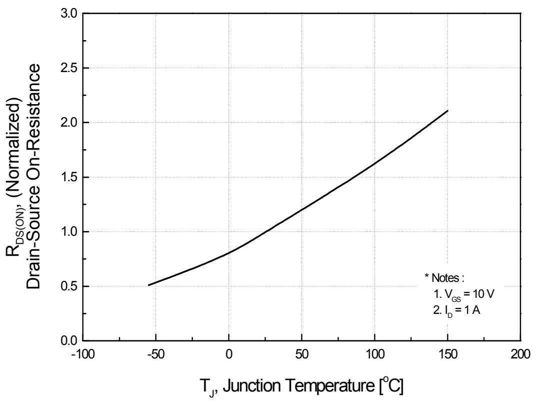


Figure 9. Maximum Safe Operating Area

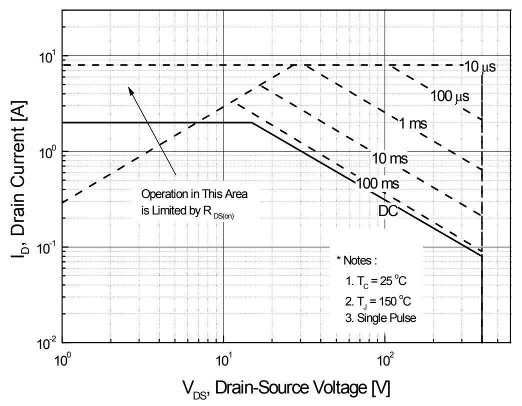


Figure 10. Maximum Drain Current vs. Case Temperature

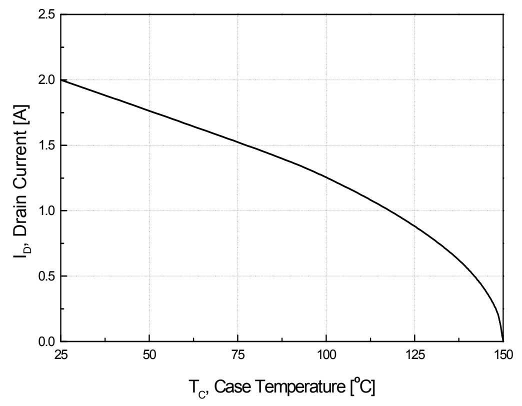
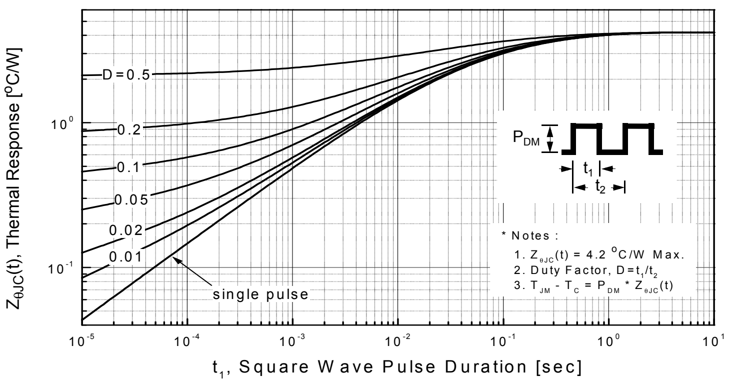


Figure 11. Transient Thermal Response Curve



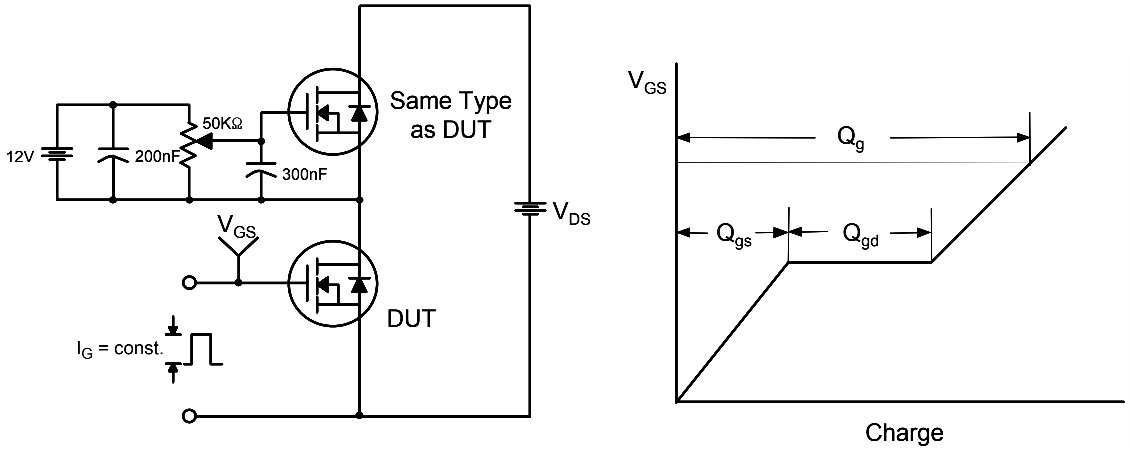


Figure 12. Gate Charge Test Circuit & Waveform

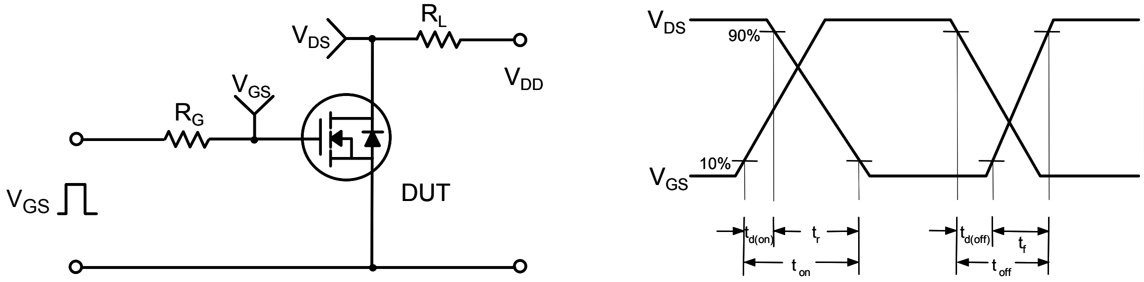


Figure 13. Resistive Switching Test Circuit & Waveforms

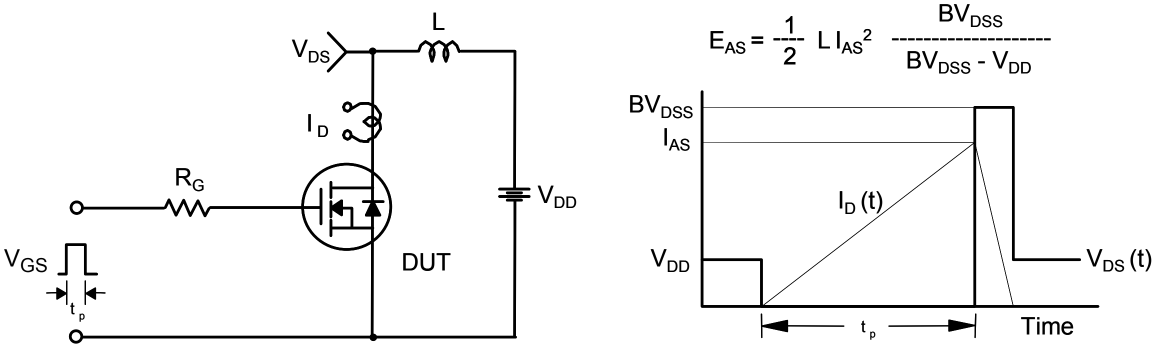


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

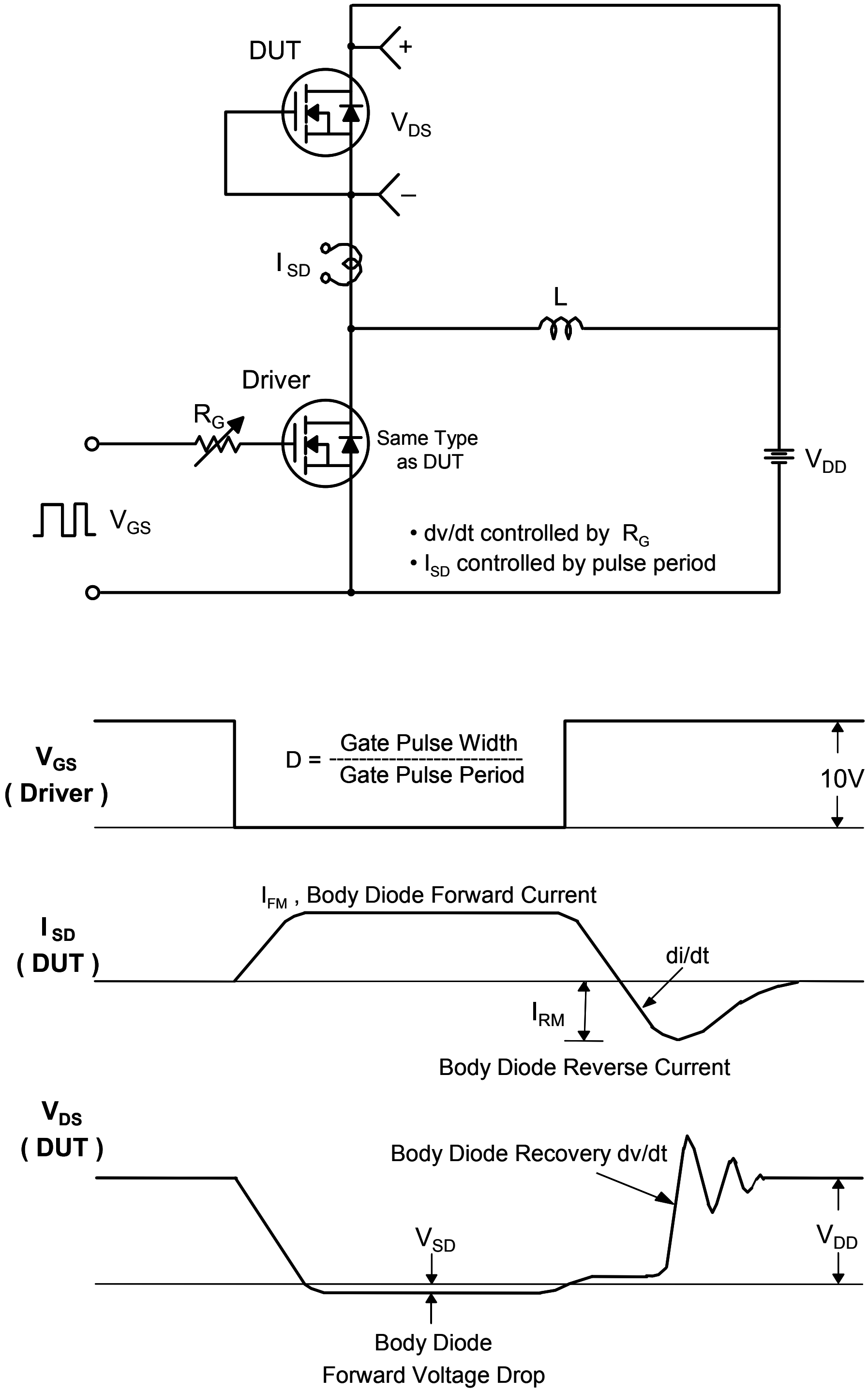
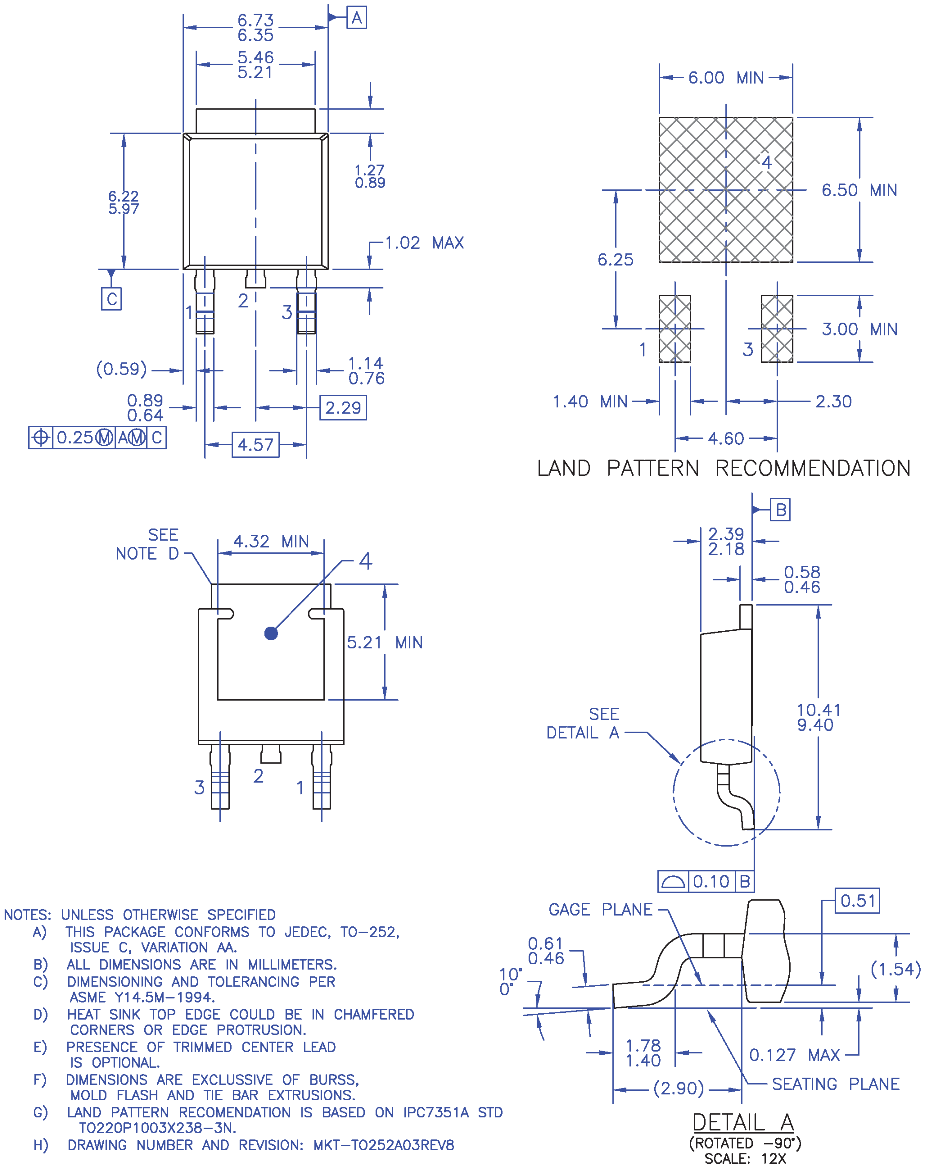


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



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- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
- H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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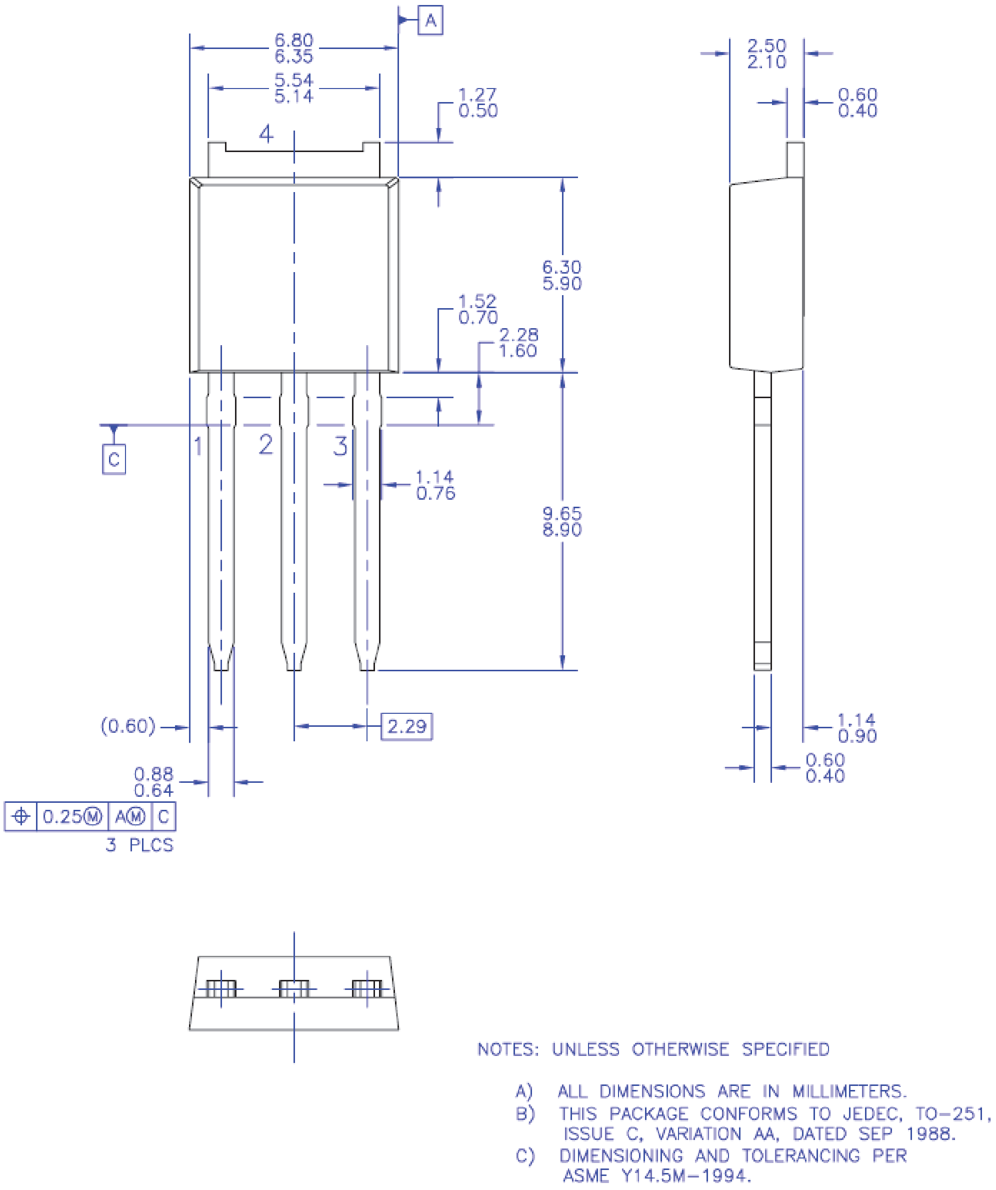

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Figure 17. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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