

# FDW2512NZ

## Dual N-Channel 2.5V Specified PowerTrench® MOSFET

### Features

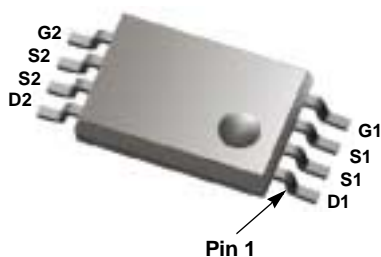
- 6A, 20V  $r_{DS(ON)} = 0.028\Omega$ ,  $V_{GS} = 4.5V$   
 $r_{DS(ON)} = 0.036\Omega$ ,  $V_{GS} = 2.5V$
- Extended  $V_{GS}$  range ( $\pm 12V$ ) for battery applications
- HBM ESD Protection Level of 3.5kV Typical (note 3)
- High performance trench technology for extremely low  $r_{DS(ON)}$
- Low profile TSSOP-8 package

### Applications

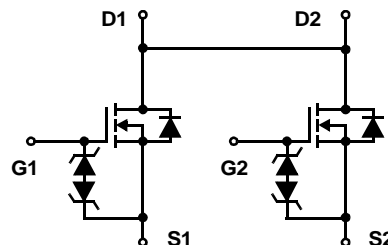
- Load switch
- Battery charge
- Battery disconnect circuits

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.



**TSSOP-8**



FDW2512NZ Dual N-Channel 2.5V Specified PowerTrench® MOSFET

**Absolute Maximum Ratings**  $T_A=25^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^{\circ}\text{C}$ , $V_{GS} = 4.5\text{V}$ , $R_{\theta JA} = 77^{\circ}\text{C/W}$ )	6.0	A
	Continuous ( $T_C = 100^{\circ}\text{C}$ , $V_{GS} = 2.5\text{V}$ , $R_{\theta JA} = 77^{\circ}\text{C/W}$ )	3.3	A
	Pulsed	Figure 4	A
$P_D$	Power dissipation	1.6	W
	Derate above $25^{\circ}\text{C}$	13	mW/ $^{\circ}\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^{\circ}\text{C}$

**Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	77	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	114	$^{\circ}\text{C/W}$

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2512NZ	FDW2512NZ	TSSOP-8	13"	12 mm	2500 units
2512NZ	FDW2512NZ_NL (Note 4)	TSSOP-8	13"	12 mm	2500 units

**Electrical Characteristics**  $T_A = 25^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	20	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$T_A = 100^{\circ}\text{C}$	-	-	5	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
		$V_{GS} = \pm 4.5\text{V}$			$\pm 250$	nA

**On Characteristics**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	0.6	0.8	1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 6.0\text{A}$ , $V_{GS} = 4.5\text{V}$	-	0.017	0.028	$\Omega$
		$I_D = 5.9\text{A}$ , $V_{GS} = 4.0\text{V}$	-	0.018	0.029	
		$I_D = 5.3\text{A}$ , $V_{GS} = 3.1\text{V}$	-	0.019	0.035	
		$I_D = 5.3\text{A}$ , $V_{GS} = 2.5\text{V}$	-	0.022	0.036	

**Dynamic Characteristics**

$C_{ISS}$	Input Capacitance	$V_{DS} = 10\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	670	-	pF	
$C_{OSS}$	Output Capacitance		-	170	-	pF	
$C_{RSS}$	Reverse Transfer Capacitance		-	115	-	pF	
$R_G$	Gate Resistance	$V_{GS} = 0.5\text{V}$ , $f = 1\text{MHz}$	-	4.2	-	$\Omega$	
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{GS} = 0\text{V}$ to 4.5V	$V_{DD} = 10\text{V}$ $I_D = 6.0\text{A}$ $I_g = 1.0\text{mA}$	-	8	12	nC
$Q_{g(2.5)}$	Total Gate Charge at 2.5V	$V_{GS} = 0\text{V}$ to 2.5V		-	5.1	7.6	
$Q_{gs}$	Gate to Source Gate Charge			-	1.1	-	
$Q_{gd}$	Gate to Drain "Miller" Charge			-	2.2	-	

**Switching Characteristics** ( $V_{GS} = 4.5V$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 10V, I_D = 6.0A$ $V_{GS} = 4.5V, R_{GS} = 16\Omega$	-	-	98	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
$t_r$	Rise Time		-	57	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	47	-	ns
$t_f$	Fall Time		-	58	-	ns
$t_{OFF}$	Turn-Off Time		-	-	158	ns

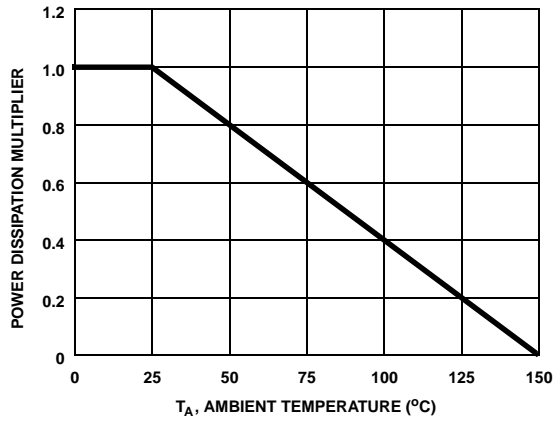
**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 1.3A$	-	0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 6.0A, dI_{SD}/dt = 100A/\mu s$	-	-	24	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 6.0A, dI_{SD}/dt = 100A/\mu s$	-	-	13	nC

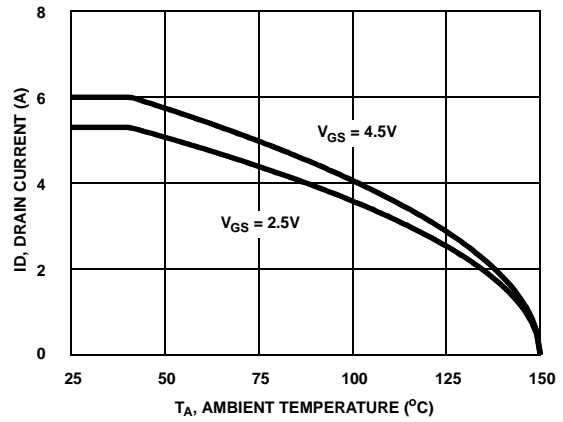
**Notes:**

1.  $R_{\theta JA}$  is 77 °C/W (steady state) when mounted on a 1 inch<sup>2</sup> copper pad on FR-4.
2.  $R_{\theta JA}$  is 114 °C/W (steady state) when mounted on a minimum copper pad on FR-4.
3. The diode connected to the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. FDW2512NZ\_NL is lead free product. FDW2512NZ\_NL marking will appear on the reel label.

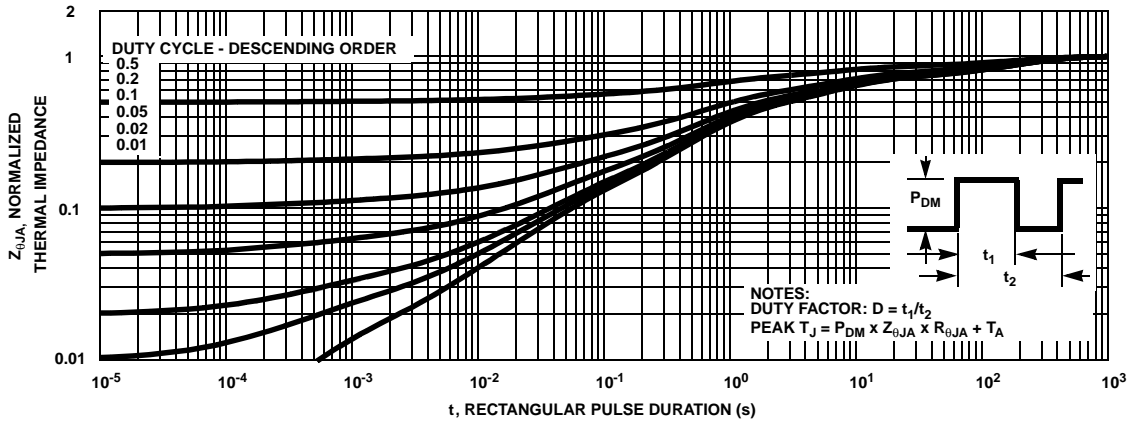
**Typical Characteristic**  $T_A = 25^\circ\text{C}$  unless otherwise noted



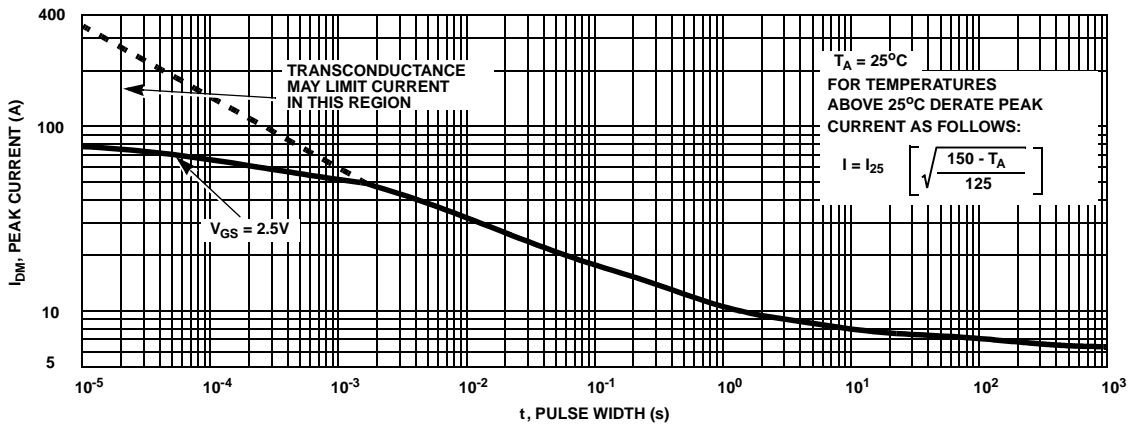
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Ambient Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**



**Figure 4. Peak Current Capability**

**Typical Characteristic** (Continued)  $T_A = 25^\circ\text{C}$  unless otherwise noted

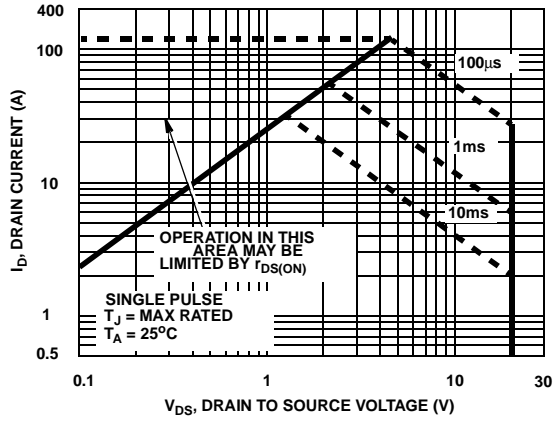


Figure 5. Forward Bias Safe Operating Area

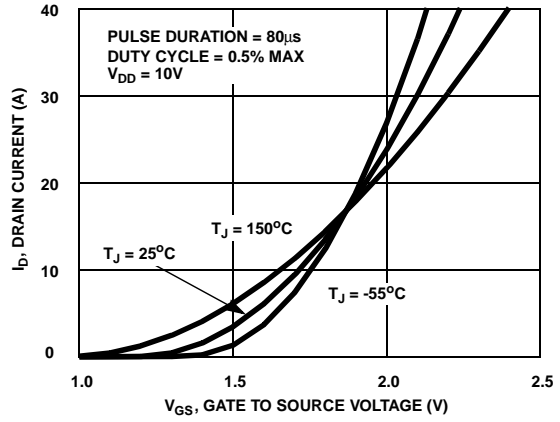


Figure 6. Transfer Characteristics

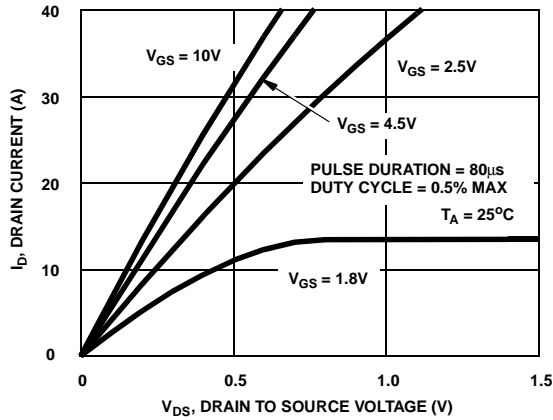


Figure 7. Saturation Characteristics

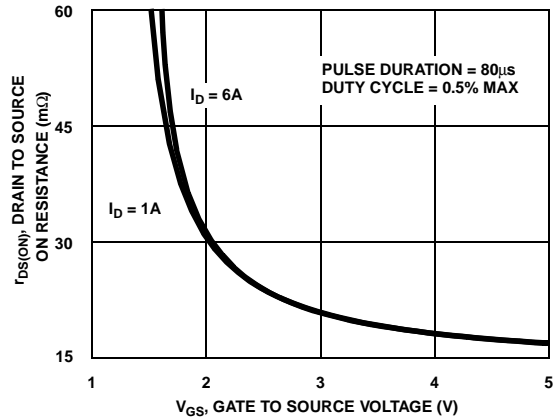


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

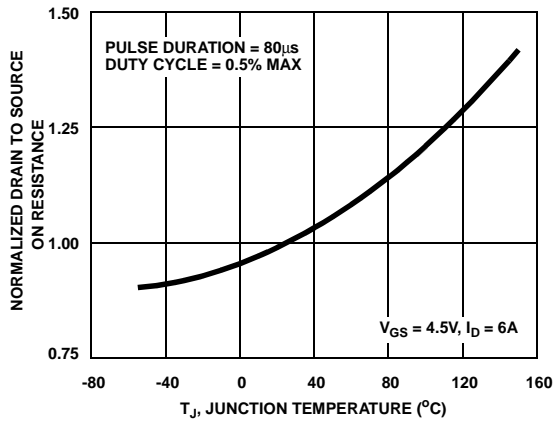


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

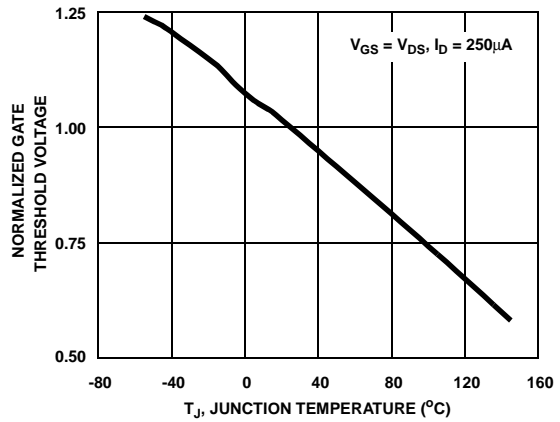
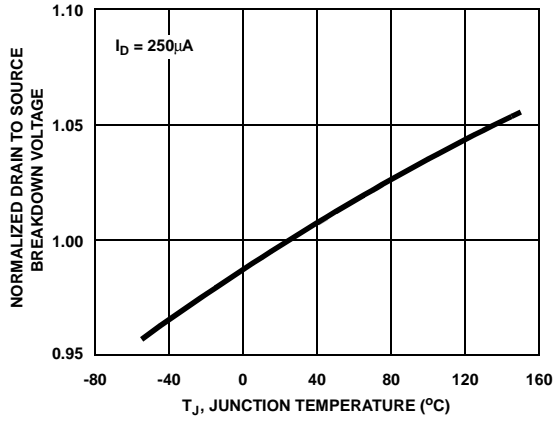
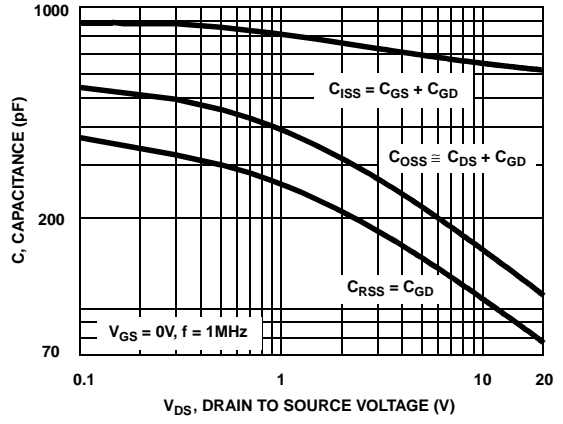


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

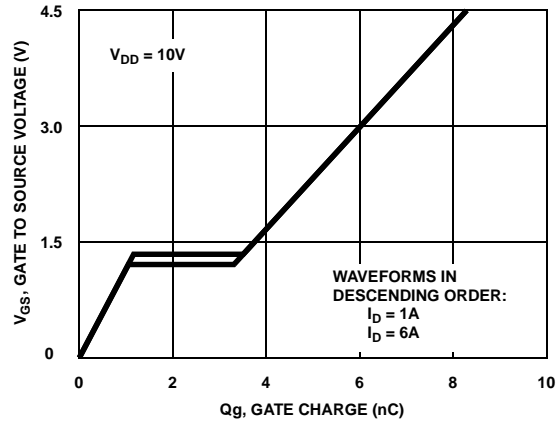
**Typical Characteristic** (Continued)  $T_A = 25^\circ\text{C}$  unless otherwise noted



**Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 12. Capacitance vs Drain to Source Voltage**



**Figure 13. Gate Charge Waveforms for Constant Gate Currents**

### Test Circuits and Waveforms

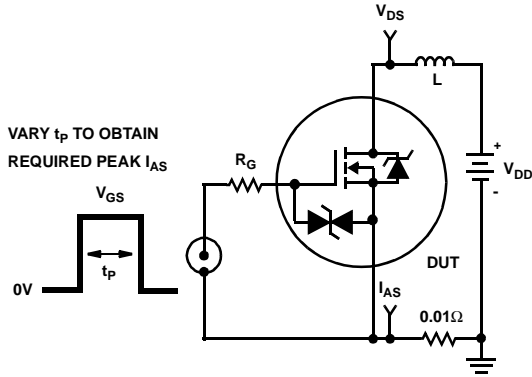


Figure 14. Unclamped Energy Test Circuit

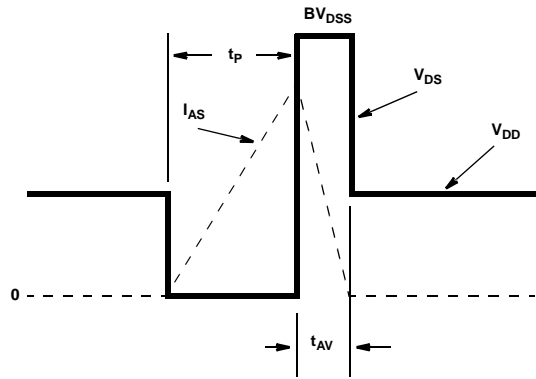


Figure 15. Unclamped Energy Waveforms

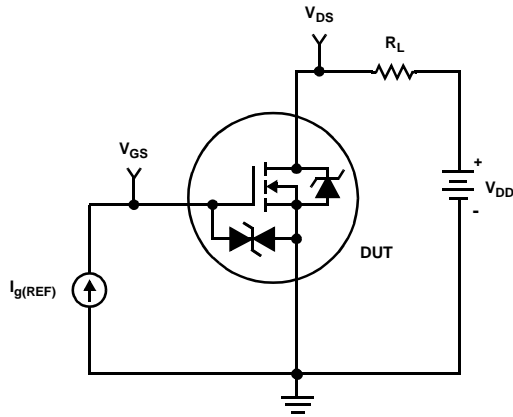


Figure 16. Gate Charge Test Circuit

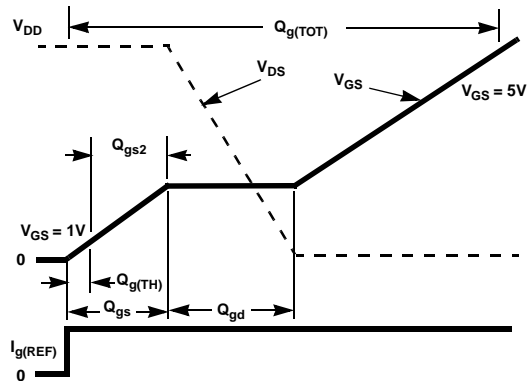


Figure 17. Gate Charge Waveforms

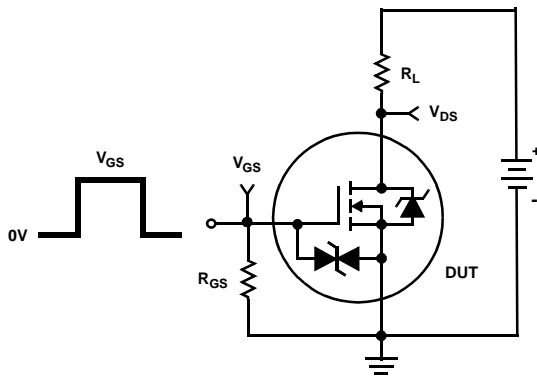


Figure 18. Switching Time Test Circuit

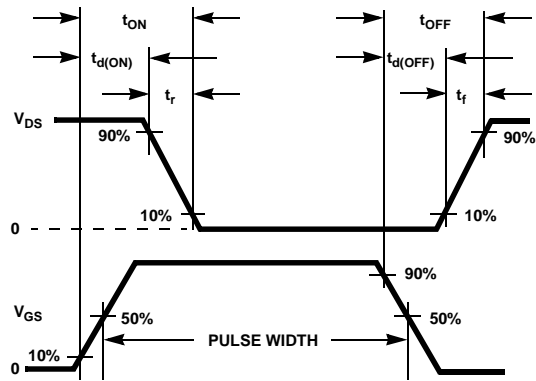


Figure 19. Switching Time Waveforms

**PSPICE Electrical Model**

.SUBCKT FDW2512NZ 2 1 3 ; rev July 2004  
 CA 12 8 8.8e-10  
 CB 15 14 8.8e-10  
 CIN 6 8 0.5e-9

DBODY 5 7 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD  
 DESD1 91 9 DESD1MODE  
 DESD2 91 7 DESD2MOD  
 EBREAK 7 11 17 18 22.2  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 8 6 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 6 20 18 22 1  
 IT 8 17 1  
 LGATE 1 9 1.49e-9  
 LDRAIN 2 5 1e-9 1  
 LGATE 1 9 1.49e-9  
 LSOURCE 3 7 0.2e-9  
 RLDRAIN 2 5 10  
 RLGATE 1 9 14.9  
 RLSOURCE 3 7 2.0

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 13.1e-3  
 RGATE 9 20 5.57  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 2e-4  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

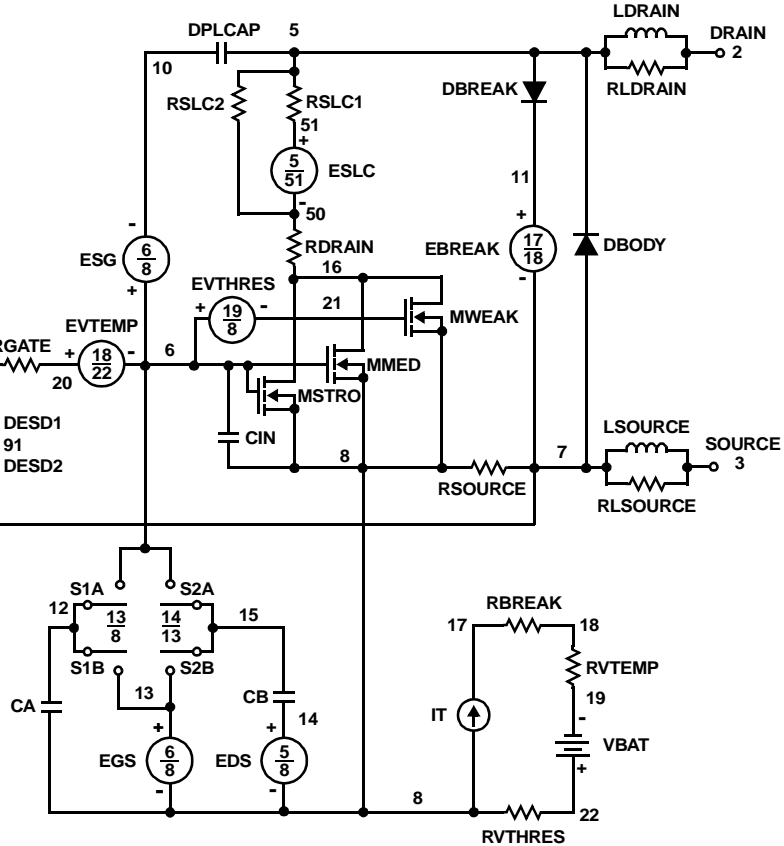
ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) \* (PWR(V(5,51)/(1e-6\*120),2.5)) }

.MODEL DBODYMOD D (IS = 7.3e-12 N=0.93 RS = 20.6e-3 IKF=0.2 TRS1 = 1.7e-3 TRS2 = 2e-6 XTI=0.2 TIKF=0.001  
 CJO = 2.0e-10 TT=1.05e-8 M = 0.58)  
 .MODEL DBREAKMOD D (RS = 1e-1 TRS1 = 9e-3 TRS2 = -2e-5)  
 .MODEL DPLCAPMOD D (CJO = 0.37e-9 IS = 1e-30 N = 10 M = 0.51)  
 .MODEL DESD1MOD D (BV=14 RS=1)  
 .MODEL DESD2MOD D (BV=14 N=1.3 RS=1)  
 .MODEL MMEDMOD NMOS (VTO = 0.96 KP = 1.98 IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 5.57)  
 .MODEL MSTROMOD NMOS (VTO = 1.2 KP = 72 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 0.72 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 55.7 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 6e-4 TC2 = -5e-7)  
 .MODEL RDRAINMOD RES (TC1 = 6e-4 TC2 = 1.2e-5)  
 .MODEL RSLCMOD RES (TC1 = 1e-9 TC2 = 1e-8)  
 .MODEL RSOURCEMOD RES (TC1 = 8.2e-2 TC2 = 1e-6)  
 .MODEL RVTHRESMOD RES (TC1 = -13e-4 TC2 = -2.5e-6)  
 .MODEL RVTEMPMOD RES (TC1 = -1.0e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5 VOFF = -1.5)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = -5)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.4 VOFF = 0.4)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.4 VOFF = -0.4)  
 ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





**SABER Electrical Model**

REV July 2004  
 template fdw2512nz n2,n1,n3  
 electrical n2,n1,n3

```

{
var i iscl
dp..model dbodymod = (isl = 7.3e-12, nl=0.93, rs = 20.6e-3, trs1 = 1.7e-3, trs2 = 2e-6, xti=0.2, cjo = 2.0e-10, ikf=0.2, tt = 1.05e-8,
m = 0.58, tikf=0.001)
dp..model dbreakmod = (rs = 1e-1, trs1 = 9e-3, trs2 = -2.0e-5)
dp..model dplcapmod = (cjo = 0.37e-9, isl=10e-30, nl=10, m=0.51)
dp..model desd1mod = (bv=14, rs=1)
dp..model desd2mod = (bv=14, nl=1.3, rs=1)
m..model mmedmod = (type=_n, vto = 0.96, kp=1.98, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto = 1.2, kp = 72, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 0.72, kp = 0.02, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -5, voff = -1.5)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -1.5, voff = -5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.4, voff = 0.4)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.4, voff = -0.4)
    
```

```

c.ca n12 n8 = 8.8e-10
c.cb n15 n14 = 8.8e-10
c.cin n6 n8 = 0.5e-9
    
```

```

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
dp.desd1 n91 n9 = model=desd1mod
dp.desd2 n91 n7 = model=desd2mod
    
```

```

spe.ebreak n11 n7 n17 n18 = 22.2
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
    
```

```

i.it n8 n17 = 1
    
```

```

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 1.49e-9
l.lsource n3 n7 = 0.2e-9
    
```

```

res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 14.9
res.rlsource n3 n7 = 2.0
    
```

```

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
    
```

```

res.rbreak n17 n18 = 1, tc1 = 6e-4, tc2 = -5e-7
res.rdrain n50 n16 = 13.1e-3, tc1 = 6e-4, tc2 = 1.2e-5
res.rgate n9 n20 = 5.57
res.rslc1 n5 n51 = 1e-6, tc1 = 1e-9, tc2 = 1e-8
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 2e-4, tc1 = 8.2e-2, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -1.0e-3, tc2 = 1e-6
res.rvthres n22 n8 = 1, tc1 = -13e-4, tc2 = -2.5e-6
    
```

```

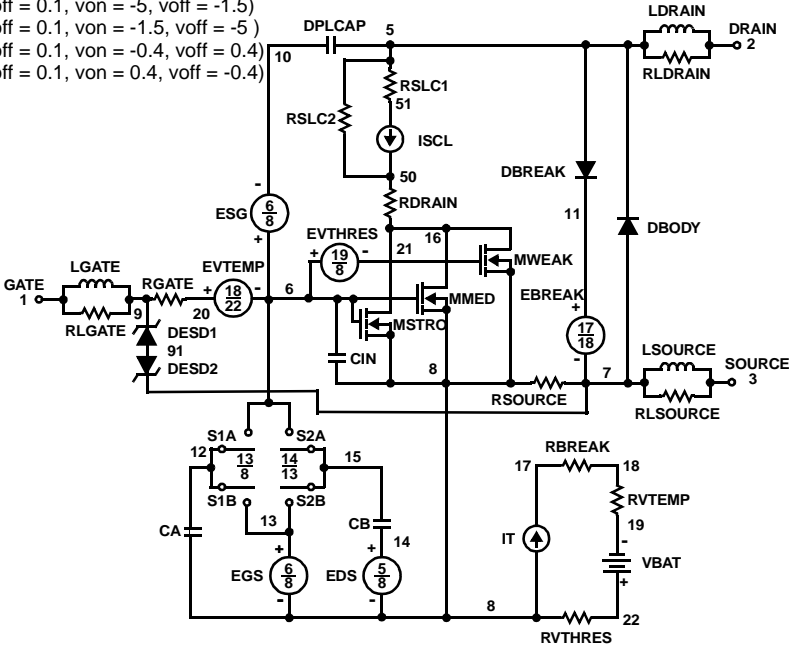
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
    
```

```

v.vbat n22 n19 = dc=1
    
```

```

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/120)** 2.5))
}
}
    
```



**SPICE Thermal Model**

REV July 2004  
 FDW2512NZ\_JA Junction Ambient  
 Minimum copper pad area

CTHERM1 Junction c2 5.7e-4  
 CHERM2 c2 c3 5.72e-4  
 CHERM3 c3 c4 5.8e-4  
 CHERM4 c4 c5 4.7e-3  
 CHERM5 c5 c6 5.1e-3  
 CHERM6 c6 c7 0.02  
 CHERM7 c7 c8 0.2  
 CHERM8 c8 Ambient 6

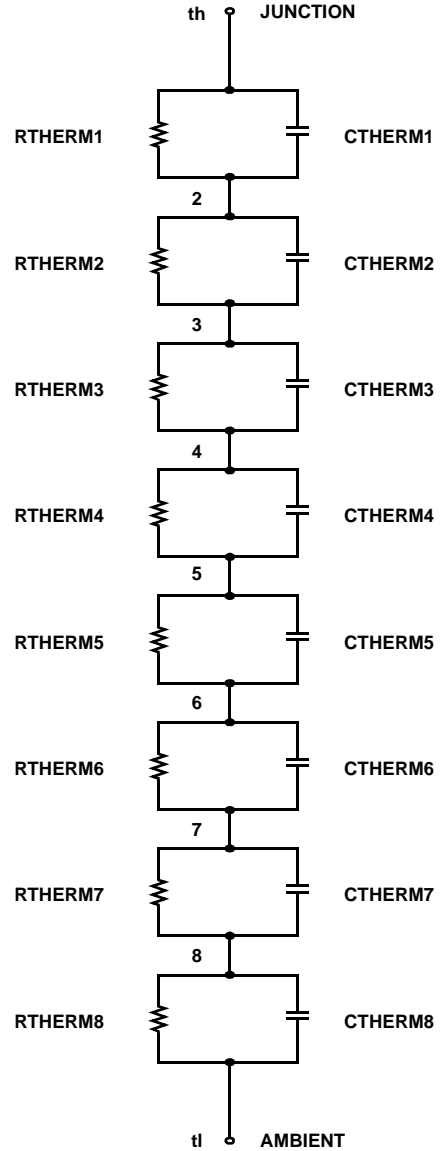
R THERM1 Junction c2 0.003  
 R THERM2 c2 c3 0.25  
 R THERM3 c3 c4 1.0  
 R THERM4 c4 c5 1.1  
 R THERM5 c5 c6 7.5  
 R THERM6 c6 c7 33.6  
 R THERM7 c7 c8 33.7  
 R THERM8 c8 Ambient 33.8

**SABER Thermal Model**

SABER thermal model FDW2512NZ  
 Minimum copper pad area  
 template thermal\_model th tl  
 thermal\_c th, tl

```
{
    ctherm.ctherm1 th c2 = 5.7e-4
    ctherm.ctherm2 c2 c3 = 5.72e-4
    ctherm.ctherm3 c3 c4 = 5.8e-4
    ctherm.ctherm4 c4 c5 = 4.7e-3
    ctherm.ctherm5 c5 c6 = 5.1e-3
    ctherm.ctherm6 c6 c7 = 0.02
    ctherm.ctherm7 c7 c8 = 0.2
    ctherm.ctherm8 c8 tl = 6
}
```

```
rtherm.rtherm1 th c2 = 0.003
rtherm.rtherm2 c2 c3 = 0.25
rtherm.rtherm3 c3 c4 = 1.0
rtherm.rtherm4 c4 c5 = 1.1
rtherm.rtherm5 c5 c6 = 7.5
rtherm.rtherm6 c6 c7 = 33.6
rtherm.rtherm7 c7 c8 = 33.7
rtherm.rtherm8 c8 tl = 33.8
}
```



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ActiveArray™	FAST®	IntelliMAX™	Power247™	SuperFET™
Bottomless™	FASTr™	ISOPLANAR™	PowerEdge™	SuperSOT™-3
CoolFET™	FPS™	LittleFET™	PowerSaver™	SuperSOT™-6
CROSSVOLT™	FRFET™	MICROCOUPLER™	PowerTrench®	SuperSOT™-8
DOME™	GlobalOptoisolator™	MicroFET™	QFET®	SyncFET™
EcoSPARK™	GTO™	MicroPak™	QS™	TinyLogic®
E <sup>2</sup> CMOS™	HiSeC™	MICROWIRE™	QT Optoelectronics™	TINYOPTO™
EnSigna™	I <sup>2</sup> C™	MSX™	Quiet Series™	TruTranslation™
FACT™	i-Lo™	MSXPro™	RapidConfigure™	UHC™
		OCX™	RapidConnect™	UltraFET®
Across the board. Around the world.™		OCXPro™	µSerDes™	UniFET™
The Power Franchise®		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	
		PACMAN™	SPM™	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.